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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z51f3221atx

7.3 A/D Converter Characteristics

Table 7-3 A/D Converter Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution		–		—	12	–	bit
Integral Linear Error	ILE	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±2	LSB
Differential Linearity Error	DLE			–	–	±1	
Zero Offset Error	ZOE			–	–	±3	
Full Scale Error	FSE			–	–	±3	
Conversion Time	t_{CON}	12bit resolution, 8MHz		20	–	–	µS
Analog Input Voltage	V_{AN}	–		AVSS	–	AVREF	V
Analog Reference Voltage	AVREF	–		1.8	–	VDD	
Analog Ground Voltage	AVSS	–		VSS	–	VSS+0.3	
Analog Input Leakage Current	I_{AN}	AVREF= 5.12V		–	–	10	µA
ADC Operating Current	I_{ADC}	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	µA

NOTES) 1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).

2. Full scale error is the difference between 1111111111 and the converted output for full-scale input voltage (AVREF).

7.4 Power-On Reset Characteristics

Table 7-4 Power-On Reset Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	–	V/mS
POR Current	I_{POR}	–	–	0.2	–	µA

7.19 Recommended Circuit and Layout

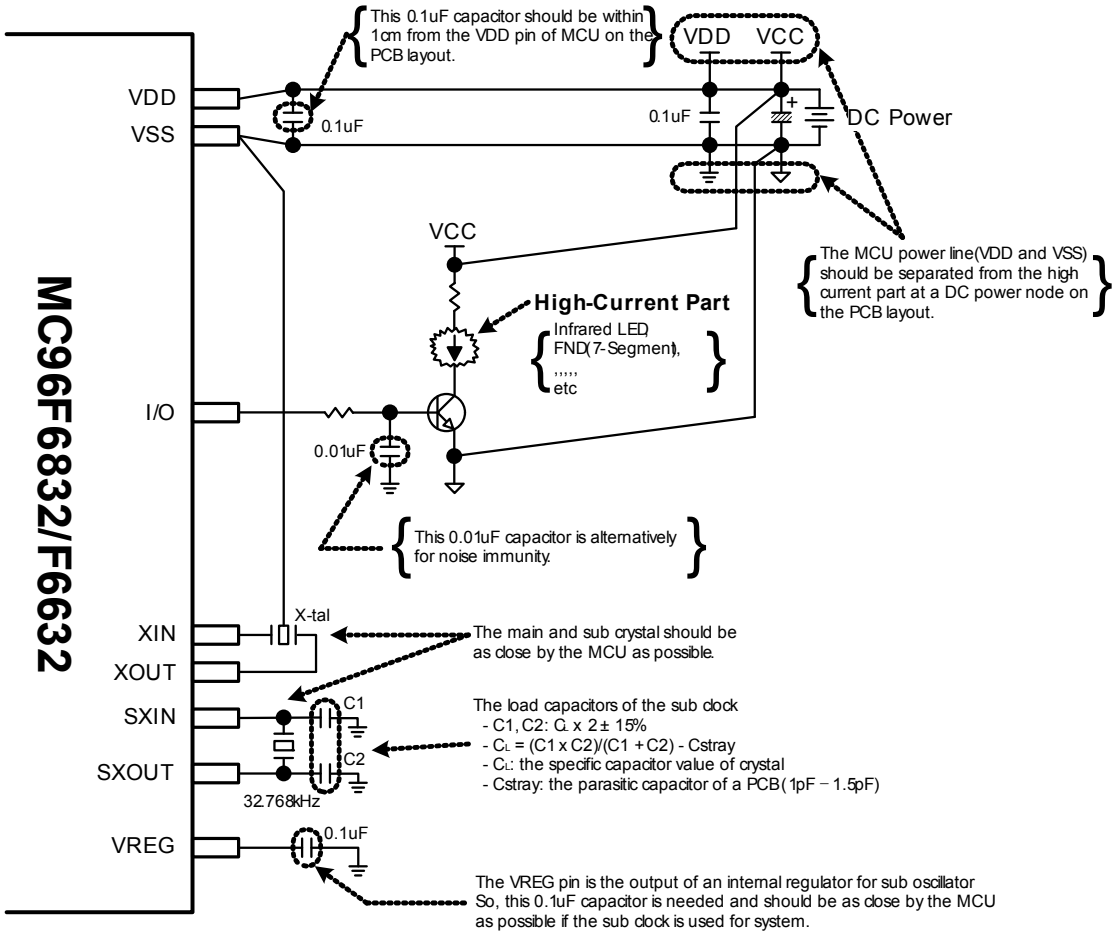


Figure 7.15 Recommended Circuit and Layout

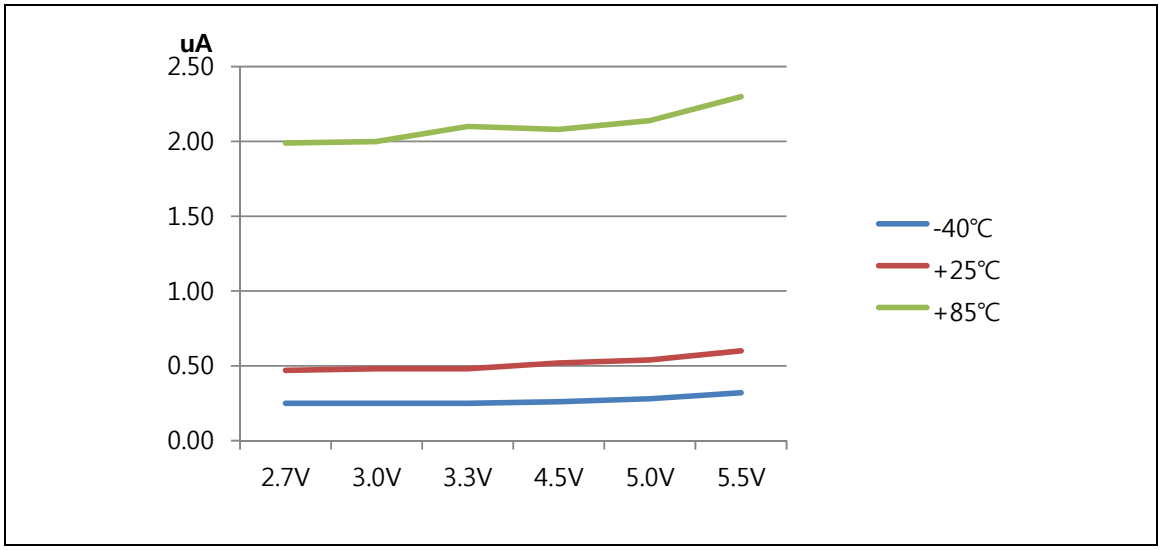


Figure 7.20 STOP (IDD5) Current

8. Memory

The Z51F3221 MCU addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

The Z51F3221 MCU provides on-chip 32k bytes of the ISP type flash program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes and it includes the stack area. External data memory (XRAM) is 1k bytes and it includes 40 bytes of LCD display RAM.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64k bytes, but this device has just 32k bytes program memory space.

Figure 8-1 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 10, for example, is assigned to location 000BH. If external interrupt 10 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

Table 9-1 Register Map (Continued)

Name	Address	Dir	Default	Description
P7	C8H	R/W	00H	P7 Data Register
P7IO	C9H	R/W	00H	P7 Direction Register
P7PU	DDH	R/W	00H	P7 Pull-up Resistor Selection Register
P7OD	CFH	R/W	00H	P7 Open-drain Selection Register
P8	D8H	R/W	FFH	P8 Data Register
P8IO	D1H	R/W	FFH	P8 Direction Register
P8PU	DEH	R/W	00H	P8 Pull-up Resistor Selection Register
P8OD	D2H	R/W	FFH	P8 Open-drain Selection Register
P9CDR	E8H	R/W	00H	P9 Control and Data Register
PFSR0	EDH	R/W	00H	Port Function Selection Register 0
PFSR1	EEH	R/W	00H	Port Function Selection Register 1
PFSR2	EFH	R/W	00H	Port Function Selection Register 2
PFSR3	F1H	R/W	00H	Port Function Selection Register 3
PFSR4	F2H	R/W	00H	Port Function Selection Register 4
PFSR5	F3H	R/W	00H	Port Function Selection Register 5
PFSR6	F4H	R/W	00H	Port Function Selection Register 6
PFSR7	F5H	R/W	00H	Port Function Selection Register 7
PFSR8	F6H	R/W	00H	Port Function Selection Register 8

9.4 P1 Port

9.4.1 P1 Port Description

P1 is 7-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD) . Refer to the port function selection registers for the P1 function selection.

9.4.2 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
–	P16	P15	P14	P13	P12	P11	P10
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 08H

P1[6:0] I/O Data

P1IO (P1 Direction Register) : 91H

7	6	5	4	3	2	1	0
–	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 08H

P1IO[6:0] P1 Data I/O Direction

0 Input

1 Output

NOTE: EINT13 function possible when input

P1PU (P1 Pull-up Resistor Selection Register) : D5H

7	6	5	4	3	2	1	0
–	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1PU[6:0] Configure Pull-up Resistor of P1 Port

0 Disable

1 Enable

P1OD (P1 Open-drain Selection Register) : 93H

7	6	5	4	3	2	1	0
–	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 08H

P1OD[6:0] Configure Open-drain of P1 Port

0 Push-pull output

1 Open-drain output

9.9 P6 Port

9.9.1 P6 Port Description

P6 is 8-bit I/O port. P6 control registers consist of P6 data register (P6), P6 direction register (P6IO), P6 pull-up resistor selection register (P6PU) and P6 open-drain selection register (P6OD). Refer to the port function selection registers for the P6 function selection.

9.9.2 Register description for P6

P6 (P6 Data Register) : C0H

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6[7:0] I/O Data

P6IO (P6 Direction Register) : C1H

7	6	5	4	3	2	1	0
P67IO	P66IO	P65IO	P64IO	P63IO	P62IO	P61IO	P60IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6IO[7:0] P6 Data I/O Direction

0 Input

1 Output

P6PU (P6 Pull-up Resistor Selection Register) : DCH

7	6	5	4	3	2	1	0
P67PU	P66PU	P65PU	P64PU	P63PU	P62PU	P61PU	P60PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6PU[7:0] Configure Pull-up Resistor of P6 Port

0 Disable

1 Enable

P6OD (P6 Open-drain Selection Register) : BBH

7	6	5	4	3	2	1	0
P67OD	P66OD	P65OD	P64OD	P63OD	P62OD	P61OD	P60OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6OD[7:0] Configure Open-drain of P6 Port

0 Push-pull output

1 Open-drain output

PFSR4 (Port Function Selection Register 4) : F2H

7	6	5	4	3	2	1	0
PFSR47	PFSR46	PFSR45	PFSR44	PFSR43	PFSR42	PFSR41	PFSR40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR47 P63 Function select
0 Port
1 SEG19 Function

PFSR46 P62 Function Select
0 Port
1 SEG18 Function

PFSR45 P61 Function select
0 Port
1 SEG17 Function

PFSR44 P60 Function Select
0 Port
1 SEG16 Function

PFSR43 P57 Function select
0 Port
1 SEG15 Function

PFSR42 P56 Function Select
0 Port
1 SEG14 Function

PFSR41 P55 Function select
0 Port
1 SEG13 Function

PFSR40 P54 Function Select
0 Port
1 SEG12 Function

11.3.6 Register Description for Watch Dog Timer

WDTCNT (Watch Dog Timer Counter Register: Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register: Write Case) : 8EH

7	6	5	4	3	2	1	0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value : FFH

WDTDR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTDR Value+1)
NOTE) Do not write “0” in the WDTDR register.

WDTCR (Watch Dog Timer Control Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	–	–	–	–	WDTIFR
R/W	R/W	R/W	–	–	–	–	R/W

Initial value : 00H

WDTEN Control WDT Operation
0 Disable
1 Enable

WDTRSON Control WDT RESET Operation
0 Free Running 8-bit timer
1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.
0 WDT Interrupt no generation
1 WDT Interrupt generation

11.6.3 8-Bit Timer 1 Carrier Frequency Mode.

The carrier frequency and the pulse of data are calculated by the formula in the following sheet .The Figure 11.16 shows the block diagram of Timer 1 for carrier frequency mode.

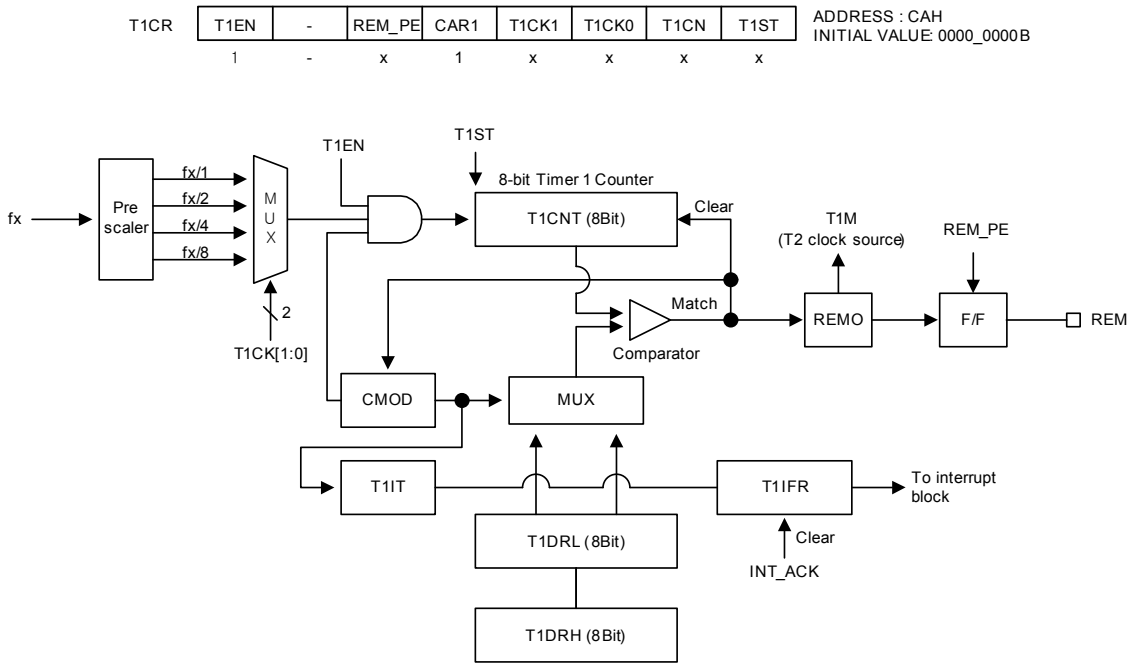


Figure 11.17 Carrier Mode for Timer 1

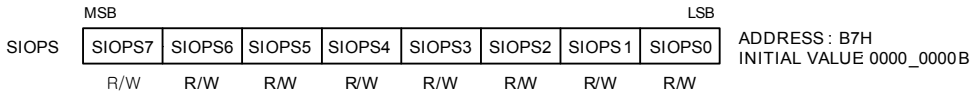
NOTE) When one of T1DRH and T1DRL values is “00H”, the carrier frequency generator (REM) output always becomes a “High” or “Low”. At that time, Timer 1 Interrupt Flag Bit (T1IFR) is not set.

11.10.3 SIO Pre-Scaler Register (SIOPS)

SIOPS contains the SIO pre-scaler value. The SIO clock rate (baud rate) is calculated by the following fomula.

Baud rate = Input clock (fx/4)/(Pre-scaler value + 1)

or SCK input clock, where the input clock is fx/4



Baud rate = (fx/4)/(SIOPS + 1)

Figure 11.27 SIO Pre-Scaler Register (SIOPS)

11.10.4 The usage of SIO

1. Select transmitter/receiver mode.
2. In transmitter mode, write data to be sent to SIODR.
3. Set CCLR to “1” to clear SIO counter and start shifting.
4. If Tx or Rx is completed, the SiO interrupt is generated and SIOIFR is set to “1”.
5. In receiver mode, the received data can be acquired by reading SIODR.

11.12.8 UART Transmitter

The UART transmitter is enabled by setting the TXE bit in UARTCR2 register. When the Transmitter is enabled, the TXD pin should be set to TXD function for the serial output pin of UART by the PFSR6[7:6] or PFSR8[5:4]. The baud-rate, operation mode and frame format must be setup once before doing any transmission. In synchronous operation mode, the ACK pin is used as transmission clock, so it should be selected to do ACK function by PFSR6[5:4] or PFSR8[3:2].

11.12.8.1 Sending Tx data

A data transmission is initiated by loading the transmit buffer (UARTDR register I/O location) with the data to be transmitted. The data written in transmit buffer is moved to the shift register when the shift register is ready to send a new frame. The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded with new data, it will transfer one complete frame according to the settings of control registers. If the 9-bit characters are used in asynchronous or synchronous operation mode, the ninth bit must be written to the TX8 bit in UARTCR3 register before it is loaded to the transmit buffer (UARTDR register).

11.12.8.2 Transmitter flag and interrupt

The UART transmitter has 2 flags which indicate its state. One is UART data register empty flag (UDRE) and the other is transmit complete flag (TXC). Both flags can be interrupt sources.

UDRE flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains data to be transmitted but has not yet been moved into the shift register. And also this flag can be cleared by writing ‘0’ to this bit position. Writing ‘1’ to this bit position is prevented.

When the data register empty interrupt enable (UDRIE) bit in UARTCR2 register is set and the global interrupt is enabled, UARTST data register empty interrupt is generated while UDRE flag is set.

The transmit complete (TXC) flag bit is set when the entire frame in the transmit shift register has been shifted out and there is no more data in the transmit buffer. The TXC flag is automatically cleared when the transmit complete interrupt service routine is executed, or it can be cleared by writing ‘0’ to TXC bit in UARTST register.

When the transmit complete interrupt enable (TXCIE) bit in UARTCR2 register is set and the global interrupt is enabled, UART transmit complete interrupt is generated while TXC flag is set.

11.12.9.5 Asynchronous Data Reception

To receive asynchronous data frame, the UART includes a clock and data recovery unit. The clock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXD pin.

The data recovery logic samples and low pass filters the incoming bits, and this removes the noise of RXD pin.

The next figure illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times of the baud-rate in normal mode. The horizontal arrows show the synchronization variation due to the asynchronous sampling process.

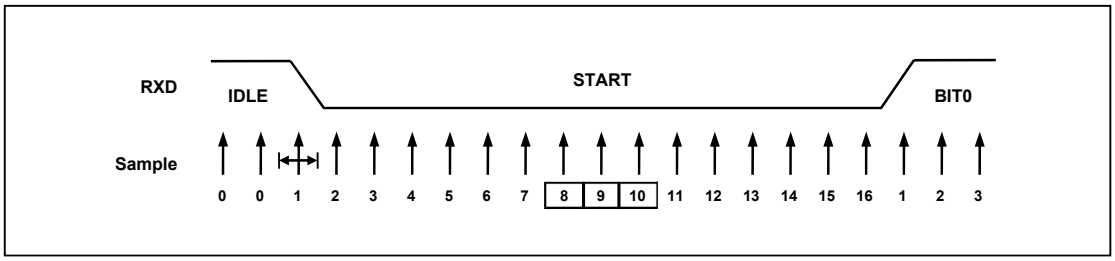


Figure 11.39 Start Bit Sampling

When the receiver is enabled (RXE=1), the clock recovery logic tries to find a high-to-low transition on the RXD line, the start bit condition. After detecting high to low transition on RXD line, the clock recovery logic uses samples 8,9, and 10 for normal mode to decide if a valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. And the data recovery can begin. The synchronization process is repeated for each start bit.

As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost similar to the clock recovery process. The data recovery logic samples 16 times for each incoming bits, and uses sample 8, 9, and 10 to decide data value. If more than 2 samples have low levels, the received bit is considered to a logic ‘0’ and if more than 2 samples have high levels, the received bit is considered to a logic ‘1’. The data recovery process is then repeated until a complete frame is received including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the Receiver is in idle state and waiting to find start bit.

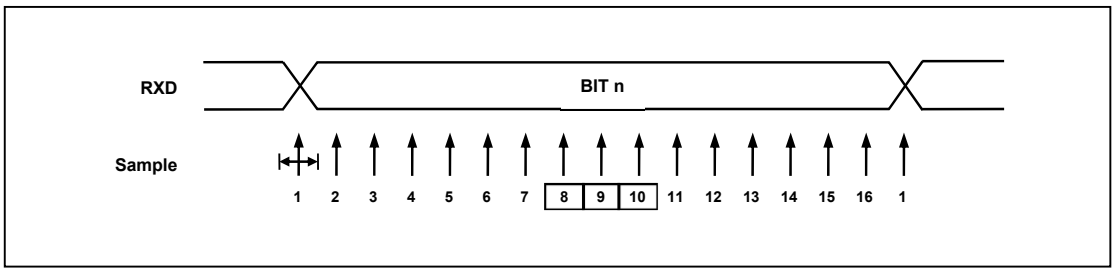


Figure 11.40 Sampling of Data and Parity Bit

11.12.13 Baud Rate setting (example)

Table 11-18 Examples of UARTBD Settings for Commonly Used Oscillator Frequencies

Baud Rate	fx=1.00MHz		fx=1.8432MHz		fx=2.00MHz	
	UARTBD	ERROR	UARTBD	ERROR	UARTBD	ERROR
2400	25	0.2%	47	0.0%	51	0.2%
4800	12	0.2%	23	0.0%	25	0.2%
9600	6	-7.0%	11	0.0%	12	0.2%
14.4k	3	8.5%	7	0.0%	8	-3.5%
19.2k	2	8.5%	5	0.0%	6	-7.0%
28.8k	1	8.5%	3	0.0%	3	8.5%
38.4k	1	-18.6%	2	0.0%	2	8.5%
57.6k	-	-	1	-25.0%	1	8.5%
76.8k	-	-	1	0.0%	1	-18.6%
115.2k	-	-	-	-	-	-
230.4k	-	-	-	-	-	-

(continued)

Baud Rate	fx=3.6864MHz		fx=4.00MHz		fx=7.3728MHz	
	UARTBD	ERROR	UARTBD	ERROR	UARTBD	ERROR
2400	95	0.0%	103	0.2%	191	0.0%
4800	47	0.0%	51	0.2%	95	0.0%
9600	23	0.0%	25	0.2%	47	0.0%
14.4k	15	0.0%	16	2.1%	31	0.0%
19.2k	11	0.0%	12	0.2%	23	0.0%
28.8k	7	0.0%	8	-3.5%	15	0.0%
38.4k	5	0.0%	6	-7.0%	11	0.0%
57.6k	3	0.0%	3	8.5%	7	0.0%
76.8k	2	0.0%	2	8.5%	5	0.0%
115.2k	1	0.0%	1	8.5%	3	0.0%
230.4k	-	-	-	-	1	0.0%
250k	-	-	-	-	1	-7.8%
0.5M	-	-	-	-	-	-

(continued)

Baud Rate	fx=8.00MHz		fx=11.0592MHz	
	UARTBD	ERROR	UARTBD	ERROR
2400	207	0.2%	-	-
4800	103	0.2%	143	0.0%
9600	51	0.2%	71	0.0%
14.4k	34	-0.8%	47	0.0%
19.2k	25	0.2%	35	0.0%
28.8k	16	2.1%	23	0.0%
38.4k	12	0.2%	17	0.0%
57.6k	8	-3.5%	11	0.0%
76.8k	6	-7.0%	8	0.0%
115.2k	3	8.5%	5	0.0%
230.4k	1	8.5%	2	0.0%
250k	1	0.0%	2	-7.8%
0.5M	-	-	-	-
1M	-	-	-	-

11.13 LCD Driver

11.13.1 Overview

The LCD driver is controlled by the LCD Control Register (LCDCRH/L). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCDCRH and LCDCRL values to logic ‘0’.

The LCD display can continue operating during IDLE and STOP modes if a sub-frequency clock is used as system clock source.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don’t rewrite LCDCRH frequently.

11.13.5 Block Diagram

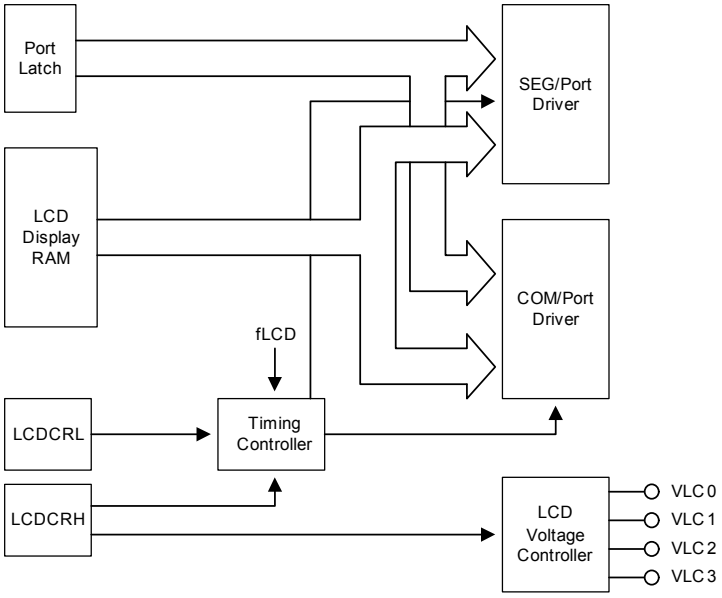


Figure 11.49 LCD Circuit Block Diagram

NOTE) The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don't rewrite LCDCRH frequently

11.13.6 Register Map

Table 11-19 LCD Register Map

Name	Address	Dir	Default	Description
LCDCRH	ECH	R/W	00H	LCD Driver Control High Register
LCDCRL	EBH	R/W	00H	LCD Driver Control Low Register

11.13.7 LCD Driver Register Description

LCD driver register has two control registers, LCD driver control high register (LCDCRH) and LCD driver control low register (LCDCRL).

11.13.8 Register Description for LCD Driver

LCDCRH (LCD Driver Control High Register) : ECH

7	6	5	4	3	2	1	0
LCDDR	LD_B3	LD_B2	LD_B1	LD_B0	LCLK1	LCLK0	DISP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

LCDDR LCD Driving Resistor for Bias Select

0 Internal LCD driving resistors for bias

1 External LCD driving resistor for bias

LD_B[3:0] LCD Duty and Bias Select (NOTE)

LD_B3	LD_B2	LD_B1	LD_B0	Description
0	0	0	0	1/2Duty, 1/2Bias (100k ohm)
0	0	0	1	1/2Duty, 1/2Bias (50k ohm)
0	0	1	0	1/2Duty, 1/3Bias (50k ohm)
0	0	1	1	1/3Duty, 1/2Bias (100k ohm)
0	1	0	0	1/3Duty, 1/2Bias (50k ohm)
0	1	0	1	1/3Duty, 1/3Bias (50k ohm)
0	1	1	0	1/4Duty, 1/2Bias (100k ohm)
0	1	1	1	1/4Duty, 1/2Bias (50k ohm)
1	0	0	0	1/4Duty, 1/3Bias (50k ohm)
1	0	0	1	Not available
1	0	1	0	Not available
1	0	1	1	1/5Duty, 1/3Bias (50k ohm)
1	1	0	0	1/6Duty, 1/3Bias (50k ohm)
1	1	0	1	1/6Duty, 1/4Bias (50k ohm)
1	1	1	0	1/8Duty, 1/3Bias (50k ohm)
1	1	1	1	1/8Duty, 1/4Bias (50k ohm)

LCLK[1:0] LCD Clock Select (When f_{WCK}(Watch timer clock)= 32.768 kHz)

LCLK1	LCLK0	Description
0	0	f_{LCD} = 128Hz
0	1	f_{LCD} = 256Hz
1	0	f_{LCD} = 512Hz
1	1	f_{LCD} = 1024Hz

NOTE) The LCD clock is generated by watch timer clock (f_{WCK}). So the watch timer should be enabled when the LCD display is turned on.

DISP LCD Display Control

0 Display off

1 Normal display on

NOTES) 1. When 1/2 bias is selected, the bias levels are set as VLC0, VLC2, and VSS
2. When 1/3 bias is selected, the bias levels are set as VLC0, VLC1, VLC2 (=VLC3), and VSS
3. When 1/4 bias is selected, the bias levels are set as VLC0, VLC1, VLC2, VLC3, and VSS
4. The bias levels are automatically set with appropriate bias circuit when internal bias resistors are used.
5. A bias circuit is connected like the “11.13.4 LCD Voltage Dividing Resistor Connection” and should be selected as an appropriate value for “LD_B[3:0]”.

12. Power Down Operation

12.1 Overview

The Z51F3221 MCU features two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, Sub-IDLE and STOP mode. In three modes, program is stopped.

12.2 Peripheral Operation in IDLE/STOP Mode

Table 12-1 Peripheral Operation during Power Down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~3	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
SIO	Operates Continuously	Only operate with external clock
UART	Operates Continuously	Stop
LCD Controller	Operates Continuously	Stop (Can be operated with sub clock)
Internal OSC (8MHz)	Oscillation	Stop when the system clock (fx) is f_{IRC}
WDTRC OSC (6kHz)	Stop	Can be operated with setting value
Main OSC (1~12MHz)	Oscillation	Stop when fx = f_{XIN}
Sub OSC (32.768kHz)	Oscillation	Stop when fx = f_{SUB}
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0,EC3), SIO (External clock), External Interrupt, UART by ACK, WT (sub clock), WDT

12.5.1 Register Map

Table 12-2 Power Down Operation Register Map

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register

12.5.2 Power Down Operation Register Description

The power down operation register consists of the power control register (PCON).

12.5.3 Register Description for Power Down Operation

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value : 00H

PCON[7:0] Power Control

01H IDLE mode enable

03H STOP mode enable

NOTES) 1. To enter IDLE mode, PCON must be set to ‘01H’.

2. To enter STOP mode, PCON must be set to ‘03H’.

3. The PCON register is automatically cleared by a release signal in STOP/IDLE mode.

4. Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples.

```
Ex1)  MOV   PCON, #01H   ; IDLE mode
      NOP
      NOP
      NOP
       •
       •
       •

Ex2)  MOV   PCON, #03H   ; STOP mode
      NOP
      NOP
      NOP
       •
       •
       •
```

Table 13-2 Boot Process Description

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection	-about 1.4V
③	- (INT-OSC 8MHz/8)x256x28h Delay section (=10ms) -VDD input voltage must rise over than flash operating voltage for Config read	-Slew Rate >= 0.15V/ms
④	- Config read point	-about 1.5V ~ 1.6V -Config Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR or Ext_reset release
⑥	- Reset Release section (BIT overflow) i) after16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	