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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	104
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	28K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f463capmc-gsk5e2

Contents

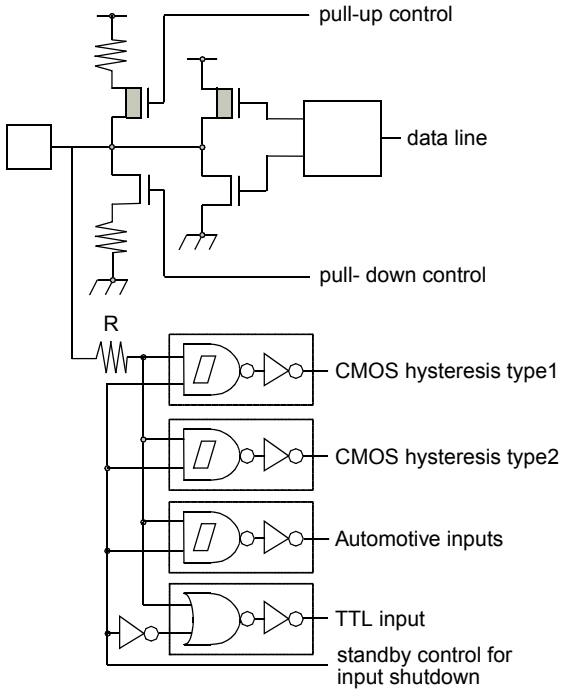
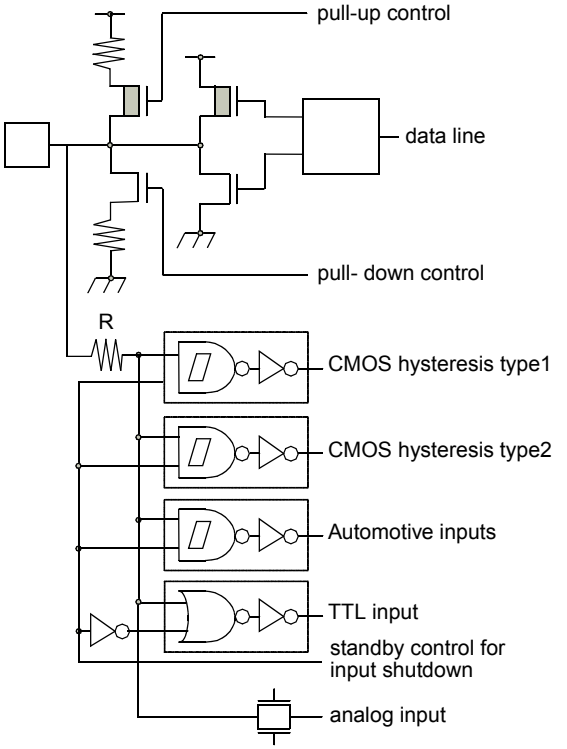
Feature	MB91V460	MB91F463CA	MB91F465CA	MB91F467CA MB91F467CB
I^2C (400K)	4 ch	3 ch	3 ch	3 ch
FR external bus	yes (32bit addr, 32bit data)	-	-	-
External Interrupts	16 ch	15 ch	15 ch	15 ch
NMI Interrupts	1 ch	1 ch	1 ch	1 ch
SMC	6 ch	6 ch	6 ch	6 ch
LCD controller (40x4)	1 ch	-	-	-
ADC (10-bit)	32 ch	30 ch	30 ch	30 ch
Alarm Comparator	2 ch	1 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes	yes
Clock Supervisor	yes	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32kHz	32kHz	32kHz	32kHz
RC oscillator	100kHz	100kHz / 2MHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 20	x 25	x 25	x 25
DSU4	yes	no	no	no
EDSU	yes (32 BP)*1	yes (8 BP)*1	yes (16 BP)*1	yes (16 BP)*1
Supply voltage	3V/5V	3V/5V	3V/5V	3V/5V
Regulator	yes	yes	yes	yes
Power consumption	n.a.	< 1 W	< 1 W	< 1 W
Temperature Range (Ta)	0.70 C	-40.105 C	-40.105 C	-40.105 C
Package	BGA660	QFP-144	QFP-144	QFP-144
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 5 sec. typical	< 5 sec. typical	< 6 sec typical

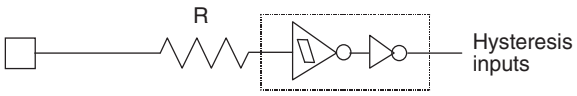
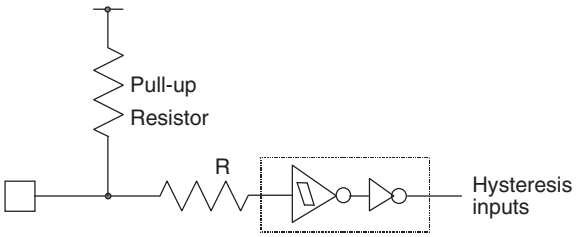
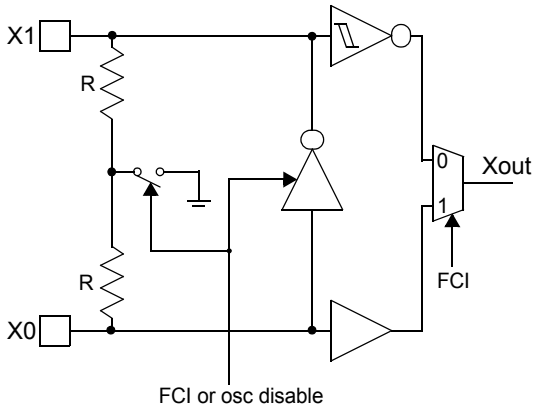
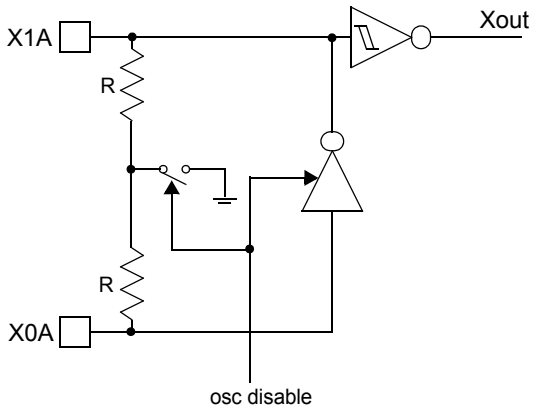
*1: MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

Pin no.	Pin name	I/O	I/O circuit type*	Function
122	P26_0	I/O	F	General-purpose input/output ports
	SMC1P2			Controller output pin of Stepper motor
	AN24			Analog input pins of A/D converter
123	P26_1	I/O	F	General-purpose input/output ports
	SMC1M2			Controller output pin of Stepper motor
	AN25			Analog input pins of A/D converter
124	P26_2	I/O	F	General-purpose input/output ports
	SMC2P2			Controller output pin of Stepper motor
	AN26			Analog input pins of A/D converter
125	P26_3	I/O	F	General-purpose input/output ports
	SMC2M2			Controller output pin of Stepper motor
	AN27			Analog input pins of A/D converter
128	P26_4	I/O	F	General-purpose input/output ports
	SMC1P3			Controller output pin of Stepper motor
	AN28			Analog input pins of A/D converter
129	P26_5	I/O	F	General-purpose input/output ports
	SMC1M3			Controller output pin of Stepper motor
	AN29			Analog input pins of A/D converter
130	P26_6	I/O	F	General-purpose input/output ports
	SMC2P3			Controller output pin of Stepper motor
	AN30			Analog input pins of A/D converter
131	P26_7	I/O	F	General-purpose input/output ports
	SMC2M3			Controller output pin of Stepper motor
	AN31			Analog input pins of A/D converter
132	P25_0	I/O	E	General-purpose input/output ports
	SMC1P4			Controller output pin of Stepper motor
133	P25_1	I/O	E	General-purpose input/output ports
	SMC1M4			Controller output pin of Stepper motor
134	P25_2	I/O	E	General-purpose input/output ports
	SMC2P4			Controller output pin of Stepper motor
135	P25_3	I/O	E	General-purpose input/output ports
	SMC2M4			Controller output pin of Stepper motor
138	P25_4	I/O	E	General-purpose input/output ports
	SMC1P5			Controller output pin of Stepper motor
139	P25_5	I/O	E	General-purpose input/output ports
	SMC1M5			Controller output pin of Stepper motor

[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109	VSS5	Supply	Ground pins
117, 127, 137	HVSS5		Ground pins for Stepper motor controller
18, 36, 54, 72, 90, 108, 144	VDD5		Power supply pins
116, 126, 136	HVDD5		Power supply pins for Stepper motor controller
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

(Continued)

5.6 Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

9.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

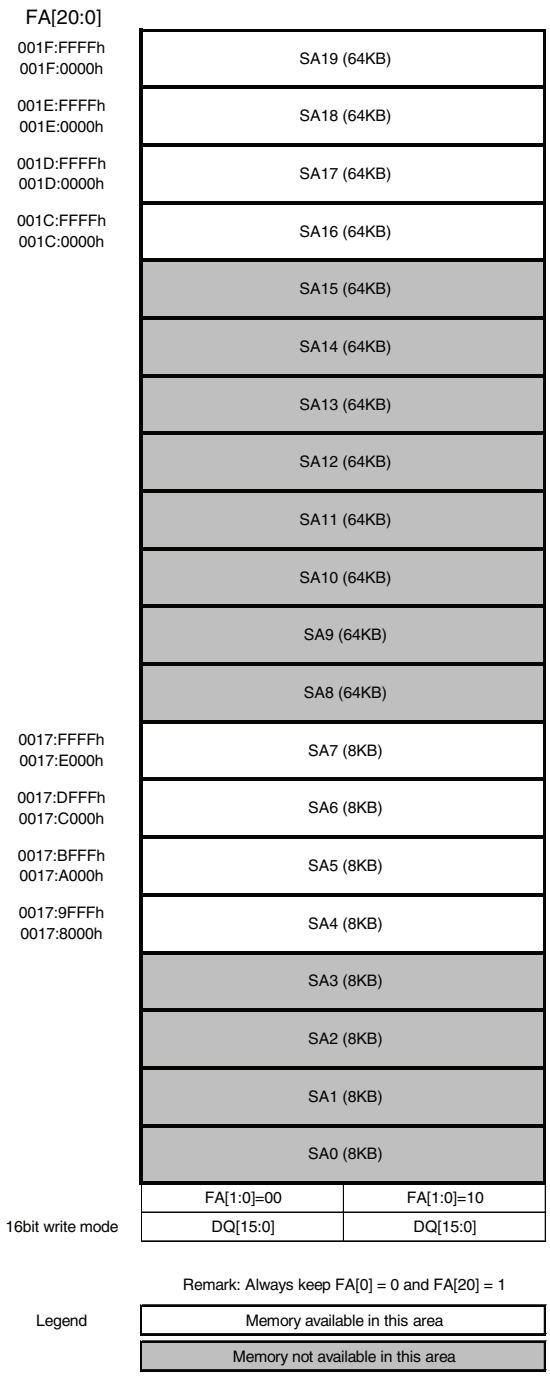
Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 100 MHz	1	1	3	-	4	

Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	1	8	

MB91F463CA


FA[20:0]
001F:FFFFh
001F:0000h
SA19 (64KB)
001E:FFFFh
001E:0000h
SA18 (64KB)
001D:FFFFh
001D:0000h
SA17 (64KB)
001C:FFFFh
001C:0000h
SA16 (64KB)
SA15 (64KB)
SA14 (64KB)
SA13 (64KB)
SA12 (64KB)
SA11 (64KB)
SA10 (64KB)
SA9 (64KB)
SA8 (64KB)
0017:FFFFh
0017:E000h
SA7 (8KB)
0017:DFFFh
0017:C000h
SA6 (8KB)
0017:BFFFh
0017:A000h
SA5 (8KB)
0017:9FFFh
0017:8000h
SA4 (8KB)
SA3 (8KB)
SA2 (8KB)
SA1 (8KB)
SA0 (8KB)
FA[1:0]=00
FA[1:0]=10
16bit write mode
DQ[15:0]
DQ[15:0]
Remark: Always keep FA[0] = 0 and FA[20] = 1
Legend
Memory available in this area
Memory not available in this area

9.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

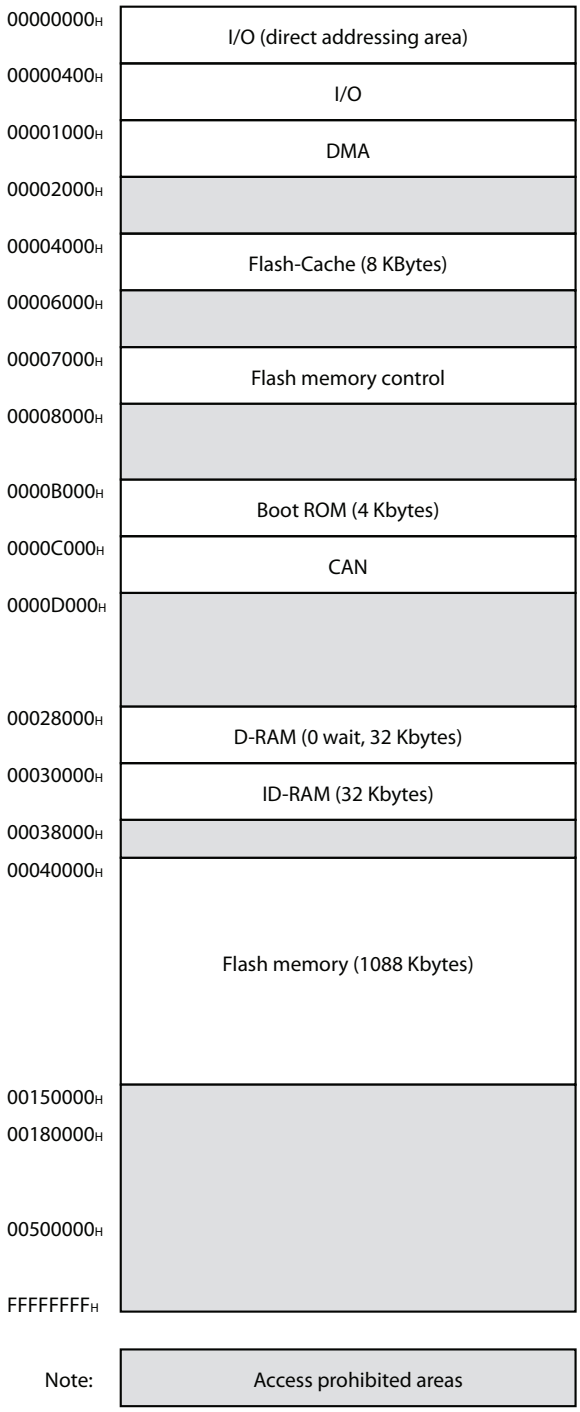
Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F465CA, MB91F467Cx external pins			Comment
		Flash memory mode	Normal function	Pin number	
—	INITX	—	INITX	84	
RESET	—	FRSTX	NMIX	85	
—	—	MD_2	MD_2	76	Set to ‘1’
—	—	MD_1	MD_1	75	Set to ‘1’
—	—	MD_0	MD_0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP28_0	100	
BYTE	Internally fixed to ‘H’	BYTEX	GP28_2	102	
WE	Internal control signal + control via interface circuit	WEX	GP28_5	111	
OE		OEX	GP28_4	110	
CE		CEX	GP20_0	38	
—		ATDIN	GP17_7	27	Set to ‘0’
—		EQIN	GP17_6	26	Set to ‘0’
—		TESTX	GP28_3	103	Set to ‘1’
—		RDYI	GP28_1	101	Set to ‘0’
A-1	Internal address bus	FA0	GP17_5	25	Set to ‘0’
A0 to A3		FA1 to FA4	GP29_0 to GP29_3	92 to 95	
A4 to A7		FA5 to FA8	GP29_4 to GP29_7	96 to 99	
A8 to A11		FA9 to FA12	GP16_0 to GP16_3	28 to 31	
A12 to A15		FA13 to FA16	GP16_4 to GP16_7	32 to 35	
A16 to A18		FA17 to FA19	GP15_0 to GP15_2	20 to 22	
A19		FA20	GP15_3	23	Set to ‘1’ on MB91F463CA, MB91F465CA
—		FA21	GP17_4	24	Set to ‘1’
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP14_0 to GP14_7	10 to 17	
DQ8 to DQ15		DQ8 to DQ15	GP02_0 to GP02_7	2 to 9	

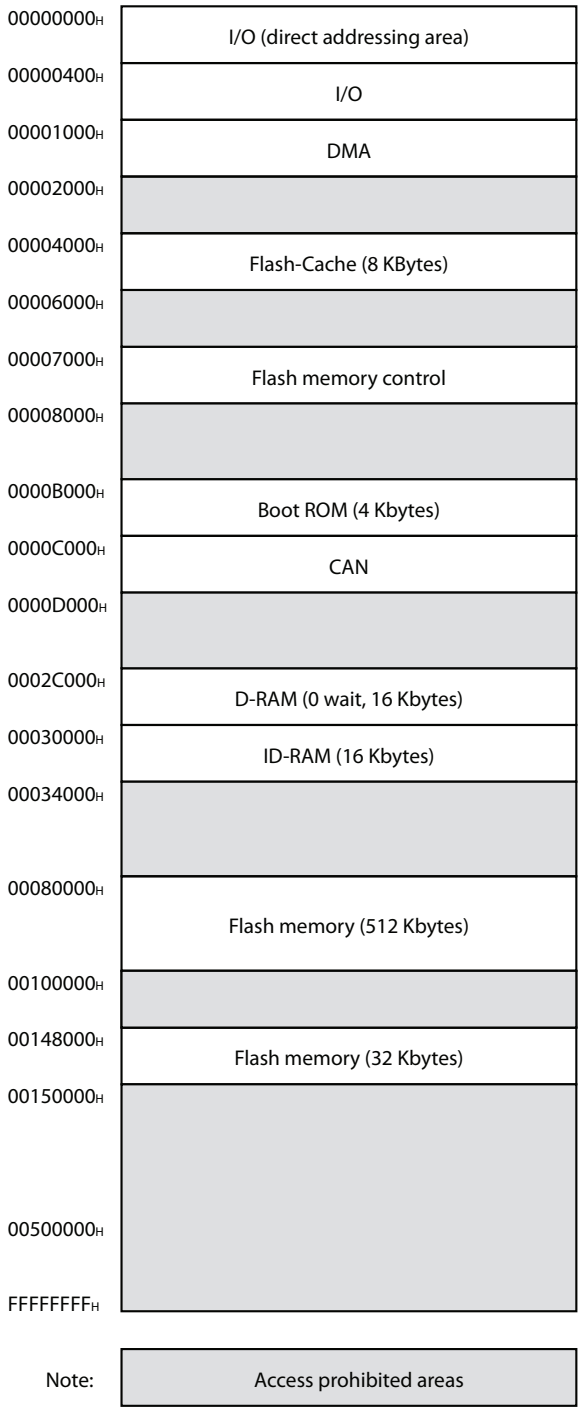
11. Memory Maps

11.1 MB91F467Cx, MB91F465CA

MB91F467Cx



MB91F465CA



Address	Register				Block
	+0	+1	+2	+3	
$0000B8_H$	PWC25 [R/W] - - - - - - XX XXXXXXXX		PWC15 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 5
$0000BC_H$	Reserved	Reserved	PWS25 [R/W] -0000000	PWS15 [R/W] - -000000	
$0000C0_H$	Reserved	PWC0 [R/W] -00000--	Reserved	PWC1 [R/W] -00000--	Stepper Motor Control 0 to 5
$0000C4_H$	Reserved	PWC2 [R/W] -00000--	Reserved	PWC3 [R/W] -00000--	
$0000C8_H$	Reserved	PWC4 [R/W] -00000--	Reserved	PWC5 [R/W] -00000--	
$0000CC_H$	Reserved				Reserved
0000D0H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
0000D4H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	
$0000DC_H$ to 000100_H	Reserved				Reserved
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H to $00012C_H$	Reserved				Reserved
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				Reserved
000240_H	DMACR [R/W] 0 - -0 0000	Reserved			

Address	Register				Block
	+0	+1	+2	+3	
$000E80_H$	Reserved	Reserved	EPILR02 [R/W] 00000000	Reserved	R-bus Extra Port Input Level Select Register
$000E84_H$	Reserved	Reserved	Reserved	Reserved	
$000E88_H$	Reserved	Reserved	Reserved	Reserved	
$000E8C_H$	Reserved	Reserved	EPILR14 [R/W] 00000000	EPILR15 [R/W] - - - - 0000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - - - - - 000	Reserved	EPILR22 [R/W] - - 00 - 0 - 0	EPILR23 [R/W] - 0000000	
$000E98_H$	EPILR24 [R/W] 00000000	EPILR25 [R/W] 00000000	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] - - 00000	EPILR29 [R/W] 00000000	Reserved	Reserved	
$000EA0_H$ to $000EBC_H$	Reserved				Reserved
$000EC0_H$	Reserved	Reserved	PPER02 [R/W] 00000000	Reserved	R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	Reserved	Reserved	Reserved	
$000EC8_H$	Reserved	Reserved	Reserved	Reserved	
$000ECC_H$	Reserved	Reserved	PPER14 [R/W] 00000000	PPER15 [R/W] - - - - 0000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - - - - - 000	Reserved	PPER22 [R/W] - - 00 - 0 - 0	PPER23 [R/W] - 0000000	
$000ED8_H$	PPER24 [R/W] 00000000	PPER25 [R/W] 00000000	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] - - 00000	PPER29 [R/W] 00000000	Reserved	Reserved	
$000EE0_H$ to $000EFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ Flash-cache/ I-RAM Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - - 00000 00000000 00000000				Flash-cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - - 00000 00000000 00000000				
007014_H to 007FFCH	Reserved				Reserved
008000H to $00BFFC_H$	MB91F467Cx Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ MB91F465CA Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ MB91F463CA Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		Reserved		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ to $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		

12.2 Flash memory and external bus area

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+0	+1	+2	+3	+4	+5	+6	+7	
040000_H to $05FFF8_H$	SA8 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA9 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				ROMS0
060000_H to $07FFF8_H$	SA10 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA11 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				ROMS1
080000_H to $09FFF8_H$	SA12 (64KB, MB91F467Cx, MB91F465CA); Reserved (MB91F463CA)				SA13 (64KB, MB91F467Cx, MB91F465CA); Reserved (MB91F463CA)				ROMS2
$0A0000_H$ to $0BFFF8_H$	SA14 (64KB, MB91F467Cx, MB91F465CA); Reserved (MB91F463CA)				SA15 (64KB, MB91F467Cx, MB91F465CA); Reserved (MB91F463CA)				ROMS3
$0C0000_H$ to $0DFFF8_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
$0E0000_H$ to $0FFFF0_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
$0FFFF8_H$	FMV [R] 06 00 00 00H				FRV [R] 00 00 BF F8H				
100000_H to $11FFF8_H$	SA20 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA21 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				ROMS6
120000_H to $13FFF8_H$	SA22 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA23 (64KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				
140000_H to $143FF8_H$	SA0 (8KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA1 (8KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				ROMS7
144000_H to $17FF8_H$	SA2 (8KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				SA3 (8KB, MB91F467Cx); Reserved (MB91F465CA, MB91F463CA)				
148000_H to $14BFF8_H$	SA4 (8KB)				SA5 (8KB)				
$14C000_H$ to $14FFF8_H$	SA6 (8KB)				SA7 (8KB)				
150000_H to $17FFF8_H$	Reserved								

15.3 DC characteristics

Note: In the following tables, "V_{DD}" means $HV_{DD}5$ for SMC pins or $V_{DD}5$ for other pins.
In the following tables, "V_{SS}" means Hvss5 for ground Pins of the stepper motor and $V_{SS}5$ for the other pins.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$0.74 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$3\ V \le V_{DD} \le 4.5\ V$
		—	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
		—	Port inputs if TTL input is selected	2.0	—	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	—	$V_{DD} - 0.3$	—	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{DD}$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$V_{SS} - 0.3$	—	$0.46 \times V_{DD}$	V	$3\ V \le V_{DD} \le 4.5\ V$
		—	Port inputs if TTL input is selected	$V_{SS} - 0.3$	—	0.8	V	
	V_{ILR}	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	$V_{SS} - 0.3$	—	0.5	V	External clock in "Oscillation mode"

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5$ × 0.25	V	
Power supply current per ADC macro *3	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current per ADC macro *3	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*3 : The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation

$T_{samp} = (2.6\ kOhm + R_{EXT}) \cdot 11pF \cdot 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$

$T_{samp} = (12.1\ kOhm + R_{EXT}) \cdot 11pF \cdot 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

15.5 Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	− 1	—	+ 1	µA	T_A=25 °C
			− 3	—	+ 3	µA	T_A=105 °C
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ − 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ − 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparion time	t_{COMPF}		—	0.1	0.2	µA	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µA	Alarm comparator enabled in normal mode *1

Note: *1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.