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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

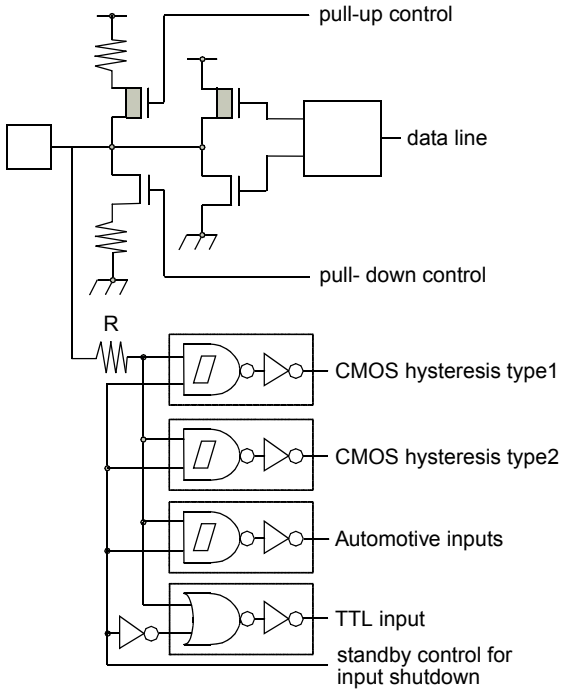
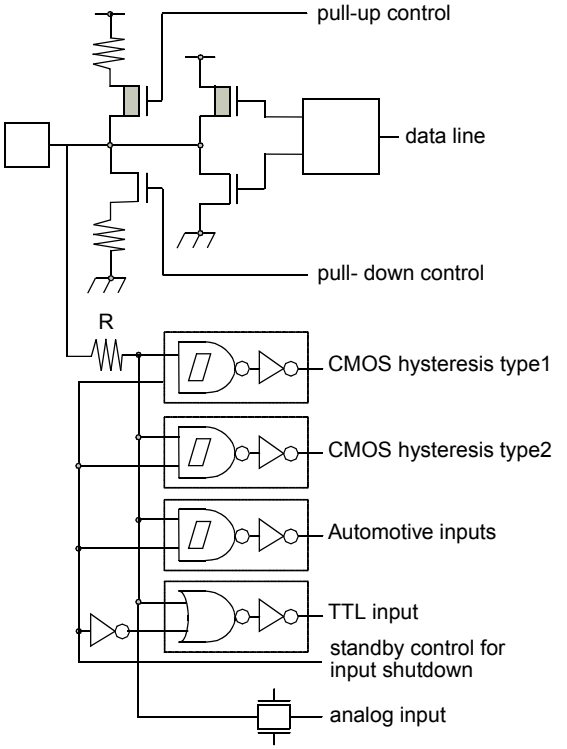
Applications of "Embedded - Microcontrollers"

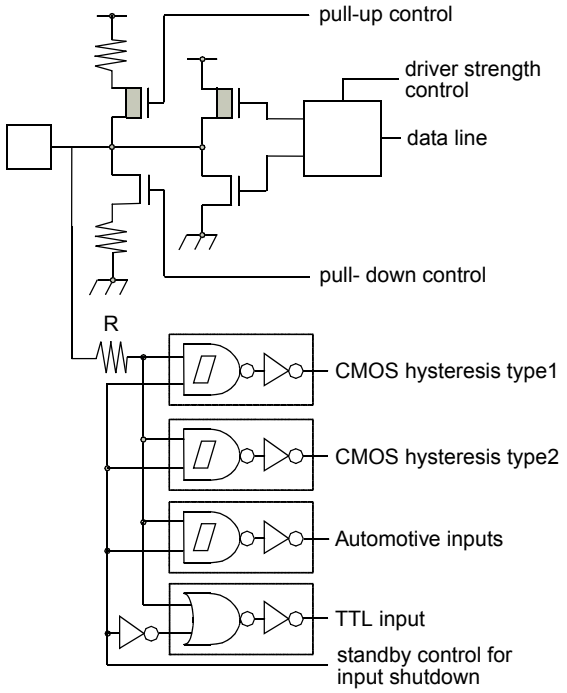
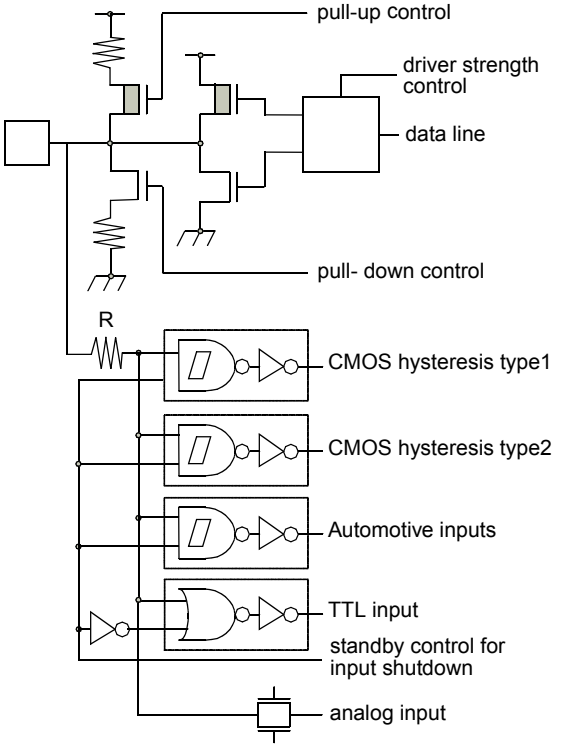
Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	104
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f465capmc-gsk5e2

3. Pin Description

3.1 MB91F463CA, MB91F465CA, MB91F467Cx

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 9	P02_0 to P02_7	I/O	A	General-purpose input/output ports
10 to 17	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins of reload timer
	TTG8/0 to TTG15/7			External trigger input pins of PPG timer
20 to 23	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
24 to 27	P17_4 to P17_7	I/O	A	General-purpose input/output ports
	PPG4 to PPG7			Output pins of PPG timer
28 to 31	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
32	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
33	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
34	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
	PFM			Pulse frequency modulator output pin
35	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

5.2 Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power supply pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

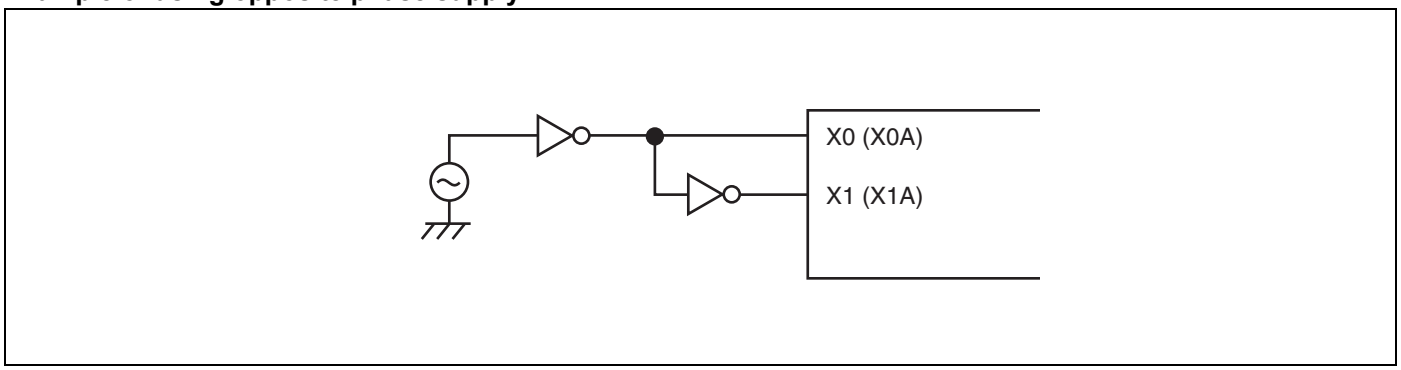
5.4 Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

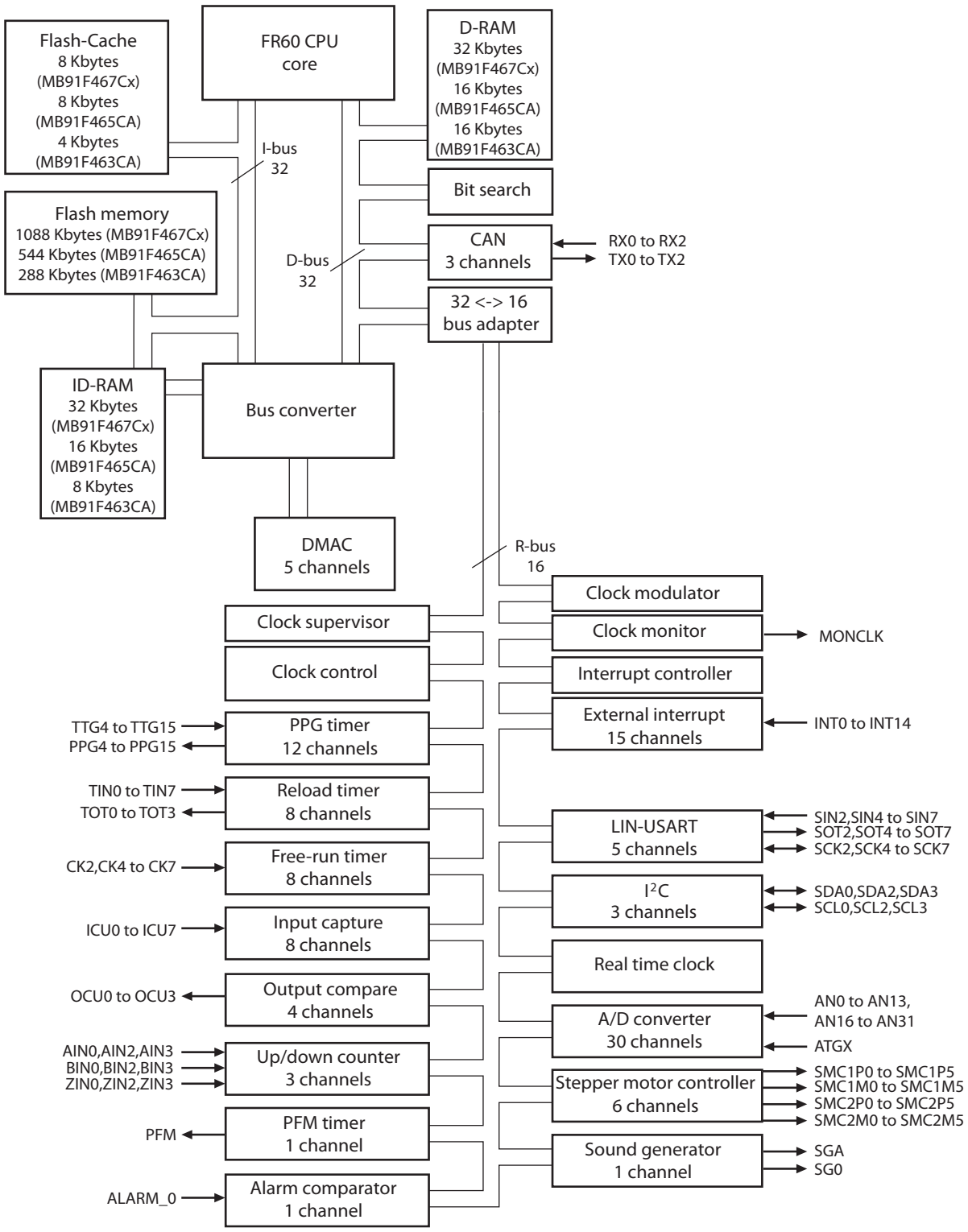
Example of using opposite phase supply



(Continued)

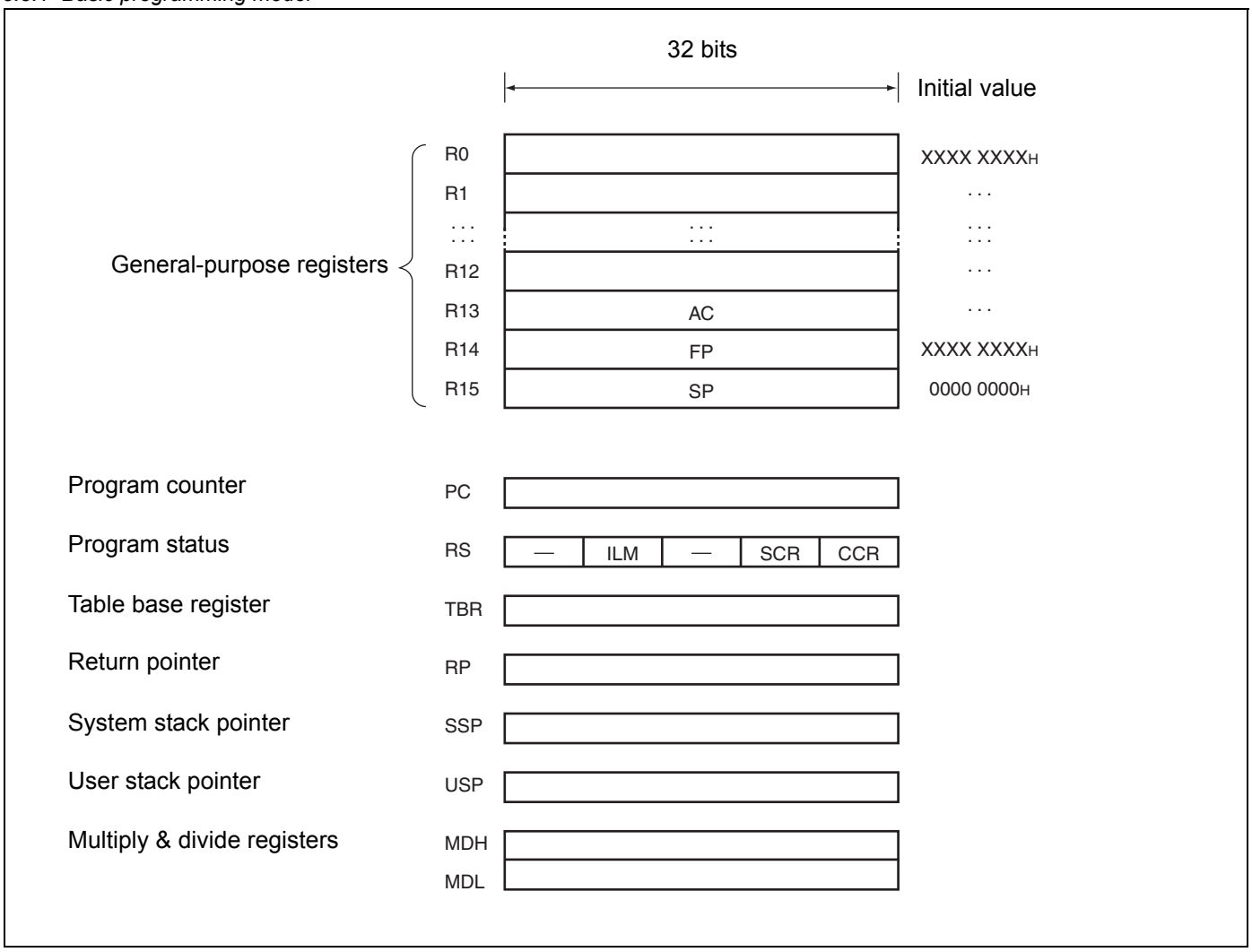
7. Block Diagram

7.1 MB91F463CA, MB91F465CA, MB91F467Cx



8.3 Programming model

8.3.1 Basic programming model



9.3 Flash access in CPU mode

9.3.1 Flash configuration

Flash memory map MB91F467Cx

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

9.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F465CA, MB91F467Cx external pins			Comment
		Flash memory mode	Normal function	Pin number	
—	INITX	—	INITX	84	
RESET	—	FRSTX	NMIX	85	
—	—	MD_2	MD_2	76	Set to ‘1’
—	—	MD_1	MD_1	75	Set to ‘1’
—	—	MD_0	MD_0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP28_0	100	
BYTE	Internally fixed to ‘H’	BYTEX	GP28_2	102	
WE	Internal control signal + control via interface circuit	WEX	GP28_5	111	
OE		OEX	GP28_4	110	
CE		CEX	GP20_0	38	
—		ATDIN	GP17_7	27	Set to ‘0’
—		EQIN	GP17_6	26	Set to ‘0’
—		TESTX	GP28_3	103	Set to ‘1’
—		RDYI	GP28_1	101	Set to ‘0’
A-1	Internal address bus	FA0	GP17_5	25	Set to ‘0’
A0 to A3		FA1 to FA4	GP29_0 to GP29_3	92 to 95	
A4 to A7		FA5 to FA8	GP29_4 to GP29_7	96 to 99	
A8 to A11		FA9 to FA12	GP16_0 to GP16_3	28 to 31	
A12 to A15		FA13 to FA16	GP16_4 to GP16_7	32 to 35	
A16 to A18		FA17 to FA19	GP15_0 to GP15_2	20 to 22	
A19		FA20	GP15_3	23	Set to ‘1’ on MB91F463CA, MB91F465CA
—		FA21	GP17_4	24	Set to ‘1’
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP14_0 to GP14_7	10 to 17	
DQ8 to DQ15		DQ8 to DQ15	GP02_0 to GP02_7	2 to 9	

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

Address	Register				Block
	+0	+1	+2	+3	
$000D00_H$	Reserved	Reserved	PDRD02 [R] XXXXXXXX	Reserved	R-bus Port Data Direct Read Register
$000D04_H$	Reserved	Reserved	Reserved	Reserved	
$000D08_H$	Reserved	Reserved	Reserved	Reserved	
$000D0C_H$	Reserved	Reserved	PDRD14 [R] XXXXXXXX	PDRD15 [R] - - - - XXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXX - - - -	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - - - - - XXX	Reserved	PDRD22 [R] - - XX - X - X	PDRD23 [R] - XXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	PDRD25 [R] XXXXXXXX	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] - - XXXXX	PDRD29 [R] XXXXXXXX	Reserved	Reserved	
$000D20_H$ to $000D3C_H$	Reserved				Reserved
$000D40_H$	Reserved	Reserved	DDR02 [R/W] 00000000	Reserved	R-bus Port Direction Register
$000D44_H$	Reserved	Reserved	Reserved	Reserved	
$000D48_H$	Reserved	Reserved	Reserved	Reserved	
$000D4C_H$	Reserved	Reserved	DDR14 [R/W] 00000000	DDR15 [R/W] - - - - 0000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 0000 - - - -	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - - - - - 000	Reserved	DDR22 [R/W] - - 00 - 0 - 0	DDR23 [R/W] - 0000000	
$000D58_H$	DDR24 [R/W] 00000000	DDR25 [R/W] 00000000	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] - - 00000	DDR29 [R/W] 00000000	Reserved	Reserved	
$000D60_H$ to $000D7C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000E80_H$	Reserved	Reserved	EPILR02 [R/W] 00000000	Reserved	R-bus Extra Port Input Level Select Register
$000E84_H$	Reserved	Reserved	Reserved	Reserved	
$000E88_H$	Reserved	Reserved	Reserved	Reserved	
$000E8C_H$	Reserved	Reserved	EPILR14 [R/W] 00000000	EPILR15 [R/W] - - - - 0000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - - - - - 000	Reserved	EPILR22 [R/W] - - 00 - 0 - 0	EPILR23 [R/W] - 0000000	
$000E98_H$	EPILR24 [R/W] 00000000	EPILR25 [R/W] 00000000	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] - - 00000	EPILR29 [R/W] 00000000	Reserved	Reserved	
$000EA0_H$ to $000EBC_H$	Reserved				Reserved
$000EC0_H$	Reserved	Reserved	PPER02 [R/W] 00000000	Reserved	R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	Reserved	Reserved	Reserved	
$000EC8_H$	Reserved	Reserved	Reserved	Reserved	
$000ECC_H$	Reserved	Reserved	PPER14 [R/W] 00000000	PPER15 [R/W] - - - - 0000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - - - - - 000	Reserved	PPER22 [R/W] - - 00 - 0 - 0	PPER23 [R/W] - 0000000	
$000ED8_H$	PPER24 [R/W] 00000000	PPER25 [R/W] 00000000	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] - - 00000	PPER29 [R/W] 00000000	Reserved	Reserved	
$000EE0_H$ to $000EFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00C038_H$ to $00C03C_H$	Reserved				
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ to $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved				
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				Reserved

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
CPU supervisor mode (INT #5 instruction) *6	5	05	-	-	0x3E8	0x000FFFE8	
Memory Protection exception *6	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap *5	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap *5	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction *5	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break exception *5	10	0A	-	-	0x3D4	0x000FFFD4	
Operand break trap *5	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap *5	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt (tool)*5	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction exception	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	0, 16
External Interrupt 1	17	11			0x3B8	0x000FFFB8	1, 17
External Interrupt 2	18	12	ICR01	0x441	0x3B4	0x000FFFB4	2, 18
External Interrupt 3	19	13			0x3B0	0x000FFFB0	3, 19
External Interrupt 4	20	14	ICR02	0x442	0x3AC	0x000FFFAC	20
External Interrupt 5	21	15			0x3A8	0x000FFFA8	21
External Interrupt 6	22	16	ICR03	0x443	0x3A4	0x000FFFA4	22
External Interrupt 7	23	17			0x3A0	0x000FFFA0	23
External Interrupt 8	24	18	ICR04	0x444	0x39C	0x000FFF9C	
External Interrupt 9	25	19			0x398	0x000FFF98	
External Interrupt 10	26	1A	ICR05	0x445	0x394	0x000FFF94	
External Interrupt 11	27	1B			0x390	0x000FFF90	
External Interrupt 12	28	1C	ICR06	0x446	0x38C	0x000FFF8C	
External Interrupt 13	29	1D			0x388	0x000FFF88	

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
USART (LIN, FIFO) 4 RX	66	42	ICR25	0x459	0x2F4	0x000FFEF4	10, 56
USART (LIN, FIFO) 4 TX	67	43			0x2F0	0x000FFEF0	11, 57
USART (LIN, FIFO) 5 RX	68	44	ICR26	0x45A	0x2EC	0x000FFEEC	12, 58
USART (LIN, FIFO) 5 TX	69	45			0x2E8	0x000FFEE8	13, 59
USART (LIN, FIFO) 6 RX	70	46	ICR27	0x45B	0x2E4	0x000FFEE4	60
USART (LIN, FIFO) 6 TX	71	47			0x2E0	0x000FFEE0	61
USART (LIN, FIFO) 7 RX	72	48	ICR28	0x45C	0x2DC	0x000FFEDC	62
USART (LIN, FIFO) 7 TX	73	49			0x2D8	0x000FFED8	63
I^2C 0 / I^2C 2	74	4A	ICR29	0x45D	0x2D4	0x000FFED4	
I^2C 3	75	4B			0x2D0	0x000FFED0	
Reserved	76	4C	ICR30	0x45E	0x2CC	0x000FFECC	64
Reserved	77	4D			0x2C8	0x000FFEC8	65
Reserved	78	4E	ICR31	0x45F	0x2C4	0x000FFEC4	66
Reserved	79	4F			0x2C0	0x000FFEC0	67
Reserved	80	50	ICR32	0x460	0x2BC	0x000FFEBC	68
Reserved	81	51			0x2B8	0x000FFEB8	69
Reserved	82	52	ICR33	0x461	0x2B4	0x000FFEB4	70
Reserved	83	53			0x2B0	0x000FFEB0	71
Reserved	84	54	ICR34	0x462	0x2AC	0x000FFEAC	72
Reserved	85	55			0x2A8	0x000FFEA8	73
Reserved	86	56	ICR35	0x463	0x2A4	0x000FFEA4	74
Reserved	87	57			0x2A0	0x000FFEA0	75
Reserved	88	58	ICR36	0x464	0x29C	0x000FFE9C	76
Reserved	89	59			0x298	0x000FFE98	77
Reserved	90	5A	ICR37	0x465	0x294	0x000FFE94	78
Reserved	91	5B			0x290	0x000FFE90	79
Input Capture 0	92	5C	ICR38	0x466	0x28C	0x000FFE8C	80
Input Capture 1	93	5D			0x288	0x000FFE88	81
Input Capture 2	94	5E	ICR39	0x467	0x284	0x000FFE84	82
Input Capture 3	95	5F			0x280	0x000FFE80	83
Input Capture 4	96	60	ICR40	0x468	0x27C	0x000FFE7C	84
Input Capture 5	97	61			0x278	0x000FFE78	85
Input Capture 6	98	62	ICR41	0x469	0x274	0x000FFE74	86
Input Capture 7	99	63			0x270	0x000FFE70	87
Output Compare 0	100	64	ICR42	0x46A	0x26C	0x000FFE6C	88
Output Compare 1	101	65			0x268	0x000FFE68	89

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -2mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -1.6mA$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -5mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -3mA$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OH} = -3mA$	$V_{DD} - 0.5$	—	—	V	
	V_{OH30}	High current outputs	$4.5V \le V_{DD} \le 5.5V$, T_A = -40°C, I_{OH} = -40mA $4.5V \le V_{DD} \le 5.5V$, I_{OH} = -30mA $3.0V \le V_{DD} \le 4.5V$, I_{OH} = -20mA	$V_{DD} - 0.5$			V	Driving strength set to 30mA
Output “L” voltage	V_{OL2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = +2mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = +1.6mA$	—	—	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = +5mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = +3mA$	—	—	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OH} = +3mA$	—	—	0.4	V	
	V_{OL30}	High current outputs	$4.5V \le V_{DD} \le 5.5V$, T_A = -40°C, I_{OH} = +40mA $4.5V \le V_{DD} \le 5.5V$, I_{OH} = +30mA $3.0V \le V_{DD} \le 4.5V$, I_{OH} = +20mA			0.5	V	Driving strength set to 30mA
Input leakage current	I_{IL}	Pnn_m *1	$3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	-1	—	$+1$	µA	
			$3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=105 °C	-3	—	$+3$		

15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
- - IO_{drive} = 5 mA
- - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- - $V_{SS}5$ = 0 V
- - T_a = -40°C to +105°C
- - C_l = 50 pF (load capacity value of pins when testing)
- - VOL = 0.2 x $V_{DD}5$
- - VOH = 0.8 x $V_{DD}5$
- - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5 = 3.0$ V to 4.5 V		$V_{DD}5 = 4.5$ V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		− 30	30	− 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} − 30*	—	m × t_{CLKP} − 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

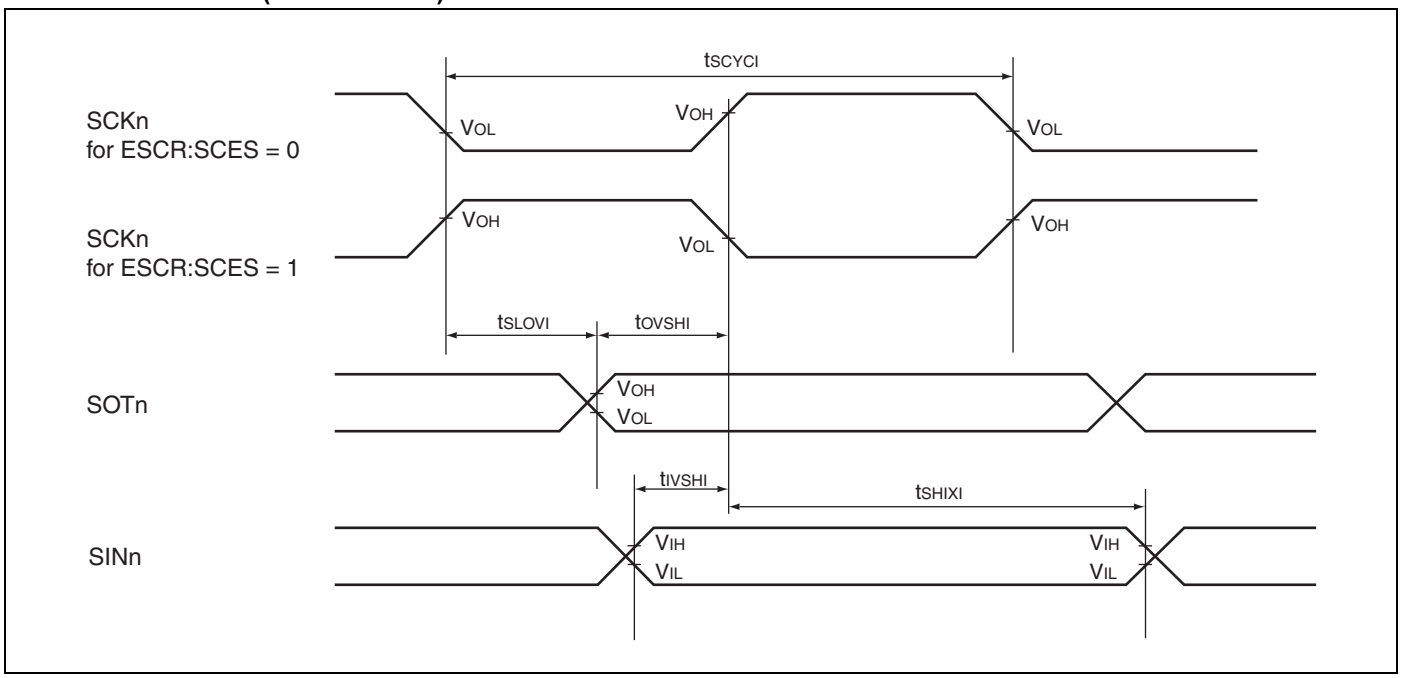
* : Parameter m depends on t_{SCYCI} and can be calculated as :

- if $t_{SCYCI} = 2*k*t_{CLKP}$, then m = k, where k is an integer > 2
- if $t_{SCYCI} = (2*k + 1)*t_{CLKP}$, then m = k + 1, where k is an integer > 1

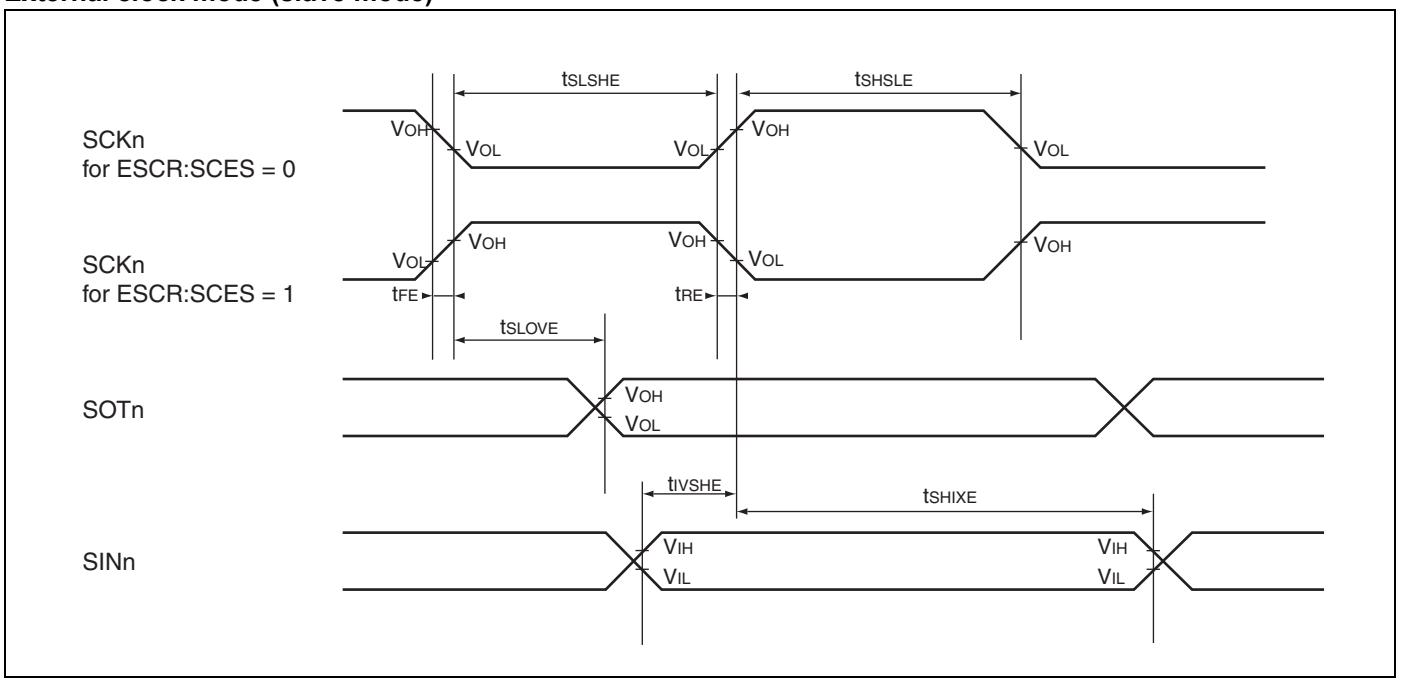
Notes :

- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

Internal clock mode (master mode)



External clock mode (slave mode)



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