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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104acasp-v0

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G14			
			30 pins	32 pins	36 pins	40 pins
192 KB	8 KB	20 KB	—	—	—	R5F104EH
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA

Flash ROM	Data flash	RAM	RL78/G14			
			44 pins	48 pins	52 pins	64 pins
512 KB	8 KB	48 KB Note	—	R5F104GL	—	R5F104LL
384 KB	8 KB	32 KB	—	R5F104GK	—	R5F104LK
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	—	—

Flash ROM	Data flash	RAM	RL78/G14	
			80 pins	100 pins
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL
384 KB	8 KB	32 KB	R5F104MK	R5F104PK
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

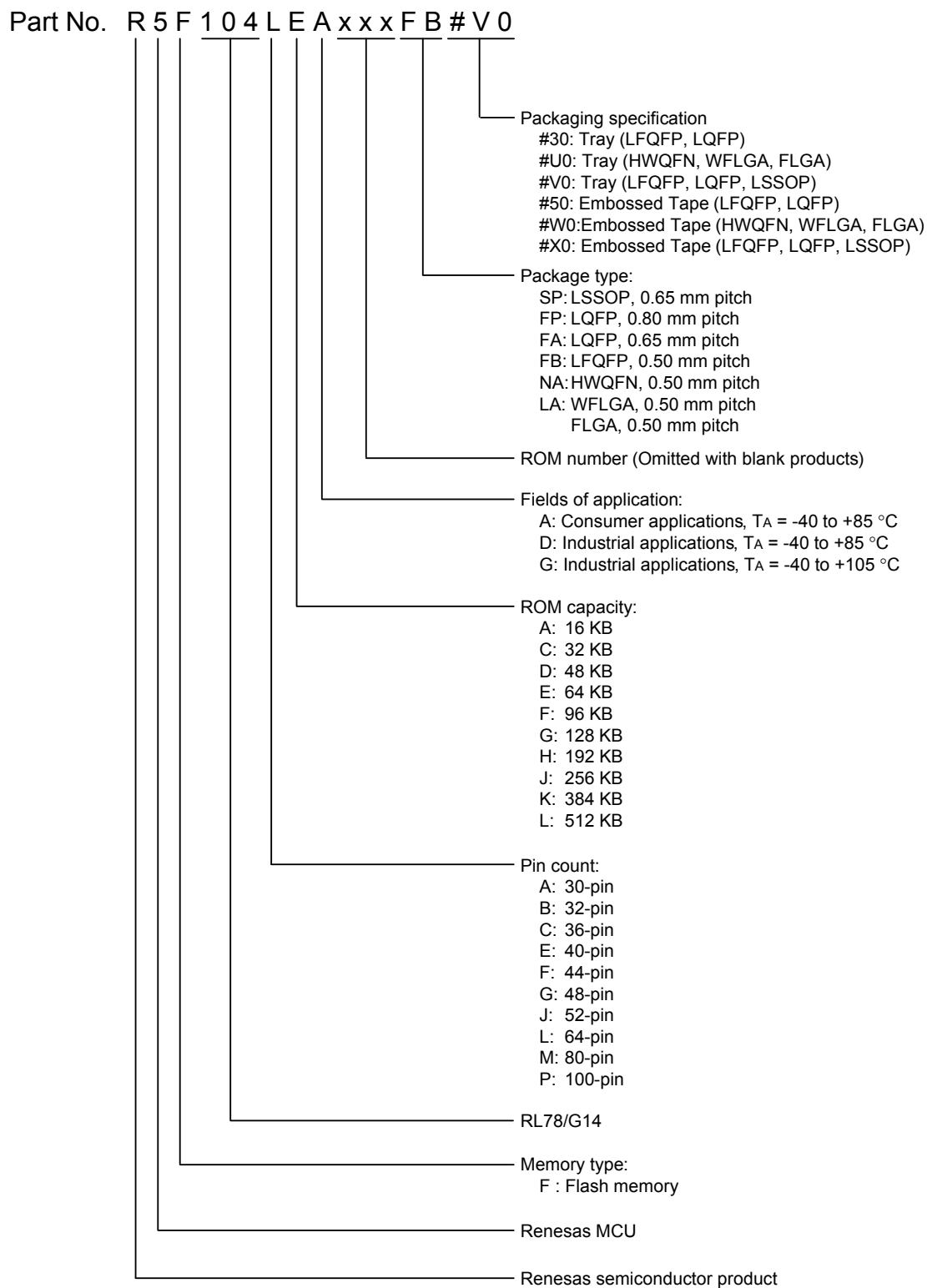
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

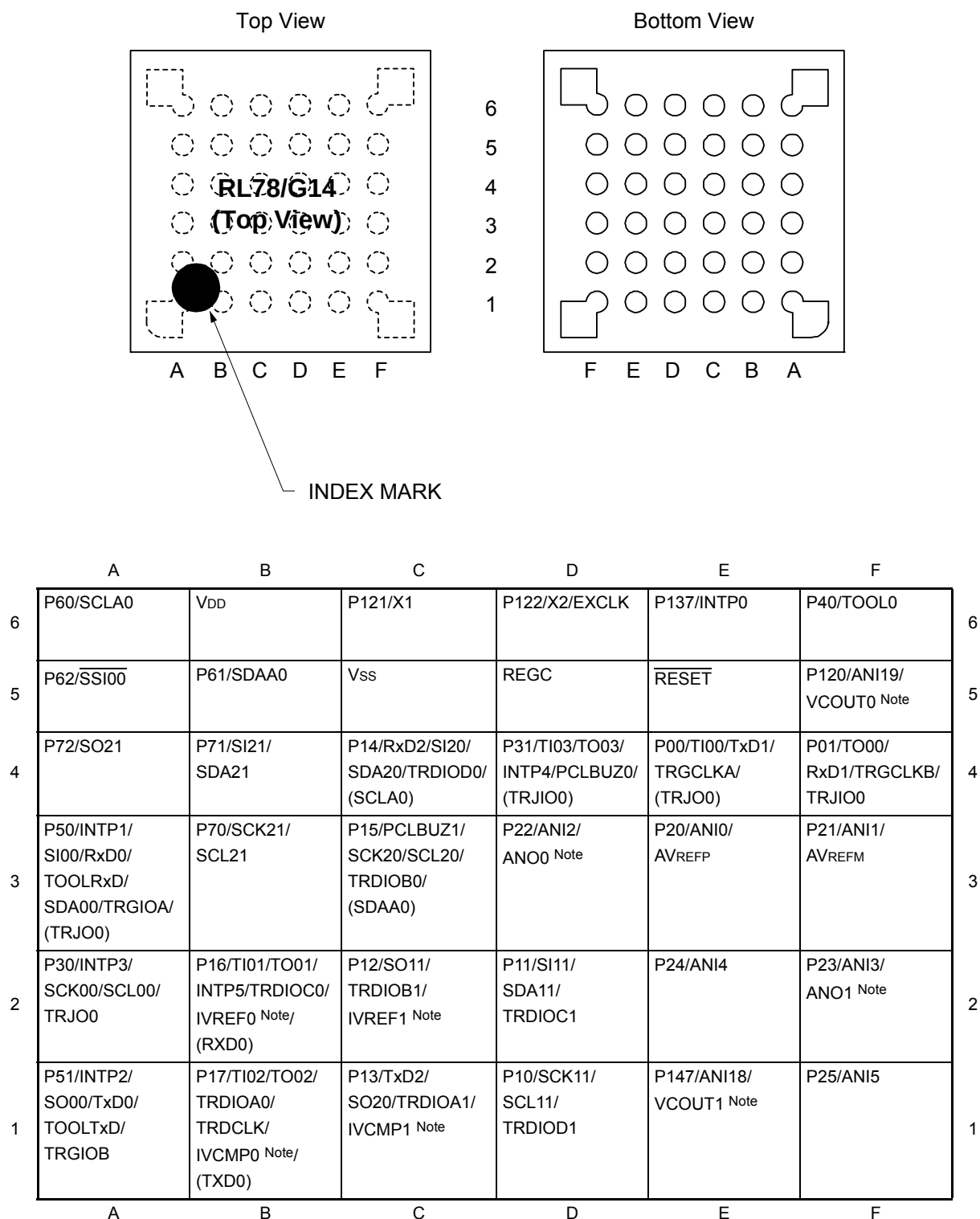
1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14



1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



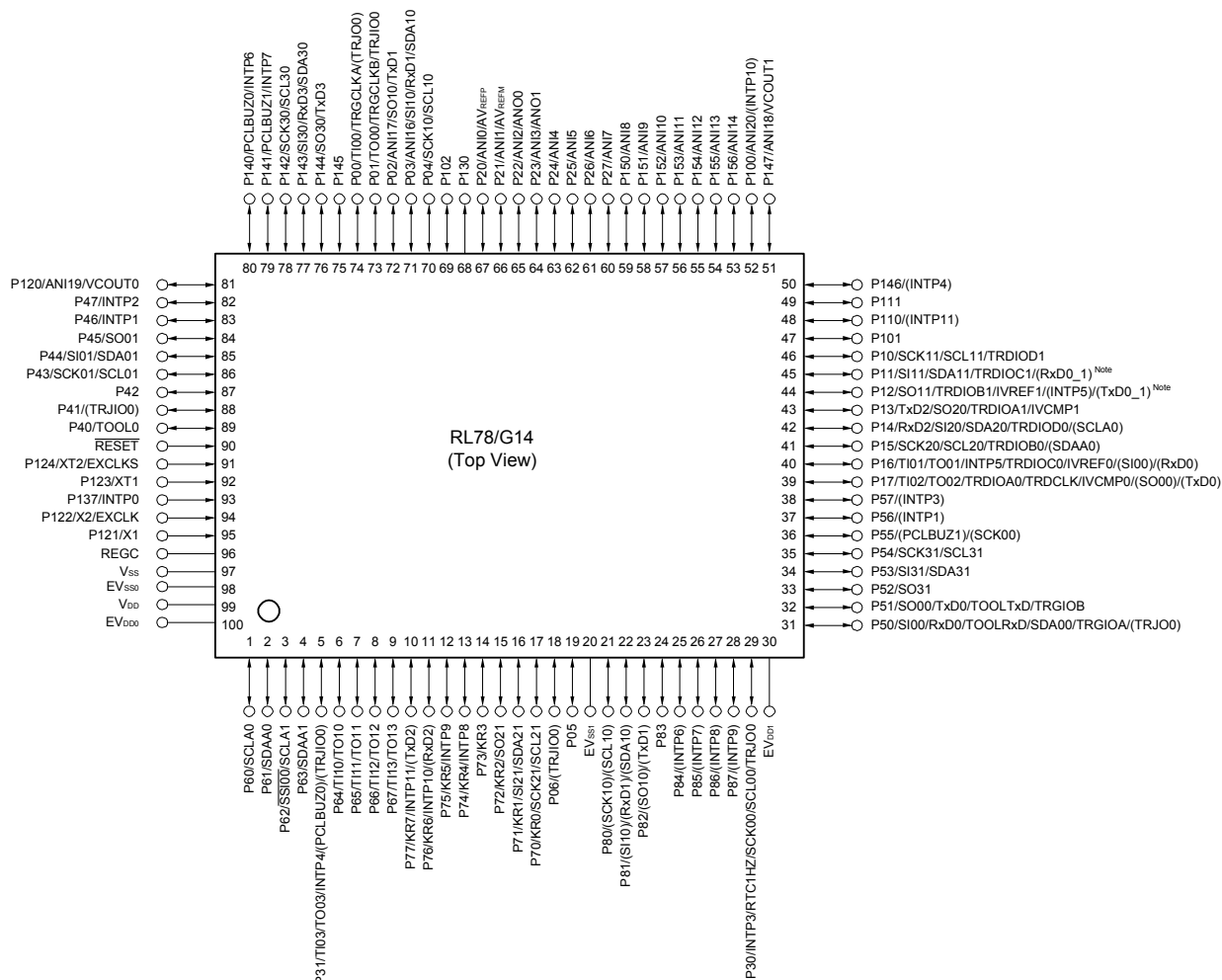
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0, EVss1 pins the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Code flash memory (KB)		96 to 128	96 to 128	96 to 128	96 to 192
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 16 Note	12 to 16 Note	12 to 16 Note	12 to 20 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)			
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)			
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)			
		—			30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits $\times$ 8 bits, 16 bits $\times$ 16 bits), Division (16 bits $\div$ 16 bits, 32 bits $\div$ 32 bits) • Multiplication and Accumulation (16 bits $\times$ 16 bits $\div$ 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)

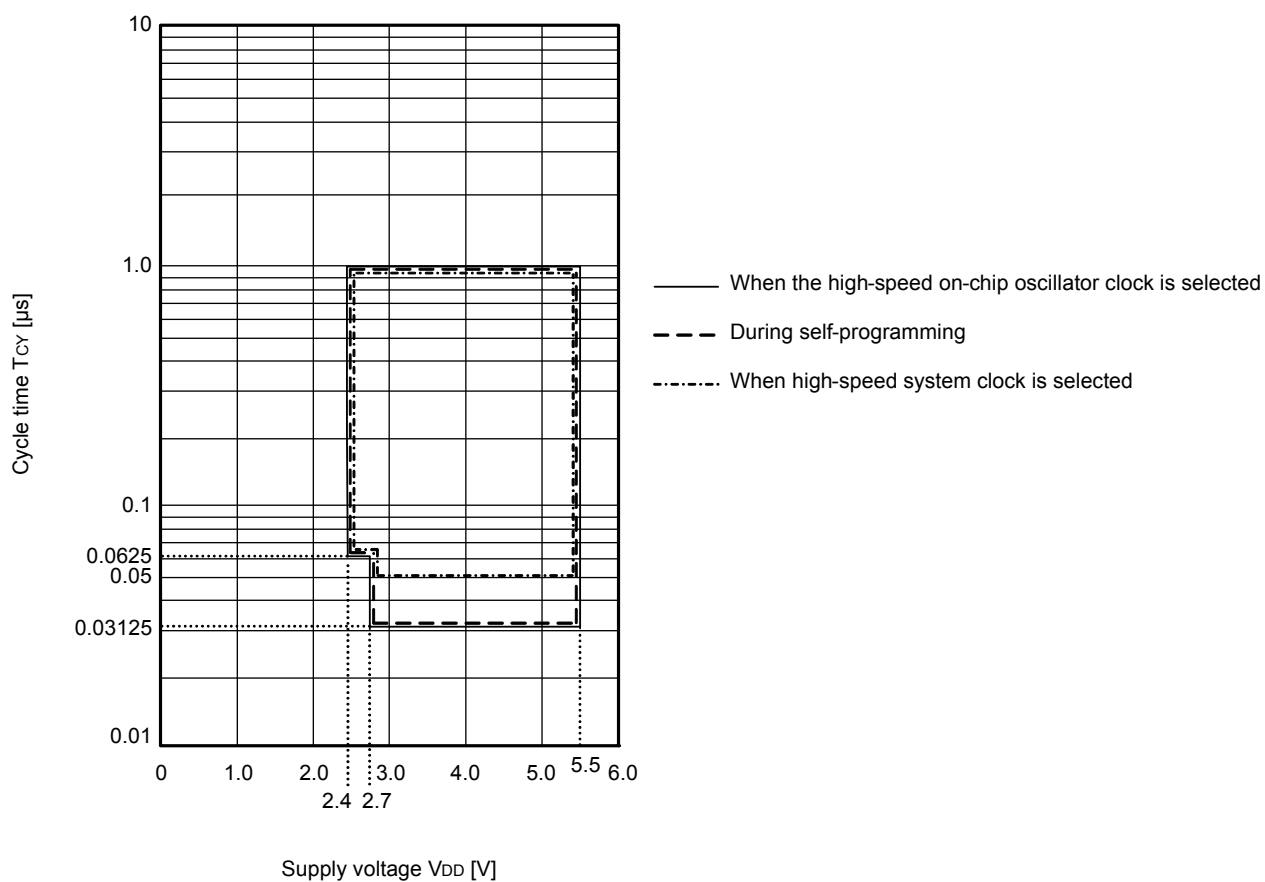
(Note is listed on the next page.)

(4) Peripheral Functions (Common to all products)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

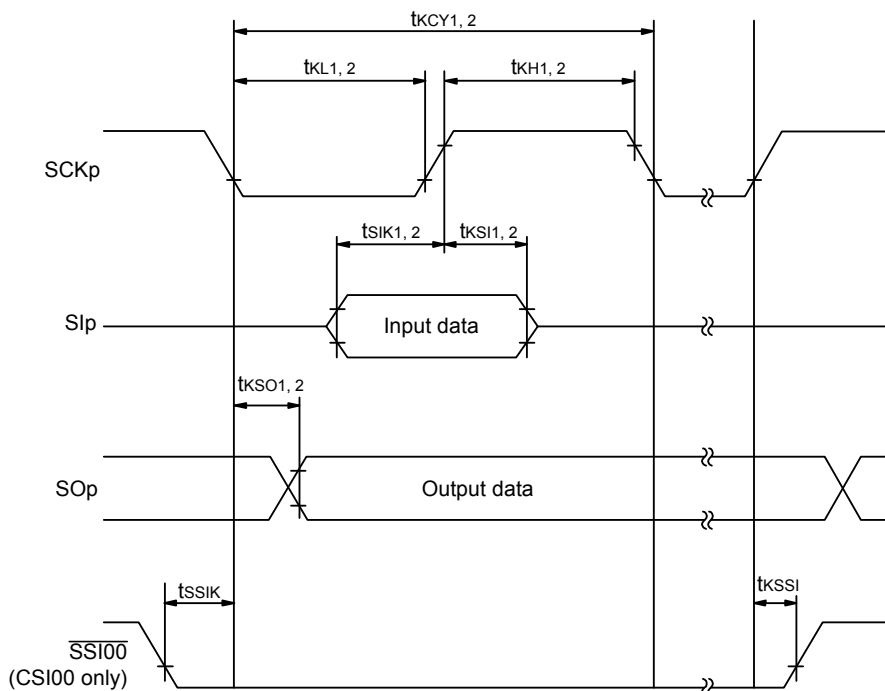
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fIL = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	
		DTC operation			3.10		

Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

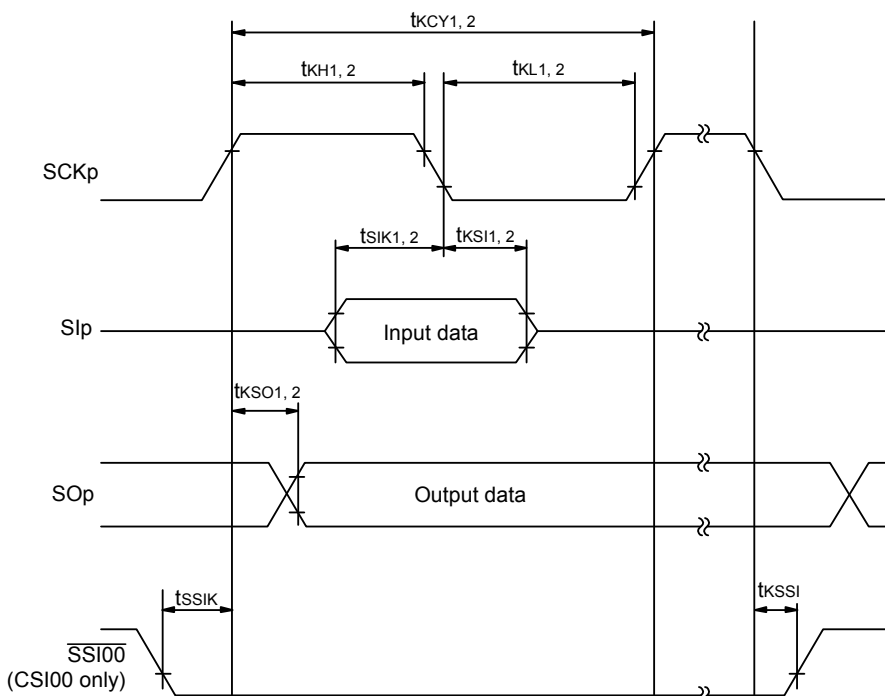
Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

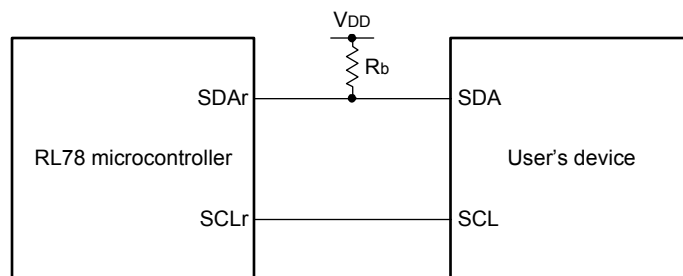
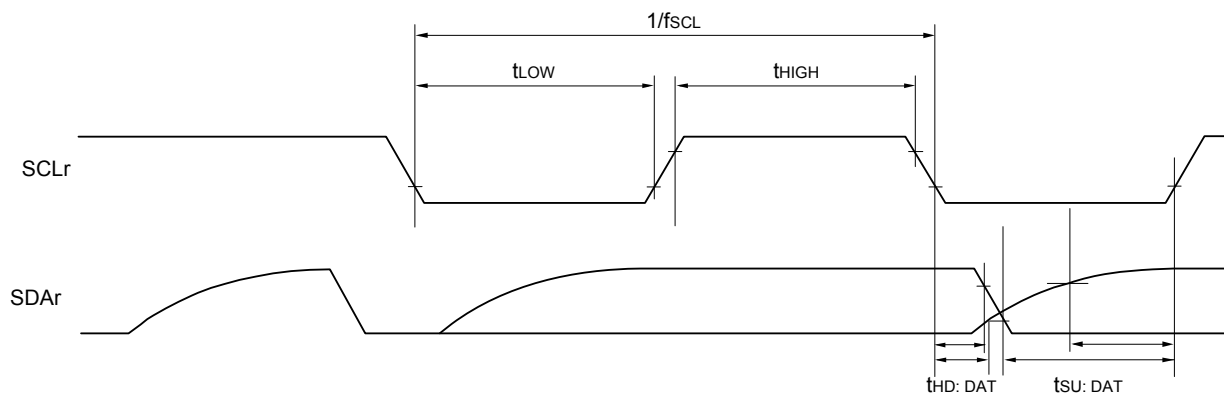


CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

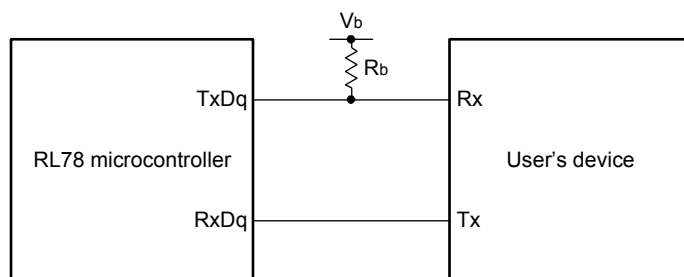
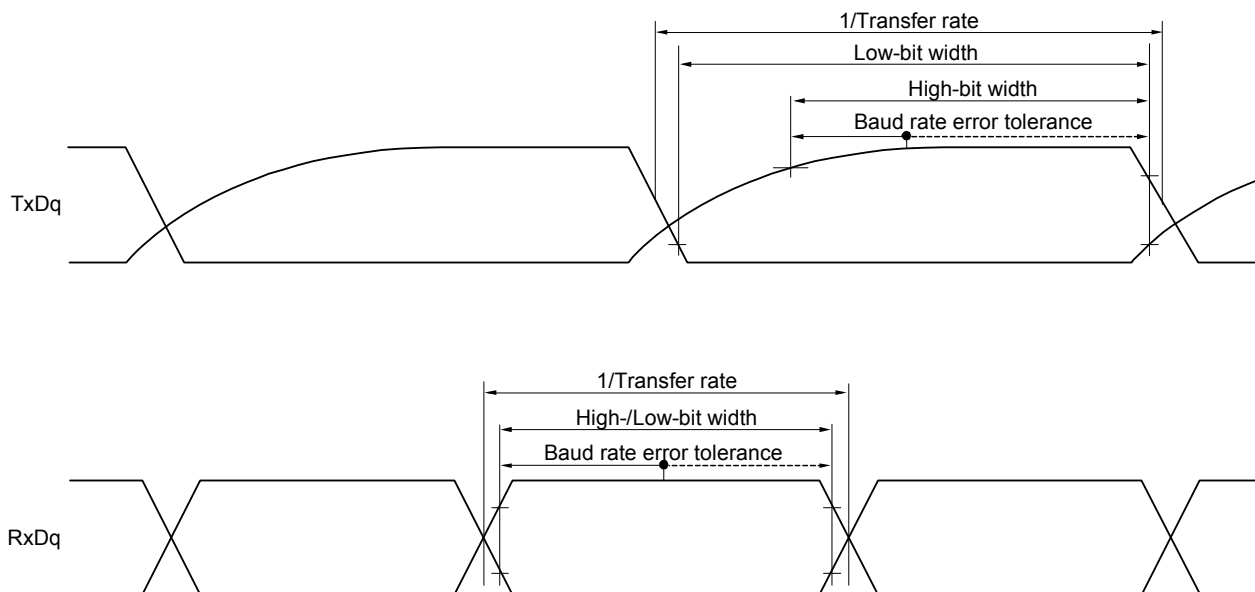
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,

C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} \leq EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		5			μs

2.6.3 D/A converter characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVSS0 = EVSS1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 5.5 V			3	μs
			1.6 V ≤ VDD < 2.7 V			6	μs

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			80.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	$2\text{ MHz} < f_{\text{CLK}} \leq 32\text{ MHz}$	1			μs
			$f_{\text{CLK}} \leq 2\text{ MHz}$	$1/f_{\text{CLK}} + 1$			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		$2.5/f_{\text{CLK}}$			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	1			μs
		INTP1 to INTP11	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250			ns
$\overline{\text{RESET}}$ low-level width	tRSL			10			μs

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	16/fMCK		ns
			fMCK ≤ 20 MHz	12/fMCK		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	16/fMCK		ns
			fMCK ≤ 16 MHz	12/fMCK		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		12/fMCK and 1000		ns
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 14		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 16		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 36		ns
Slp setup time (to SCKp↑) Note 1	tSIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 40		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 60		ns
Slp hold time (from SCKp↑) Note 2	tSIH2			1/fMCK + 62		ns
Delay time from SCKp↓ to SOp output Note 3	tKS02	C = 30 pF Note 4	2.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 66	ns
			2.4 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

Note 5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq E_{VDD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ E_{VDD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(1/2)**

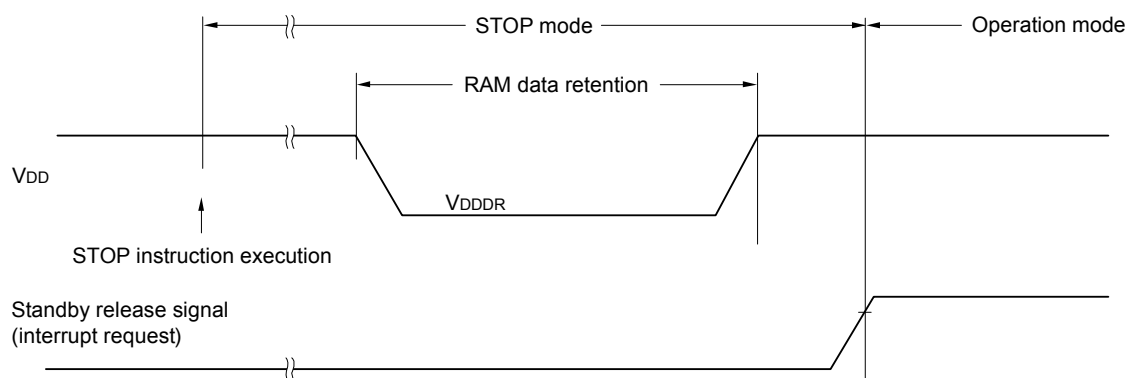
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		400 Note 1	kHz
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		400 Note 1	kHz
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$		100 Note 1	kHz
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		100 Note 1	kHz
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	1200		ns
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$	4600		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	4650		ns
Hold time when SCLr = "H"	t _{HIGH}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	620		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	500		ns
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$	2700		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	1830		ns

3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ Note 4	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

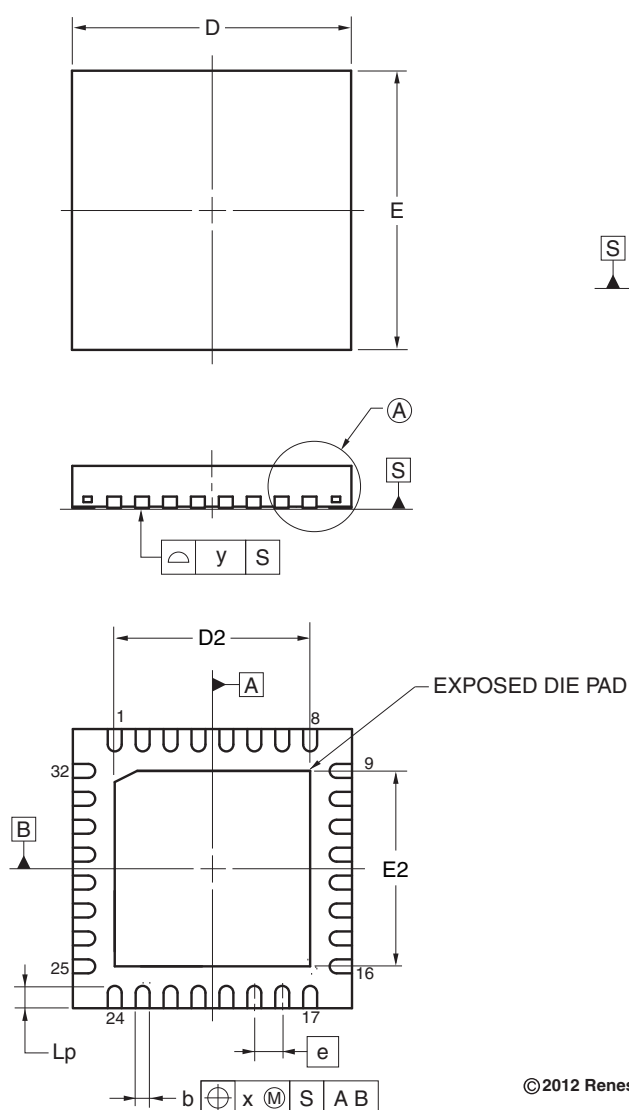
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.2 32-pin products

R5F104BAANA, R5F104BCANA, R5F104BDANA, R5F104BEANA, R5F104BFANA, R5F104BGANA
 R5F104BADNA, R5F104BCDNA, R5F104BDDNA, R5F104BEDNA, R5F104BFDNA, R5F104BGDNA
 R5F104BAGNA, R5F104BCGNA, R5F104BDGNA, R5F104BEGNA, R5F104BFGNA, R5F104BGGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-4	0.06



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

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R5F104PKAFB, R5F104PLAFB
R5F104PKGFB, R5F104PLGFB

