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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Obsolete
RL78
16-Bit
32MHz
CSI, I ² C, LINbus, UART/USART
DMA, LVD, POR, PWM, WDT
22
32KB (32K x 8)
FLASH
4K x 8
4K x 8
1.6V ~ 5.5V
A/D 8x8/10b
Internal
-40°C ~ 85°C (TA)
Surface Mount
32-LQFP
32-LQFP (7x7)
https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104bcafp-x0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

○ ROM, RAM capacities

Elash ROM	Data flach	PAM	RL78/G14					
T IdSIT KOW	Data liasii		30 pins	32 pins	36 pins	40 pins		
192 KB	8 KB	20 KB	—	—	—	R5F104EH		
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG		
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF		
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE		
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED		
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC		
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA		

Elash ROM	Data flach	PAM		RL78	8/G14	
T Idolf TOW	Data liasii		44 pins	48 pins	52 pins	64 pins
512 KB	8 KB	48 KB Note		R5F104GL	—	R5F104LL
384 KB	8 KB	32 KB	_	R5F104GK	—	R5F104LK
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	_	

Elach DOM	Data flach	DAM	RL78	3/G14
T IdSIT KOW	Data hash		80 pins	100 pins
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL
384 KB	8 KB	32 KB	R5F104MK	R5F104PK
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).



1.5.9 80-pin products





- Note 1. Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 Note 2. During HALT instruction execution by flash memory.
- Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 4.** When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 32 MHz
 - 2.4 V \leq VDD \leq 5.5 V@1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 8 MHz
 - LV (low-voltage main) mode: $1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}_{\textcircled{O}}1 \text{ MHz}$ to 4 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remark 3.** file: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



2.4 AC Characteristics

Items	Symbol		Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (min-	Тсү	Main system	HS (high-speed main)	$2.7~V \leq V_{DD} \leq 5.5~V$	0.03125		1	μs
imum instruction exe-		clock (fMAIN)	mode	$2.4 \text{ V} \leq \text{V}_{DD} < 2.7 \text{ V}$	0.0625		1	μs
cution time)		operation	LS (low-speed main) mode	$1.8 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$	0.125		1	μs
			LV (low-voltage main) mode	$1.6~V \le V_{DD} \le 5.5~V$	0.25		1	μs
		Subsystem clock (fsub) operation		$1.8~V \le V_{DD} \le 5.5~V$	28.5	30.5	31.3	μs
		In the self-	HS (high-speed main)	$2.7~V \leq V \text{DD} \leq 5.5~V$	0.03125		1	μs
		program-	mode	$2.4 \text{ V} \leq \text{V}_{DD} < 2.7 \text{ V}$	0.0625		1	μs
		ming mode	LS (low-speed main) mode	$1.8 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V}$	0.125		1	μs
			LV (low-voltage main) mode	$1.8 \text{ V} \leq \text{V}\text{DD} \leq 5.5 \text{ V}$	0.25		1	μs
External system clock	fEX	$2.7~V \leq V_{DD} \leq$	5.5 V		1.0		20.0	MHz
frequency		$2.4~V \leq V_{DD} \leq$	2.7 V		1.0		16.0	MHz
		$1.8 \text{ V} \le \text{V}_{\text{DD}}$ <	2.4 V		1.0		8.0	MHz
		$1.6 \text{ V} \leq \text{V}_{\text{DD}}$ <	1.8 V		1.0		4.0	MHz
	fexs				32		35	kHz
External system clock	texн,	$2.7~V \leq V \text{DD} \leq$	5.5 V		24			ns
input high-level width,	texL	$2.4~V \leq V \text{DD} \leq$	2.7 V		30			ns
IOW-IEVEI WIQ[I]		$1.8 \text{ V} \leq \text{Vdd} <$	2.4 V		60			ns
		$1.6 \text{ V} \leq \text{V}_{\text{DD}}$ <	1.8 V		120			ns
	texhs, texls				13.7			μs
TI00 to TI03, TI10 to TI13 input high-level width, low-level width	ttiH, tti∟				1/fмск + 10 Note			ns
Timer RJ input cycle	fc	TRJIO		$2.7~V \leq EV_{DD0} \leq 5.5~V$	100			ns
				$1.8 \text{ V} \le \text{EV}_{\text{DD0}} \le 2.7 \text{ V}$	300			ns
				$1.6 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V}$	500			ns
Timer RJ input high-	tтjiн,	TRJIO		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	40			ns
level width, low-level	t⊤JIL			$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V}$	120			ns
				$1.6 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V}$	200			ns

(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

NoteThe following conditions are required for low voltage interface when EVDD0 < VDD $1.8 V \le EVDD0 < 2.7 V$: MIN. 125 ns $1.6 V \le EVDD0 < 1.8 V$: MIN. 250 ns

Remark fMCK: Timer array unit operation clock frequency (Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))







- **Note 4.** This value as an example is calculated when the conditions described in the "Conditions" column are met.
- Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Note 5. Use it with $EV_{DD0} \ge V_b$.
- **Note 6.** The smaller maximum transfer rate derived by using fMck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V \leq EVDD0 < 3.3 V and 1.6 V \leq Vb \leq 2.0 V

Maximum transfer rate

sfer rate =
$$\frac{}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$

1

Baud rate error (theoretical value) =

$$\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 100 [\%]$$

$$(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

- **Note 7.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.
- Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)



RL78/G14

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

Parameter	Symbol	Conditions		HS (high-s main) mo	HS (high-speed L main) mode		LS (low-speed main) mode		LV (low-voltage main) mode	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tксү1	tксү1 ≥ 2/fc∟к	$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 20 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$	200		1150		1150		ns
			$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_{b} \leq 2.7 \; V, \\ C_{b} = 20 \; pF, \; R_{b} = 2.7 \; k\Omega \end{array}$	300		1150		1150		ns
SCKp high-level width	tкнı	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 20 \ pF, \ R_b = 1.4 \ k\Omega \\ \hline 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq EV_{DD0} < 4.0 \ V, \\ C_b = 20 \ pF, \ R_b = 2.7 \ V, \\ C_b = 20 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		tkcy1/2 - 50		tkcy1/2 - 50		tkcy1/2 - 50		ns
				tксү1/2 - 120		tксү1/2 - 120		tксү1/2 - 120		ns
SCKp low-level width	tĸ∟ı			tксү1/2 - 7		tксү1/2 - 50		tkcy1/2 - 50		ns
				tксү1/2 - 10		tkcy1/2 - 50		tkcy1/2 - 50		ns
SIp setup time (to SCKp↑) ^{Note 1}	tsıкı	$\begin{array}{l} 4.0 \ V \leq EV_{DDO} \\ 2.7 \ V \leq V_{b} \leq V_{b} \\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	0 ≤ 5.5 V, 4.0 V, = 1.4 kΩ	58		479		479		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq \\ C_{b} \texttt{=} 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) ^{Note 1}	tĸsı1	$\begin{array}{l} 4.0 \ V \leq EV_{DDO} \\ 2.7 \ V \leq V_{b} \leq V_{b} \\ C_{b} \texttt{=} 20 \ pF, \ R_{b} \end{array}$	0 ≤ 5.5 V, 4.0 V, = 1.4 kΩ	10		10		10		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq 1 \\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp out- put ^{Note 1}	tkso1	$\begin{array}{l} 4.0 \ V \leq EV_{DD}\\ 2.7 \ V \leq V_{b} \leq V\\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	0 ≤ 5.5 V, 4.0 V, = 1.4 kΩ		60		60		60	ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq \\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ		130		130		130	ns

(TA = -40 to +85°C, 2.7 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(Notes, Caution, and Remarks are listed on the next page.)



(3) I²C fast mode plus

(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Co	Conditions		h-speed mode	LS (lov main)	v-speed mode	LV (low main)	-voltage mode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsc∟	$\begin{array}{ll} \mbox{Fast mode plus:} & 2.7 \ \mbox{V} \leq EV_{DD0} \leq 5.5 \ \mbox{V} \\ \mbox{fcLk} \geq 10 \ \mbox{MHz} \end{array}$		0	1000	_		-		kHz
Setup time of restart condi- tion	tsu: sta	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		0.26		_		-		μs
Hold time Note 1	thd: STA	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		0.26		—		—		μs
Hold time when SCLA0 = "L"	t∟ow	$2.7~V \leq EV_{DD0} \leq 5$	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			—		-		μs
Hold time when SCLA0 = "H"	tніgн	$2.7~V \leq EV_{DD0} \leq 5$.5 V	0.26		—		-	-	μs
Data setup time (reception)	tsu: dat	$2.7~V \leq EV_{DD0} \leq 5$.5 V	50		—		-	_	ns
Data hold time (transmission) Note 2	thd: dat	$2.7~V \leq EV_{DD0} \leq 5.5~V$		0	0.45		_		-	μs
Setup time of stop condition	tsu: sto	$2.7~V \leq EV_{DD0} \leq 5$	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$.26 —		_	-	_	μs
Bus-free time	t BUF	$2.7~V \leq EV_{DD0} \leq 5$.5 V	0.5		-	_	_	_	μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of the DEDAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

- Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.
- Note 3. The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows. Fast mode plus: Cb = 120 pF, Rb = 1.1 k Ω

IICA serial transfer timing



Remark n = 0, 1



2.7 **RAM Data Retention Characteristics**

(TA = -40 to +85°C, Vss = 0V)									
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit			
Data retention supply voltage	VDDDR		1.46 Note		5.5	V			

The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset Note is effected, but RAM data is not retained when a POR reset is effected.



2.8 **Flash Memory Programming Characteristics**

$(1A = -40 tO + 60 C, 1.6 V \le VDD \le 0.5 V, VSS = 0 V$	$(T_A = -40 \text{ to } +85^{\circ}\text{C}.)$	$1.8 \text{ V} \leq \text{VDD} \leq 5.5$	V. Vss = 0 V)
---	--	--	-----------------

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fclk	$1.8~V \leq V_{DD} \leq 5.5~V$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years Ta = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 **Dedicated Flash Memory Programmer Communication (UART)**

(TA = -40 to +85°C, 1.8 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps



3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C)

This chapter describes the following electrical specifications. Target products G: Industrial applications $T_A = -40$ to $+105^{\circ}C$ R5F104xxGxx

- Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.
- Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.
- Caution 4. Please contact Renesas Electronics sales office for derating of operation under TA = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
- Remark When RL78/G14 is used in the range of T_A = -40 to +85°C, see 2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C).



Items	Symbol	Condition	IS	MIN.	TYP.	MAX.	Unit
Output voltage, high	Voh1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57,	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7			V
		P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110,	2.7 V ≤ EVDD0 ≤ 5.5 V, Іон1 = -2.0 mA	EVDD0 - 0.6			V
		P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V, Іон1 = -1.5 mA	EVDD0 - 0.5			V
	Voh2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA	Vdd - 0.5			V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ I_{OL1} = 8.5 \ mA \end{array}$			0.7	V
			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ IOL1 = 3.0 mA			0.6	V
			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ IOL1 = 1.5 mA			0.4	V
			$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ IOL1 = 0.6 mA			0.4	V
	Vol2	P20 to P27, P150 to P156	$\begin{array}{l} 2.4 \ V \leq V \ \text{DD} \leq 5.5 \ V, \\ I \ \text{OL2} = 400 \ \mu A \end{array}$			0.4	V
	Vol3	P60 to P63	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ IOL3 = 15.0 mA			2.0	V
			$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V},$ $\text{IOL3 = 5.0 \text{ mA}}$			0.4	V
			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ IOL3 = 3.0 mA			0.4	V
			$2.4 \text{ V} \le \text{EVDD0} \le 5.5 \text{ V},$ IOL3 = 2.0 mA			0.4	V

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(4/5)

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



Parameter Symbo Conditions MIN. TYP. MAX. fносо = 64 MHz, $V_{DD} = 5.0 V$ 2.6 Supply DD1 Operat-HS (high-speed main) Basic current ing mode mode Note 5 fill = 32 MHz Note 3 operation VDD = 3.0 V 2.6 Note 1 fносо = 32 MHz. Basic VDD = 5.0 V 2.3 fiH = 32 MHz Note 3 operation VDD = 3.0 V 2.3 fносо = 64 MHz, VDD = 5.0 V HS (high-speed main) Normal 5.4 10.9 mode Note 5 fiH = 32 MHz Note 3 operation $V_{DD} = 3.0 V$ 54 10.9 VDD = 5.0 V 10.3 fносо = 32 MHz. Normal 5.0 fin = 32 MHz Note 3 operation VDD = 3.0 V 10.3 5.0 VDD = 5.0 V fHOCO = 48 MHz. 42 82 Normal fiH = 24 MHz Note 3 operation VDD = 3.0 V 4.2 8.2 fносо = 24 MHz, Normal VDD = 5.0 V 4.0 7.8 fill = 24 MHz Note 3 operation VDD = 3.0 V 40 78 fносо = 16 MHz, Normal VDD = 5.0 V 3.0 5.6 fin = 16 MHz Note 3 operation VDD = 3.0 V 3.0 5.6 HS (high-speed main) 3.4 f_{MX} = 20 MHz Note 2 Normal Square wave input 6.6 mode Note 5 VDD = 5.0 V operation Resonator connection 3.6 6.7 f_{MX} = 20 MHz Note 2, Normal Square wave input 34 6.6 operation $V_{DD} = 3.0 V$ Resonator connection 3.6 6.7 fmx = 10 MHz Note 2, 2.1 3.9 Normal Square wave input VDD = 5.0 V operation Resonator connection 22 4.0 f_{MX} = 10 MHz Note 2. Normal Square wave input 2.1 3.9 VDD = 3.0 V operation Resonator connection 2.2 4.0 fsub = 32.768 kHz Note 4 49 71 Subsystem clock Normal Square wave input operation operation $T_A = -40^{\circ}C$ Resonator connection 4.9 7.1 fsub = 32.768 kHz Note 4 Normal Square wave input 4.9 7.1 $T_A = +25^{\circ}C$ operation 4.9 7.1 Resonator connection Normal 5.1 8.8 fsub = 32.768 kHz Note 4 Square wave input $T_A = +50^{\circ}C$ operation 8.8 Resonator connection 5.1 10.5 fsub = 32.768 kHz Note 4 Square wave input 5.5 Normal TA = +70°C operation Resonator connection 5.5 10.5 fsub = 32.768 kHz Note 4 Normal 6.5 14.5 Square wave input TA = +85°C operation 6.5 14.5 Resonator connection

fsub = 32.768 kHz Note 4

 $T_{A} = +105^{\circ}C$

Normal

operation

Square wave input

Resonator connection

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(Notes and Remarks are listed on the next page.)

Unit

mΑ

mΑ

mΑ

μΑ

13.0

13.0

58.0

58.0

<R>

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply cur-	IDD2	HALT mode	HS (high-speed main)	fносо = 64 MHz,	VDD = 5.0 V		0.93	5.16	mA
rent Note 1	Note 2		mode Note 7	fiH = 32 MHz Note 4	VDD = 3.0 V		0.93	5.16	
				fносо = 32 MHz,	VDD = 5.0 V		0.5	4.47	1
				fiн = 32 MHz Note 4	VDD = 3.0 V		0.5	4.47	
				fносо = 48 MHz,	VDD = 5.0 V		0.72	4.08	
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.72	4.08	1
				fносо = 24 MHz,	V _{DD} = 5.0 V		0.42	3.51	
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.42	3.51	
				fносо = 16 MHz,	VDD = 5.0 V		0.39	2.38	
				fiH = 16 MHz Note 4	VDD = 3.0 V		0.39	2.38	
			HS (high-speed main)	f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.31	2.83	mA
			mode Note 7	VDD = 5.0 V	Resonator connection		0.41	2.92	
				f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.31	2.83	
				VDD = 3.0 V	Resonator connection		0.41	2.92	
				f _{MX} = 10 MHz Note 3,	Square wave input		0.21	1.46	
				VDD = 5.0 V	Resonator connection		0.26	1.57	
		f _{MX} = 10 MHz ^{Note 3} ,	Square wave input		0.21	1.46	1		
				VDD = 3.0 V	Resonator connection		0.26	1.57	1
			Subsystem clock oper-	fsue = 32.768 kHz Note 5,	Square wave input		0.31	0.76	μΑ
			ation	Ta = -40°C	Resonator connection		0.50	0.95	
				fsue = 32.768 kHz Note 5,	Square wave input		0.38	0.76	
				TA = +25°C	Resonator connection		0.57	0.95	
				fsue = 32.768 kHz ^{Note 5} ,	Square wave input		0.47	3.59	
				TA = +50°C	Resonator connection		0.70	3.78	
				fsub = 32.768 kHz Note 5,	Square wave input		0.80	6.20	
				T _A = +70°C	Resonator connection		1.00	6.39	
				fsue = 32.768 kHz ^{Note 5} ,	Square wave input		1.65	10.56	
				TA = +85°C	Resonator connection		1.84	10.75	
				fsue = 32.768 kHz ^{Note 5} ,	Square wave input		8.00	65.7	
				T _A = +105°C	Resonator connection		8.00	65.7	
	IDD3	STOP mode	TA = -40°C				0.19	0.63	μA
	Note 6	Note 8	TA = +25°C				0.30	0.63	
			TA = +50°C				0.41	3.47	
			T _A = +70°C				0.80	6.08	
			TA = +85°C				1.53	10.44	
			T _A = +105°C				6.50	67.14	

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(Notes and Remarks are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) (TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Conditions		Symbol Conditions HS (high-speed main mode		peed main) ode	Unit
				MIN.	MAX.		
SCKp cycle time	t КСҮ1	tĸcy1 ≥ 4/fcLĸ	$2.7~\text{V} \leq \text{Evdd0} \leq 5.5~\text{V}$	250		ns	
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	500		ns	
SCKp high-/low-level width	tĸнı, tĸ∟ı	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү1/2 - 24		ns	
		$2.7 V \le EV_{DD0} \le 5.5 V$ $2.4 V \le EV_{DD0} \le 5.5 V$		tксү1/2 - 36		ns	
				tксү1/2 - 76		ns	
SIp setup time (to SCKp↑) Note 1	tsıĸı	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		66		ns	
		$2.7 V \le EV_{DD0} \le 5.5 V$ $2.4 V \le EV_{DD0} \le 5.5 V$		66		ns	
				113		ns	
SIp hold time (from SCKp [↑]) Note 2	tksii			38		ns	
Delay time from SCKp \downarrow to SOp output ^{Note 3}	tkso1	C = 30 pF Note 4			50	ns	

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

- Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).
- **Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)
- Remark 2. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))



(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed	main) mode	Unit
				MIN.	MAX.	
SCKp cycle time Note 5	tксү2	$4.0~V \leq EV_{DD0} \leq 5.5~V$	20 MHz < fмск	16/fмск		ns
			fмск ≤ 20 MHz	12/fмск		ns
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	16 MHz < fмск	16/f мск		ns
			fмск ≤ 16 MHz	12/fмск		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	·	12/fмск and 1000		ns
SCKp high-/low-level width	tkh2, tkl2	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү2/2 - 14		ns
		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			ns
		$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$		tĸcy2/2 - 36		ns
SIp setup time (to SCKp↑) ^{Note 1}	tsık2	$2.7~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$		1/fмск + 40		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		1/fмск + 60		ns
SIp hold time (from SCKp [↑]) Note 2	tksi2			1/fмск + 62		ns
Delay time from SCKp \downarrow to SOp output $^{Note\;3}$	tkso2	C = 30 pF Note 4 $2.7 V \le EV_{DD0} \le 5.5 V$			2/fмск + 66	ns
			$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		2/fмск + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))





CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31) Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

The smaller maximum transfer rate derived by using fMck/12 or the following expression is the valid maximum transfer Note 5. rate.

Expression for calculating the transfer rate when 2.4 V \leq EVDD0 < 3.3 V and 1.6 V \leq Vb \leq 2.0 V

1

Maximum transfer rate =
$$\frac{1.5}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$

Baud rate e

$$\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}$$

$$(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Note 6. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.
- Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin Caution products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(TA = -40 to +105°C, 2	$2.4 V \leq EVDD0 = EVDD^{2}$	$1 \leq VDD \leq 5.5 V, VSS$	= EVss0 $=$ EVss1 $=$ 0 V)
(

(1/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	fsc∟			400 Note 1	kHz
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		400 Note 1	kHz
		$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_{b} \leq 4.0 \; V, \\ C_{b} = 100 \; pF, \; R_{b} = 2.8 \; k\Omega \end{array}$		100 Note 1	kHz
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		100 Note 1	kHz
		$\label{eq:2.4} \begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$		100 Note 1	kHz
Hold time when SCLr = "L"	tLOW		1200		ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	1200		ns
			4600		ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	4600		ns
		$\begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$	4650		ns
Hold time when SCLr = "H"	tнigн		620		ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	500		ns
		$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 100 \; pF, \; R_b = 2.8 \; k\Omega \end{array}$	2700		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	2400		ns
		$\label{eq:2.4} \begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$	1830		ns



3.7 **RAM Data Retention Characteristics**

(TA = -40 to +105°C, Vss = 0V)								
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Data retention supply voltage	VDDDR		1.44 Note		5.5	V		

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 **Flash Memory Programming Characteristics**

($T_{A} = -40 \text{ to}$	+105°C. 2.4	↓ V ≤ V	/DD ≤ 5.5 \	V. Vss	= 0 V)
	14 - 10 10				-,	- • • • •

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fclk	$2.4~V \leq V \text{dd} \leq 5.5~V$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years TA = 85°C ^{Note 4}	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C ^{Note 4}	100,000			
		Retained for 20 years TA = 85°C ^{Note 4}	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps



4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18







NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.



·κ

Α 9.85±0.15 в 0.45 MAX С 0.65 (T.P.) $0.24_{-0.07}^{+0.08}$ D F 0.1±0.05 F 1.3±0.1 G 1.2 8.1±0.2 Н 6.1±0.2 I 1.0±0.2 J 0.17±0.03 κ L 0.5 0.13 Μ Ν 0.10 Р 3°+5° 0.25 т 0.6±0.15 U

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