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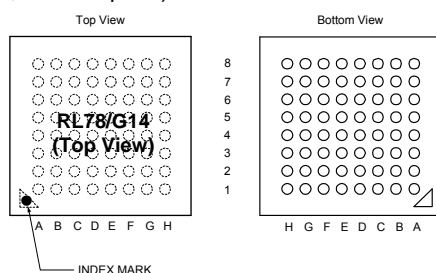
What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104bcana-v0

• 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)

	A	B	C	D	E	F	G	H	
8	EVDD0	EVSS0	P121/X1	P122/X2/EXCLK	P137/INTP0	P123/XT1	P124/XT2/EXCLKS	P120/ANI19/VCOUT0 Note 1	8
7	P60/SCLA0	VDD	VSS	REGC	RESET	P01/TO00/TRGCLKB/TRJIO0	P00/TI00/TRGCLKA/(TRJO0)	P140/PCLBUZ0/INTP6	7
6	P61/SDAA0	P62/SSI00	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/SO10/TxD1	P141/PCLBUZ1/INTP7	6
5	P77/KR7/INTP11/(TXD2)	P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/SI10/RxD1/SDA10	P04/SCK10/SCL10	P130	P20/ANI0/AVREFP	5
4	P75/KR5/INTP9/SCK01/SCL01	P76/KR6/INTP10/(RXD2)	P52/(INTP1)	P54/(INTP3)	P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 Note 1/(SI00)/(RXD0)	P21/ANI1/AVREFM	P22/ANI2/ANO0 Note 1	P23/ANI3/ANO1 Note 1	4
3	P70/KR0/SCK21/SCL21	P73/KR3/SO01	P74/KR4/INTP8/SI01/SDA01	P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 Note 1/(SO00)/(TXD0)	P15/SCK20/SCL20/TRDIOB0/(SDAA0)	P12/SO11/TRDIOB1/IVREF1 Note 1/(INTP5)/(TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0	P72/KR2/SO21	P71/KR1/SI21/SDA21	P06/(INTP11)/(TRJIO0)	P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)	P11/SI11/SDA11/TRDIOC1/(RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)	P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB	P55/(PCLBUZ1)/(SCK00)/(INTP4)	P13/TxD2/SO20/TRDIOA1/IVCMP1 Note 1	P10/SCK11/SCL11/TRDIOD1	P146	P147/ANI18/VCOUT1 Note 1	1
	A	B	C	D	E	F	G	H	

Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.
Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.
Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

(2/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Clock output/buzzer output		2	2	2	2

		[30-pin, 32-pin, 36-pin products]
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz
		  (Main system clock: f_{MAIN} = 20 MHz operation)
		[40-pin products]
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz
		  (Main system clock: f_{MAIN} = 20 MHz operation)
		• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz
		  (Subsystem clock: f_{SUB} = 32.768 kHz operation)			

8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels			
	I²C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		28 sources			29 sources
Event link controller (ELC)		Event input: 19 Event trigger output: 7			Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			

Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = −40 to +85°C)
		                                      1.51 ±0.06 V (T_A = −40 to +105°C)
		• Power-down-reset: 1.50 ±0.04 V (T_A = −40 to +85°C)
		                                      1.50 ±0.06 V (T_A = −40 to +105°C)			

Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = −40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = −40 to +105°C)			
Operating ambient temperature		T_A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note   The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

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Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Clock output/buzzer output		2	2	2	2

		[30-pin, 32-pin, 36-pin products]
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz
		  (Main system clock: f_{MAIN} = 20 MHz operation)
		[40-pin products]
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz
		  (Main system clock: f_{MAIN} = 20 MHz operation)
		• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz
		  (Subsystem clock: f_{SUB} = 32.768 kHz operation)			

8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
D/A converter		1 channel	2 channels		
Comparator		2 channels			
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels			
	I2C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources			31 sources
Event link controller (ELC)		Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			

Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = −40 to +85°C)
		                          1.51 ±0.06 V (T_A = −40 to +105°C)
		• Power-down-reset: 1.50 ±0.04 V (T_A = −40 to +85°C)
		                          1.50 ±0.06 V (T_A = −40 to +105°C)			

Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = −40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = −40 to +105°C)			
Operating ambient temperature		T_A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note   The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5			V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7			V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5			V
			1.6 V ≤ EVDD0 < 1.8 V, IOH1 = -1.0 mA	EVDD0 - 0.5			V
	VOH2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOH2 = -100 µA	VDD - 0.5			V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 20.0 mA			1.3	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA			0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA			0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.3 mA			0.4	V
	VOL2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 400 µA			0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA			2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA			0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA			0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA			0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA			0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(T$_A$ = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD1}$	Operating mode	HS (high-speed main) mode Note 5	f$_{HOCO}$ = 64 MHz, f$_{IH}$ = 32 MHz Note 3	Basic operation	V$_{DD}$ = 5.0 V		2.9		mA
						V$_{DD}$ = 3.0 V		2.9		
				f$_{HOCO}$ = 32 MHz, f$_{IH}$ = 32 MHz Note 3	Basic operation	V$_{DD}$ = 5.0 V		2.5		
						V$_{DD}$ = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f$_{HOCO}$ = 64 MHz, f$_{IH}$ = 32 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		6.0	11.2	mA
						V$_{DD}$ = 3.0 V		6.0	11.2	
				f$_{HOCO}$ = 32 MHz, f$_{IH}$ = 32 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		5.5	10.6	
						V$_{DD}$ = 3.0 V		5.5	10.6	
				f$_{HOCO}$ = 48 MHz, f$_{IH}$ = 24 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		4.7	8.6	
						V$_{DD}$ = 3.0 V		4.7	8.6	
				f$_{HOCO}$ = 24 MHz, f$_{IH}$ = 24 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		4.4	8.2	
						V$_{DD}$ = 3.0 V		4.4	8.2	
				f$_{HOCO}$ = 16 MHz, f$_{IH}$ = 16 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		3.3	5.9	
						V$_{DD}$ = 3.0 V		3.3	5.9	
			LS (low-speed main) mode Note 5	f$_{HOCO}$ = 8 MHz, f$_{IH}$ = 8 MHz Note 3	Normal operation	V$_{DD}$ = 3.0 V		1.5	2.5	mA
						V$_{DD}$ = 2.0 V		1.5	2.5	
			LV (low-voltage main) mode Note 5	f$_{HOCO}$ = 4 MHz, f$_{IH}$ = 4 MHz Note 3	Normal operation	V$_{DD}$ = 3.0 V		1.5	2.1	mA
						V$_{DD}$ = 2.0 V		1.5	2.1	
			HS (high-speed main) mode Note 5	f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.7	6.8	
						Resonator connection		3.9	7.0	
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
			LS (low-speed main) mode Note 5	f$_{MX}$ = 8 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f$_{MX}$ = 8 MHz Note 2, V$_{DD}$ = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 4, T$_A$ = -40°C	Normal operation	Square wave input		5.2		μA
						Resonator connection		5.2		
				f$_{SUB}$ = 32.768 kHz Note 4, T$_A$ = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f$_{SUB}$ = 32.768 kHz Note 4, T$_A$ = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f$_{SUB}$ = 32.768 kHz Note 4, T$_A$ = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f$_{SUB}$ = 32.768 kHz Note 4, T$_A$ = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(**Notes** and **Remarks** are listed on the next page.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)   **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 400		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/f_{MCK} + 400		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400		ns

Caution   **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark   p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)
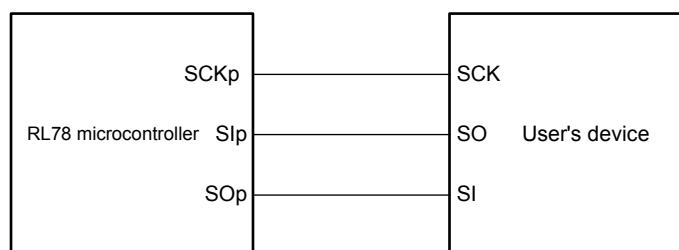
CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))
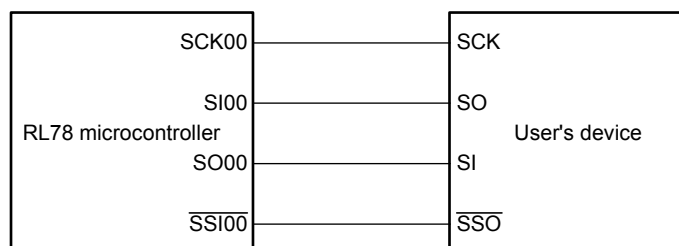
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Note 4.　This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5.　Use it with EV$_{DD0}$ ≥ V$_b$.

Note 6.　The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV$_{DD0}$ < 3.3 V and 1.6 V ≤ V$_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7.　This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution　**Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $EV_{DD0} \geq V_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)
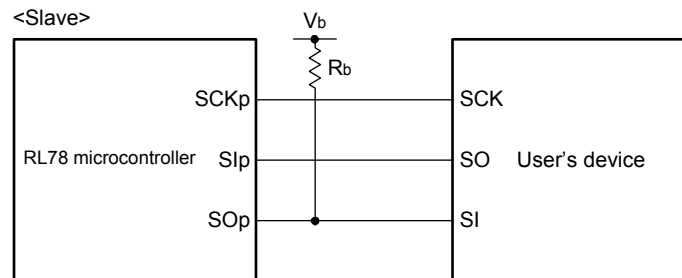
Remark 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

2.10   Timing of Entry to Flash Memory Programming Modes

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t$_{SUINIT}$	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t$_{SU}$	POR and LVD reset must end before the external reset ends.	10			µs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must end before the external reset ends.	1			ms
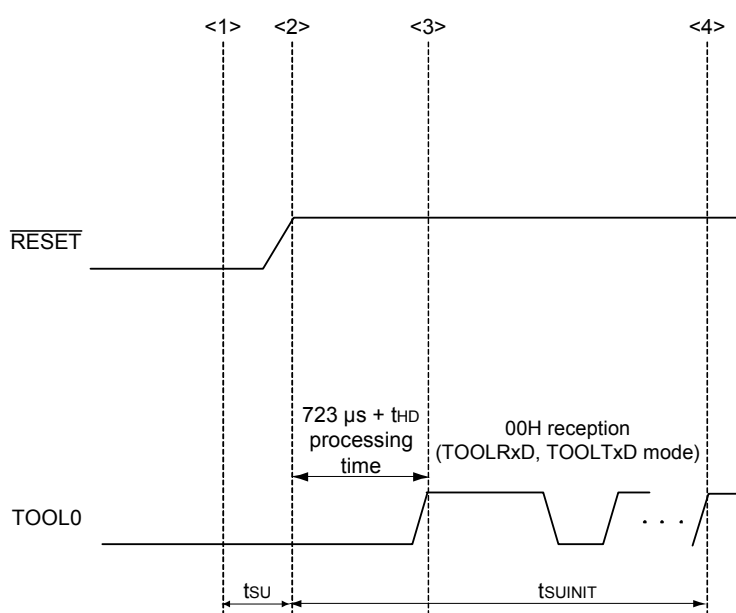
<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark   t$_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

t$_{SU}$:   How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t$_{HD}$:   How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3.2   Oscillator Characteristics

3.2.1   X1, XT1 characteristics

(T_A = -40 to +105°C, 2.4 V $\leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V $\leq V_{DD} \leq$ 5.5 V	1.0		20.0	MHz
		2.4 V $\leq V_{DD}$ < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note   Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

3.2.2   On-chip oscillator characteristics

(T_A = -40 to +105°C, 2.4 V $\leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V $\leq V_{DD} \leq$ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	2.4 V $\leq V_{DD} \leq$ 5.5 V	-1.5		+1.5	%
		+85 to +105°C	2.4 V $\leq V_{DD} \leq$ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1.   High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2.   This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -3.0 mA	EV$_{DD0}$ - 0.7			V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -2.0 mA	EV$_{DD0}$ - 0.6			V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -1.5 mA	EV$_{DD0}$ - 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OH2}$ = -100 μA	V$_{DD}$ - 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V

Caution   **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = -40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t$_{TDIH}$, t$_{TDIL}$	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/f$_{CLK}$			ns
Timer RD forced cutoff signal input low-level width	t$_{TDSIL}$	P130/INTP0	2MHz < f$_{CLK}$ ≤ 32 MHz	1			µs
			f$_{CLK}$ ≤ 2 MHz	1/f$_{CLK}$ + 1			
Timer RG input high-level width, low-level width	t$_{TGIH}$, t$_{TGIL}$	TRGIOA, TRGIOB		2.5/f$_{CLK}$			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	1			µs
		INTP1 to INTP11	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V	1			µs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V	250			ns
$\overline{RESET}$ low-level width	t$_{RSL}$			10			µs

3.6.2   Temperature sensor characteristics/internal reference voltage characteristic

(T_A = -40 to +105°C, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3   D/A converter characteristics

(T_A = -40 to +105°C, 2.4 V $\leq$ EV_{SS0} = EV_{SS1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V $\leq$ V_{DD} $\leq$ 5.5 V			3	μs
			2.4 V $\leq$ V_{DD} < 2.7 V			6	μs

3.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T$_A$ = -40 to +105°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V$_{LVD0}$	Rising edge	3.90	4.06	4.22	V
			Falling edge	3.83	3.98	4.13	V
		V$_{LVD1}$	Rising edge	3.60	3.75	3.90	V
			Falling edge	3.53	3.67	3.81	V
		V$_{LVD2}$	Rising edge	3.01	3.13	3.25	V
			Falling edge	2.94	3.06	3.18	V
		V$_{LVD3}$	Rising edge	2.90	3.02	3.14	V
			Falling edge	2.85	2.96	3.07	V
		V$_{LVD4}$	Rising edge	2.81	2.92	3.03	V
			Falling edge	2.75	2.86	2.97	V
		V$_{LVD5}$	Rising edge	2.70	2.81	2.92	V
			Falling edge	2.64	2.75	2.86	V
		V$_{LVD6}$	Rising edge	2.61	2.71	2.81	V
			Falling edge	2.55	2.65	2.75	V
		V$_{LVD7}$	Rising edge	2.51	2.61	2.71	V
			Falling edge	2.45	2.55	2.65	V
Minimum pulse width		t$_{LW}$		300			μs
Detection delay time						300	μs

4. PACKAGE DRAWINGS

4.1   30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18

detail of lead end
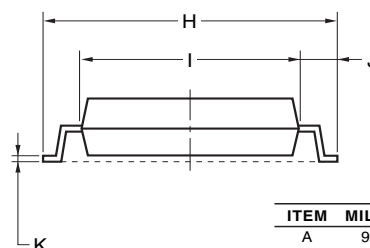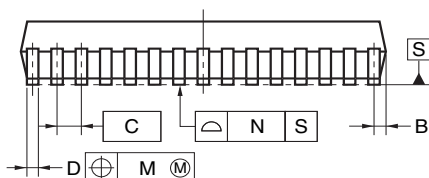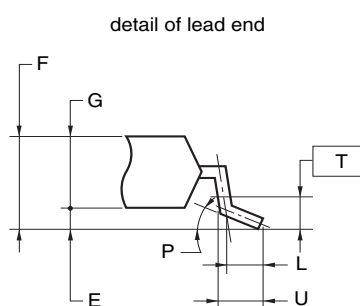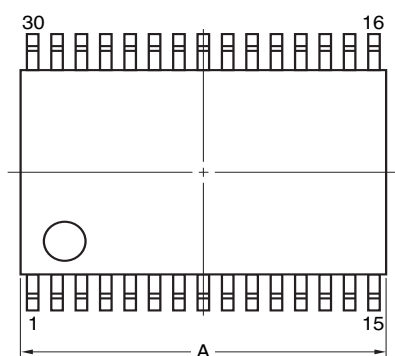
NOTE

Each lead centerline is located within 0.13 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB, R5F104LJAFB

R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB, R5F104LJDFB

R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB, R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35
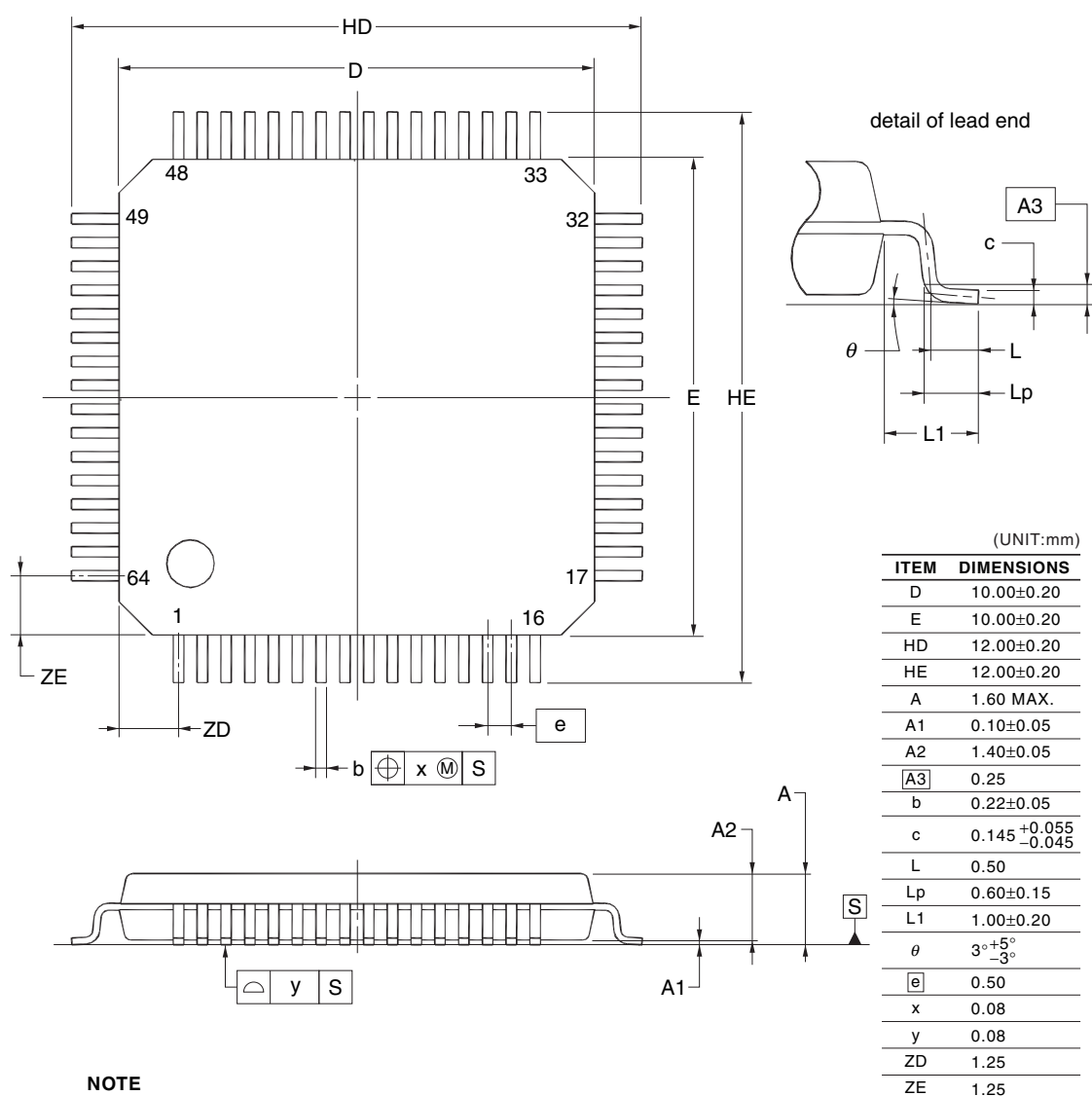
detail of lead end

(UNIT:mm)

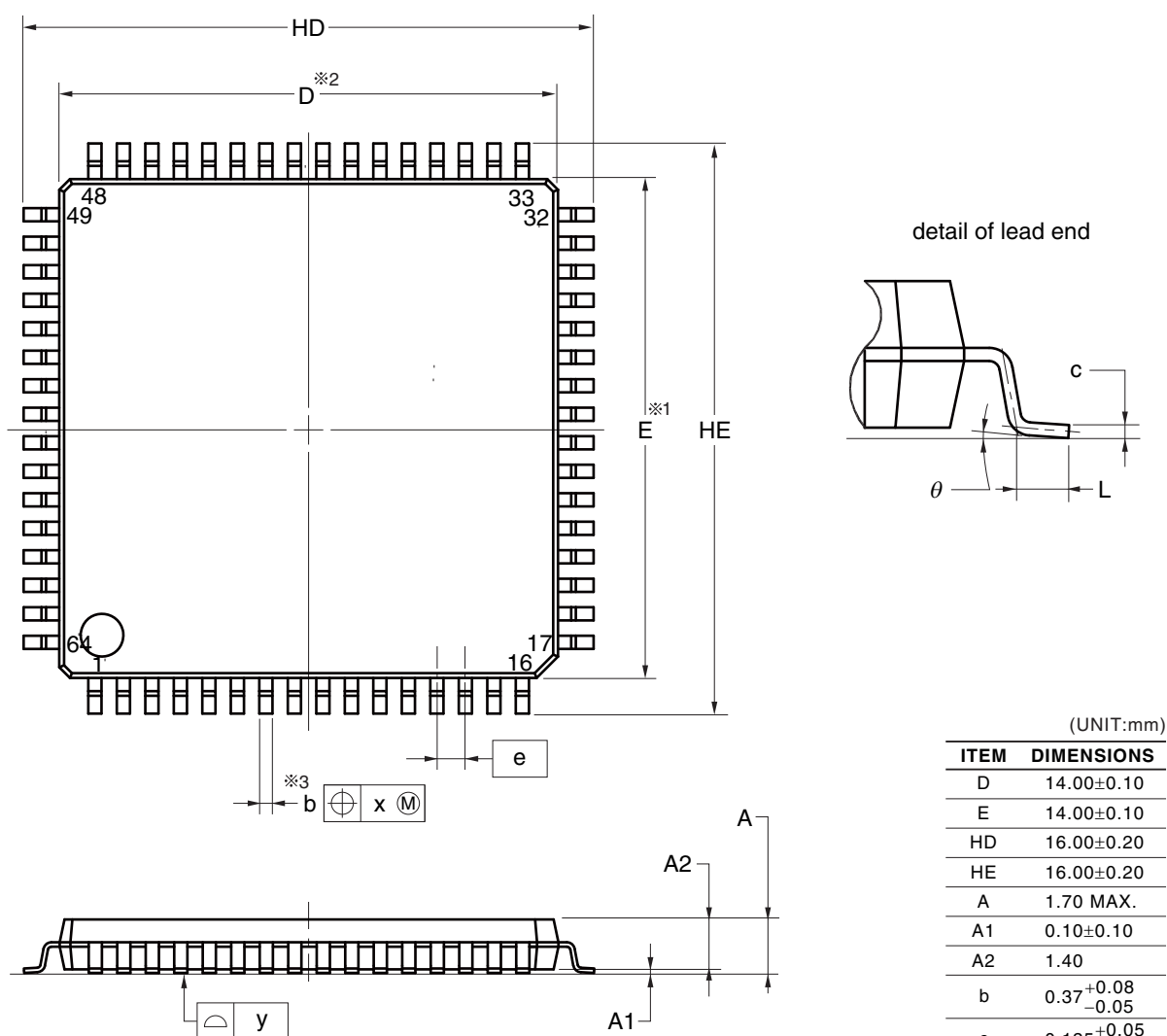| ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 {}^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° {}^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LFDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.10
E	14.00±0.10
HD	16.00±0.20
HE	16.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	$0.37^{+0.08}_{-0.05}$
c	$0.125^{+0.05}_{-0.02}$
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

4.9   80-pin products

R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
R5F104MFDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.