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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104bgdfp-x0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.3.6 48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



- **Note 2.** Mounted on the 384 KB or more code flash memory products.
- Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).
- Remark 1. For pin identification, see 1.4 Pin Identification.
- **Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5 Block Diagram

1.5.1 30-pin products



Note Mounted on the 96 KB or more code flash memory products.



1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.



Note	The flash library uses RAM in self-programming and rewriting of the data flash memory.
	The target products and start address of the RAM areas used by the flash library are shown below.
	R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
	For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family
	(R20UT2944).



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		44-pin	48-pin	52-pin	64-pin			
l	tem	R5F104Fx	R5F104Gx	R5F104Jx	R5F104Lx			
		(x = F to H, J)	(x = F to H, J)	(x = F to H, J)	(x = F to H, J)			
Clock output/buzz	zer output	2	2	2	2			
		• 2.44 kHz, 4.88 kHz,	9.76 kHz, 1.25 MHz, 2.	5 MHz, 5 MHz, 10 MHz				
		(Main system clock:	fMAIN = 20 MHz operation	on)				
		• 256 Hz, 512 Hz, 1.0	24 KHZ, 2.048 KHZ, 4.09	96 kHz, 8.192 kHz, 16.3 tion)	384 kHz, 32.768 kHz			
9/10 bit recolution					12 obonnolo			
8/10-bit resolution	TA/D converter		To channels	12 channels	12 channels			
D/A converter		2 channels						
Comparator		2 channels						
Serial interface		[44-pin products]			:6 - d 120 - 4 - d - a - a - a - a			
		CSI: 1 channel/UAR		N-DUS): 1 channel/simpi	Iffed I2C: 1 channel			
		CSI: 2 channels/LIAI	RT: 1 channel/simplified	I ² C: 2 channels				
		[48-pin, 52-pin produc	ts]					
		CSI: 2 channels/UAI	RT (UART supporting L	IN-bus): 1 channel/simp	olified I ² C: 2 channels			
		CSI: 1 channel/UAR	T: 1 channel/simplified I	² C: 1 channel				
		CSI: 2 channels/UAF	RT: 1 channel/simplified	I ² C: 2 channels				
		[64-pin products]						
		• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 2 channels						
		CSI: 2 cnannels/UART: 1 channel/simplified I ² C: 2 channels						
		• CSI: 2 channels/UAI	RI: 1 channel/simplified		1			
	I ² C bus		1 channel	1 channel	1 channel			
Data transfer con	troller (DTC)	31 sources	32 sources		33 sources			
Event link control	ler (ELC)	Event input: 22						
	1	Event trigger output: 9)	1				
Vectored inter-	Internal	24	24	24	24			
Tupi sources	External	7	10	12	13			
Key interrupt		4	6	8	8			
Reset		Reset by RESET pir	ı					
		 Internal reset by wat 	chdog timer					
		Internal reset by pov	ver-on-reset					
		Internal reset by volu	age delector	Note				
		Internal reset by RA	M parity error					
		Internal reset by illegal-memory access						
Power-on-reset c	ircuit	Power-on-reset:	1.51 ±0.04 V (TA = -40	to +85°C)				
			1.51 ±0.06 V (TA = -40	to +105°C)				
		• Power-down-reset: 1.50 ±0.04 V (TA = -40 to +85°C)						
		$1.50 \pm 0.06 \text{ V} (1\text{A} = -40 \text{ to } +105^{\circ}\text{C})$						
Voltage detector		1.63 V to 4.06 V (14 stages)						
On-chip debug fu	nction	Provided						
Power supply vol	tage	VDD = 1.6 to 5.5 V (TA	$= -40 \text{ to } +85^{\circ}\text{C}$					
Operating and in	at tomporet	VDD = 2.4 to 5.5 V (1A = -40 to +105°C)						
Operating ambier	it temperature	$IA = -40$ to $+85^{\circ}C$ (A: $T_{A} = -40$ to $+105^{\circ}C$ (C	Consumer applications	, ט: industrial applicatio	ns),			
		IA+0 10 + 105 C (G		/				

Note

The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (TA = -40 to $+85^{\circ}$ C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^{\circ}C$

R5F104xxAxx

- D: Industrial applications TA = -40 to +85°C R5F104xxDxx
- G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C R5F104xxGxx
- Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.
- Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.



2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

$(TA = -40 \text{ to } +85^{\circ}C, 1.6 \text{ V} \le \text{VDD} \le 5.5 \text{ V}, \text{Vss} = 0 \text{ V})$

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/	$2.7~V \leq V \text{DD} \leq 5.5~V$	1.0		20.0	MHz
	crystal resonator	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	1.0		16.0	
		$1.8 \text{ V} \leq \text{V}_{\text{DD}} < 2.4 \text{ V}$	1.0		8.0	
		$1.6 \text{ V} \le \text{V}_{\text{DD}} < 1.8 \text{ V}$	1.0		4.0	
XT1 clock oscillation frequency (fxT) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

- Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
- Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G14 User's Manual.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V \leq VDD \leq 5.5 V, Vss = 0 V)

Oscillators	Parameters	C	conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fiн			1		32	MHz
High-speed on-chip oscillator clock frequency		-20 to +85°C	$1.8~V \le V_{DD} \le 5.5~V$	-1.0		+1.0	%
accuracy			$1.6 \text{ V} \le \text{V}_{\text{DD}} < 1.8 \text{ V}$	-5.0		+5.0	%
		-40 to -20°C	$1.8 \text{ V} \le \text{V}_{\text{DD}} < 5.5 \text{ V}$	-1.5		+1.5	%
			$1.6 \text{ V} \le \text{V}_{\text{DD}} < 1.8 \text{ V}$	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.



- Note 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or Vss, EVss0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3. When high-speed system clock and subsystem clock are stopped.
- Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer
- Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq VDD \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq VDD \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq VDD \leq 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V \leq VDD \leq 5.5 V@1 MHz to 4 MHz

- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.) Remark 3. file:
- High-speed on-chip oscillator clock frequency (32 MHz max.) Remark 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

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- Note 1. Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 Note 2. During HALT instruction execution by flash memory.
- **Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 4.** When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 32 MHz
 - 2.4 V \leq VDD \leq 5.5 V@1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 4 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remark 3.** file: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsuB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C





TCY vs VDD (LS (low-speed main) mode)

TCY vs VDD (LV (low-voltage main) mode)







CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31) Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

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2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, T _A = +25°C		1.05		V
Internal reference voltage	Vbgr	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tamp		5			μs

(TA = -40 to +85°C, 2.4 V \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, HS (high-speed main) mode)

2.6.3 D/A converter characteristics

(TA = -40 to +85°C, 1.6 V \leq EVsso = EVss1 \leq VDD \leq 5.5 V, Vss = EVsso = EVss1 = 0 V)

Parameter	Symbol	Con	ditions	MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 M Ω	$1.8~V \le V_{DD} \le 5.5~V$			±2.5	LSB
		Rload = 8 M Ω	$1.8~V \le V_{DD} \le 5.5~V$			±2.5	LSB
Settling time	t SET	Cload = 20 pF	$2.7~V \leq V_{DD} \leq 5.5~V$			3	μs
			$1.6 \text{ V} \le \text{V}_{\text{DD}}$ < 2.7 V			6	μs



- Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
- **Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
- Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- **Note 8.** Current flowing during programming of the data flash.
- Note 9. Current flowing during self-programming.
- Note 10. For shift time to the SNOOZE mode, see 23.3.3 SNOOZE mode in the RL78/G14 User's Manual.
- **Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the HALT mode.
- **Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Note 13. A comparator and D/A converter are provided in products with 96 KB or more code flash memory.
- Remark 1. fil: Low-speed on-chip oscillator clock frequency
- Remark 2. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3. fcLK: CPU/peripheral hardware clock frequency
- Remark 4. Temperature condition of the TYP. value is TA = 25°C



AC Timing Test Points



External System Clock Timing



TI/TO Timing







3.6.4 Comparator

Parameter	Symbol	Col	nditions	MIN.	TYP.	MAX.	Unit
Input voltage range	lvref			0		EVDD0 - 1.4	V
	lvcmp			-0.3		EVDD0 + 0.3	V
Output delay	td	V _{DD} = 3.0 V Input slew rate > 50 mV/µs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode	e, window mode		0.76 Vdd		V
Low-electric-potential ref- erence voltage	VTW-	Comparator high-speed mode	e, window mode		0.24 Vdd		V
Operation stabilization wait time	tсмр			100			μs
Internal reference voltage Note	VBGR	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ HS}$ (h	nigh-speed main) mode	1.38	1.45	1.50	V

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Note Not usable in sub-clock operation or STOP mode.

3.6.5 POR circuit characteristics

(TA = -40 to +105°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.45	1.51	1.57	V
	VPDR	Voltage threshold on VDD falling Note 1	1.44	1.50	1.56	V
Minimum pulse width Note 2	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).





3.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR \leq VDD \leq 5.5 V, VSS = 0 V)

Pa	rameter	Symbol	Conditions	s MIN. TYP. MAX.		Unit	
Voltage detection	Supply voltage level	VLVD0	Rising edge	3.90	4.06	4.22	V
threshold			Falling edge	3.83	3.98	4.13	V
		VLVD1	Rising edge	3.60	3.75	3.90	V
			Falling edge	3.53	3.67	3.81	V
		VLVD2	Rising edge	3.01	3.13	3.25	V
			Falling edge	2.94	3.06	3.18	V
		VLVD3	Rising edge	2.90	3.02	3.14	V
			Falling edge	2.85	2.96	3.07	V
		VLVD4	Rising edge	2.81	2.92	3.03	V
			Falling edge	2.75	2.86	2.97	V
		VLVD5	Rising edge	2.70	2.81	2.92	V
			Falling edge	2.64	2.75	2.86	V
		VLVD6	Rising edge	2.61	2.71	2.81	V
			Falling edge	2.55	2.65	2.75	V
		VLVD7	Rising edge	2.51	2.61	2.71	V
			Falling edge	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay tim	le					300	μs



4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18







NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.



·κ

Α 9.85±0.15 в 0.45 MAX С 0.65 (T.P.) $0.24_{-0.07}^{+0.08}$ D F 0.1±0.05 F 1.3±0.1 G 1.2 8.1±0.2 Н 6.1±0.2 I 1.0±0.2 J 0.17±0.03 κ L 0.5 0.13 Μ Ν 0.10 Р 3°+5° 0.25 т 0.6±0.15 U

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R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA, R5F104GHANA, R5F104GJANA

R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA, R5F104GJDNA, R5F104GJDNA

R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,

R5F104GHGNA, R5F104GJGNA

R5F104GKANA, R5F104GLANA

R5F104GKGNA, R5F104GLGNA



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REVISION HISTORY

RL78/G14 Datasheet

Rev.	Date		Description	
		Page	Summary	
2.00	Oct 25, 2013	112 to 169	Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS	
		171 to 187	Modification of 4.1 30-pin products to 4.10 100-pin products	
3.00	Feb 07, 2014	All	Addition of products with maximum 512 KB flash ROM and 48 KB RAM	
		1	Modification of 1.1 Features	
		2	Modification of ROM, RAM capacities and addition of note 3	
		3	Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14	
		6 to 8	Addition of part number	
		15, 16	Modification of 1.3.6 48-pin products	
		17	Modification of 1.3.7 52-pin products	
		18, 19	Modification of 1.3.8 64-pin products	
		20	Modification of 1.3.9 80-pin products	
		21, 22	Modification of 1.3.10 100-pin products	
		35, 37, 39, 41, 43, 45, 47	Modification of operating ambient temperature in 1.6 Outline of Functions	
		42, 43	Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB)	
		46, 47	Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB)	
		65 to 68	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products	
		118	Modification of 2.7 Data Memory Retention Characteristics	
		137 to 140	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products	
		180	Modification of 3.7 Data Memory Retention Characteristics	
		189, 190	Addition and modification of 4.6 48-pin products	
		191	Modification of 4.7 52-pin products	
		193 to 195	Addition and modification of 4.8 64-pin products	
		198, 199	Addition and modification of 4.9 80-pin products	
		201, 202	Addition and modification of 4.10 100-pin products	
3.20	Jan 05, 2015	p.2	Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note	
		p.6	Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information	
		p.6 to 8	Deletion of note 2 in 1.2 Ordering Information	
		p.17	Deletion of note 2 in 1.3.7 52-pin products	
		p.36, 39, 42, 45, 48, 50, 52	Modification of description in 1.6 Outline of Functions	
		p.46, 48	Deletion of description of 52-pin in 1.6 Outline of Functions	
		p.47	Modification of note of 1.6 Outline of Functions	
		p.62, 64, 66, 68, 70, 72	Modification of specifications in 2.3.2 Supply current characteristics	

NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.