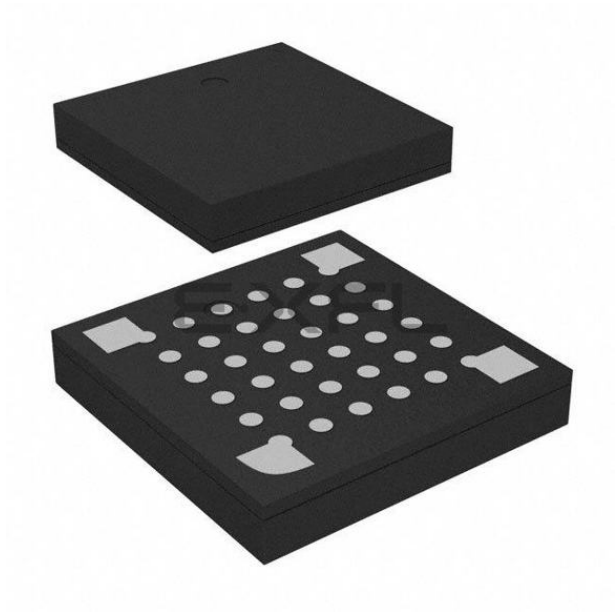
# Renesas Electronics America Inc - R5F104CAALA#U0 Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-WFLGA |
| Supplier Device Package | 36-WFLGA (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104caala-u0 |

○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G14 | | | |
|---|---|---|---|---|---|---|
| | | | 30 pins | 32 pins | 36 pins | 40 pins |
| 192 KB | 8 KB | 20 KB | — | — | — | R5F104EH |
| 128 KB | 8 KB | 16 KB | R5F104AG | R5F104BG | R5F104CG | R5F104EG |
| 96 KB | 8 KB | 12 KB | R5F104AF | R5F104BF | R5F104CF | R5F104EF |
| 64 KB | 4 KB | 5.5 KB Note | R5F104AE | R5F104BE | R5F104CE | R5F104EE |
| 48 KB | 4 KB | 5.5 KB Note | R5F104AD | R5F104BD | R5F104CD | R5F104ED |
| 32 KB | 4 KB | 4 KB | R5F104AC | R5F104BC | R5F104CC | R5F104EC |
| 16 KB | 4 KB | 2.5 KB | R5F104AA | R5F104BA | R5F104CA | R5F104EA |

| Flash ROM | Data flash | RAM | RL78/G14 | | | |
|---|---|---|---|---|---|---|
| | | | 44 pins | 48 pins | 52 pins | 64 pins |
| 512 KB | 8 KB | 48 KB Note | — | R5F104GL | — | R5F104LL |
| 384 KB | 8 KB | 32 KB | — | R5F104GK | — | R5F104LK |
| 256 KB | 8 KB | 24 KB Note | R5F104FJ | R5F104GJ | R5F104JJ | R5F104LJ |
| 192 KB | 8 KB | 20 KB | R5F104FH | R5F104GH | R5F104JH | R5F104LH |
| 128 KB | 8 KB | 16 KB | R5F104FG | R5F104GG | R5F104JG | R5F104LG |
| 96 KB | 8 KB | 12 KB | R5F104FF | R5F104GF | R5F104JF | R5F104LF |
| 64 KB | 4 KB | 5.5 KB Note | R5F104FE | R5F104GE | R5F104JE | R5F104LE |
| 48 KB | 4 KB | 5.5 KB Note | R5F104FD | R5F104GD | R5F104JD | R5F104LD |
| 32 KB | 4 KB | 4 KB | R5F104FC | R5F104GC | R5F104JC | R5F104LC |
| 16 KB | 4 KB | 2.5 KB | R5F104FA | R5F104GA | — | — |

| Flash ROM | Data flash | RAM | RL78/G14 | |
|---|---|---|---|---|
| | | | 80 pins | 100 pins |
| 512 KB | 8 KB | 48 KB Note | R5F104ML | R5F104PL |
| 384 KB | 8 KB | 32 KB | R5F104MK | R5F104PK |
| 256 KB | 8 KB | 24 KB Note | R5F104MJ | R5F104PJ |
| 192 KB | 8 KB | 20 KB | R5F104MH | R5F104PH |
| 128 KB | 8 KB | 16 KB | R5F104MG | R5F104PG |
| 96 KB | 8 KB | 12 KB | R5F104MF | R5F104PF |

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/5)

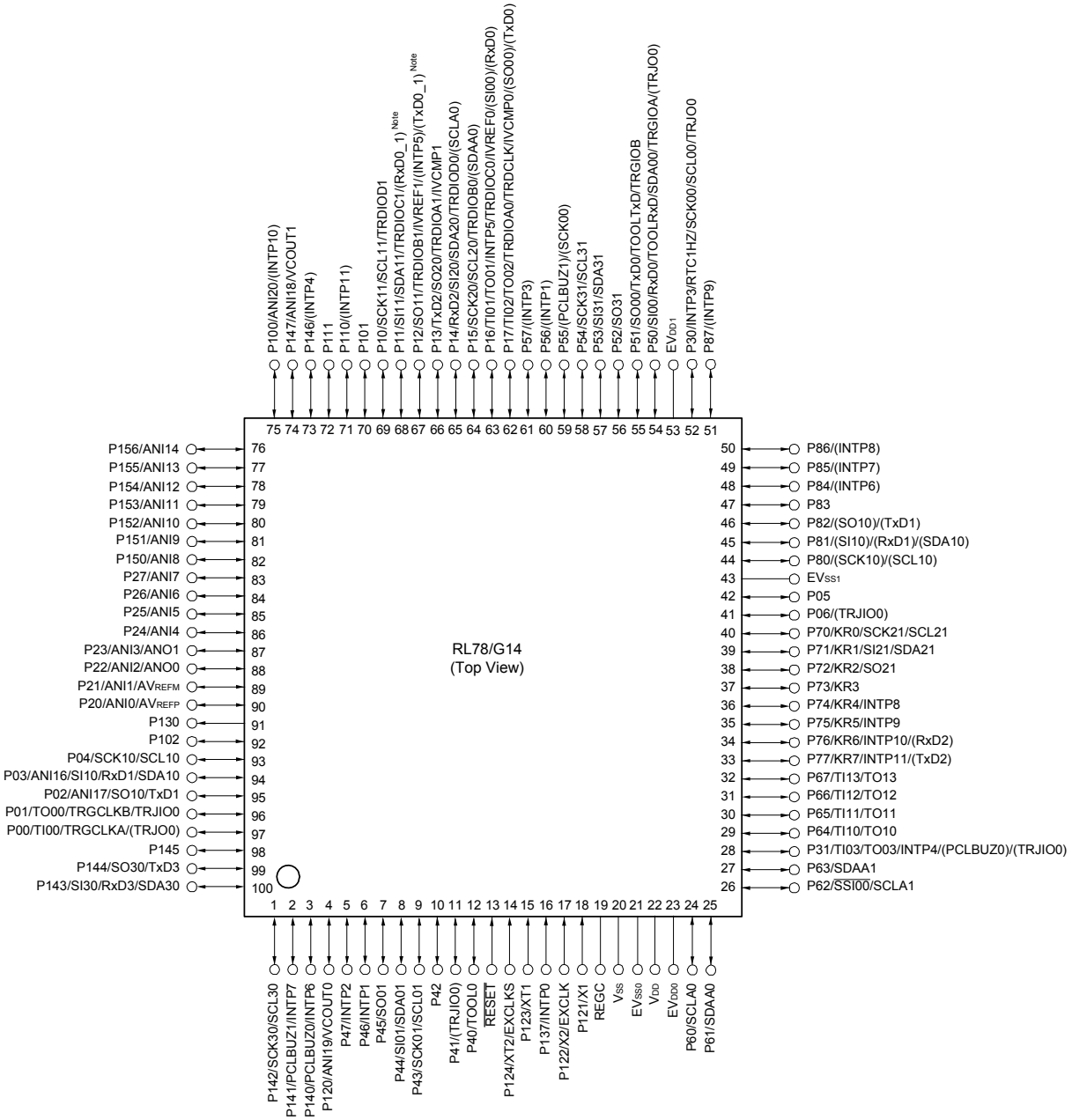
| Pin count | Package | Fields of Application Note | Ordering Part Number |
|---|---|---|---|
| 40 pins | 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch) | A | R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0<br>R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0 |
| | | D | R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0<br>R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0 |
| | | G | R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0<br>R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0 |
| 44 pins | 44-pin plastic LQFP (10 × 10, 0.8 mm pitch) | A | R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0<br>R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0 |
| | | D | R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0<br>R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0 |
| | | G | R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0<br>R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0 |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3.10 100-pin products

• 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)




**Note** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.**

**Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).**

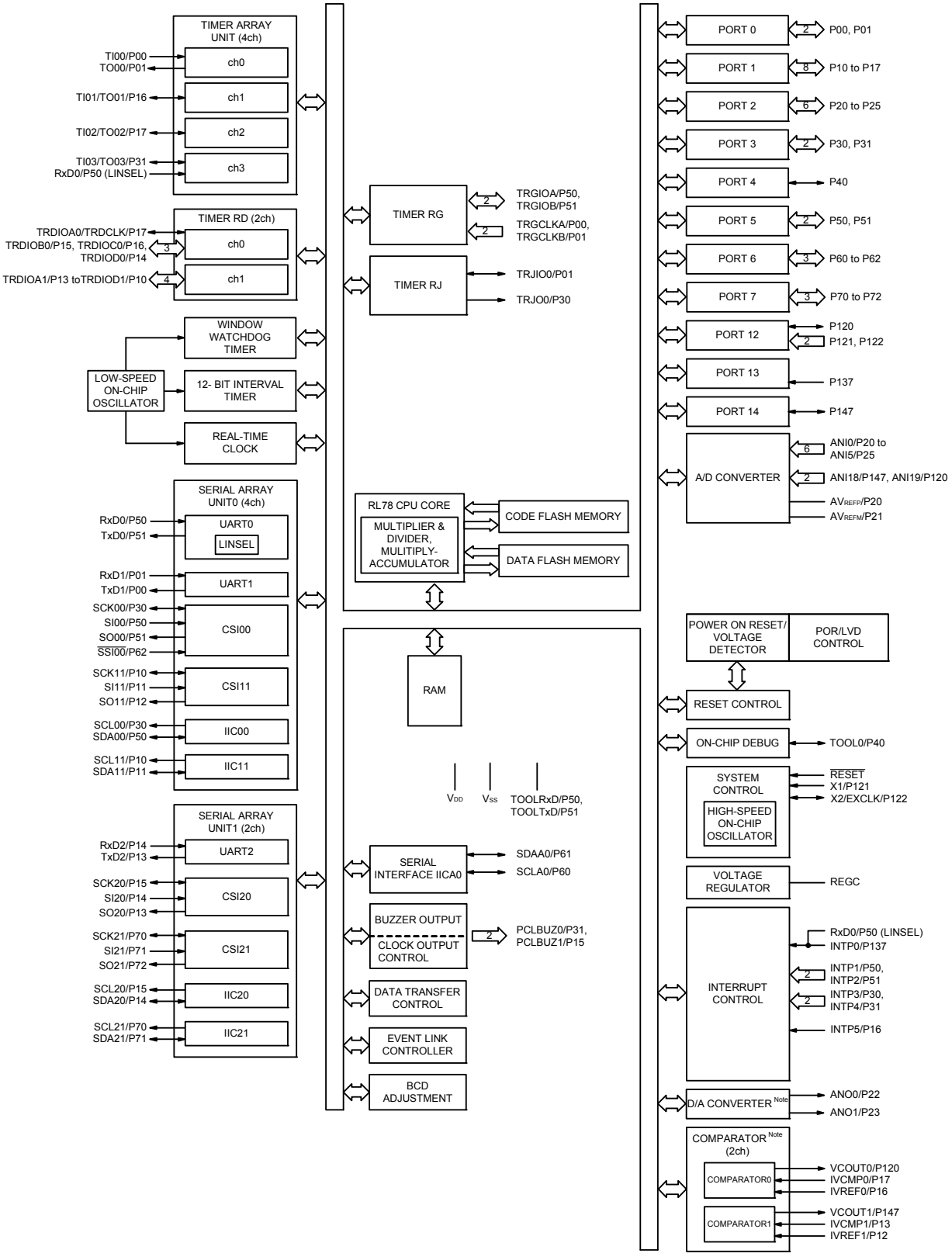
**Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

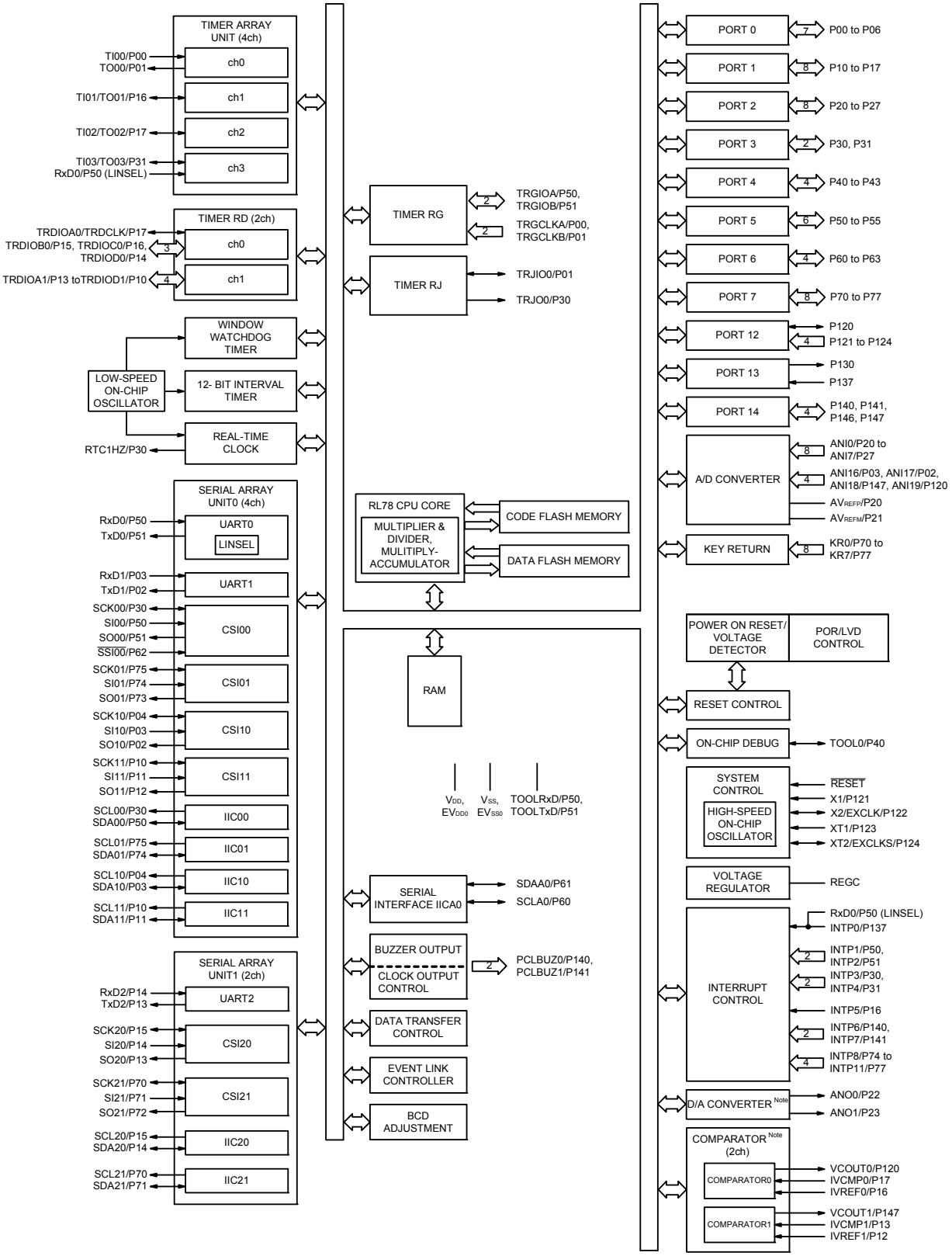
**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

## 1.5.3 36-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.8 64-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = F, G) | R5F104Bx (x = F, G) | R5F104Cx (x = F, G) | R5F104Ex (x = F to H) |
| Code flash memory (KB) | | 96 to 128 | 96 to 128 | 96 to 128 | 96 to 192 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 16 Note | 12 to 16 Note | 12 to 16 Note | 12 to 20 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | — | | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | — | | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 26 | 28 | 32 | 36 |
| | CMOS I/O | 21 | 22 | 26 | 28 |
| | CMOS input | 3 | 3 | 3 | 5 |
| | CMOS output | — | — | — | — |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 3 | 3 | 3 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |

(**Note** is listed on the next page.)

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 44-pin<br>R5F104Fx<br>(x = F to H, J) | 48-pin<br>R5F104Gx<br>(x = F to H, J) | 52-pin<br>R5F104Jx<br>(x = F to H, J) | 64-pin<br>R5F104Lx<br>(x = F to H, J) |
|---|---|---|---|---|---|
| Code flash memory (KB) | | 96 to 256 | 96 to 256 | 96 to 256 | 96 to 256 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 24 Note | 12 to 24 Note | 12 to 24 Note | 12 to 24 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 40 | 44 | 48 | 58 |
| | CMOS I/O | 31 | 34 | 38 | 48 |
| | CMOS input | 5 | 5 | 5 | 5 |
| | CMOS output | — | 1 | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 | 4 | 4 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 14 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | |

(**Note** is listed on the next page.)

## 2.3.2 Supply current characteristics

### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.1 | 8.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.1 | 8.7 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.1 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.1 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 6.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 6.9 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.3 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.6 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 2.0 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.8 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | mA |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

(**Notes** and **Remarks** are listed on the next page.)

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.4 | 10.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.4 | 10.2 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.0 | 9.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.0 | 9.6 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.2 | 7.8 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 7.8 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.4 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.4 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.0 | 5.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.0 | 5.3 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.4 | 2.3 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.4 | 2.3 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.9 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 6.2 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.4 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 6.2 | |
| | | | | | | Resonator connection | | 3.6 | 6.4 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.6 | |
| | | | | | | Resonator connection | | 2.2 | 3.7 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.6 | |
| | | | | | | Resonator connection | | 2.2 | 3.7 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.3 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 2.2 | |
| | | | | | | Resonator connection | | 1.2 | 2.3 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.9 | 7.1 | µA |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.1 | |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.1 | 8.8 | |
| | | | | | | Resonator connection | | 5.1 | 8.8 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |

(**Notes** and **Remarks** are listed on the next page.)

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 2.60 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 2.60 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 2.03 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 2.03 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 1.50 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 1.50 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 800 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 800 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 450 | 755 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 450 | 755 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.69 | mA |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.69 | |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 610 | µA |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 610 | |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.31 | | µA |
| | | | | | Resonator connection | | 0.50 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.38 | 0.76 | |
| | | | | | Resonator connection | | 0.57 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.47 | 3.59 | |
| | | | | | Resonator connection | | 0.70 | 3.78 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.80 | 6.20 | |
| | | | | | Resonator connection | | 1.00 | 6.39 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.65 | 10.56 | |
| | | | | | Resonator connection | | 1.84 | 10.75 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | | µA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.59 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.42 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.03 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.39 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$, $t_{TDIL}$ | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | | 3/$f_{CLK}$ | | | ns |
| Timer RD forced cutoff signal input low-level width | $t_{TDSIL}$ | P130/INTP0 | 2MHz < $f_{CLK}$ ≤ 32 MHz | 1 | | | µs |
| | | | $f_{CLK}$ ≤ 2 MHz | 1/$f_{CLK}$ + 1 | | | |
| Timer RG input high-level width, low-level width | $t_{TGIH}$, $t_{TGIL}$ | TRGIOA, TRGIOB | | 2.5/$f_{CLK}$ | | | ns |
| TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 1 | | | µs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

### (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 245 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

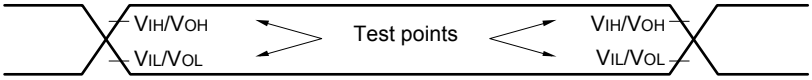
**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

## 3.5 Peripheral Functions Characteristics

AC Timing Test Points




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/12 Note 2 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |

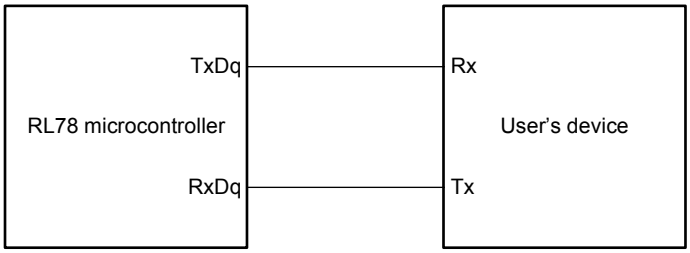
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 1.3 Mbps

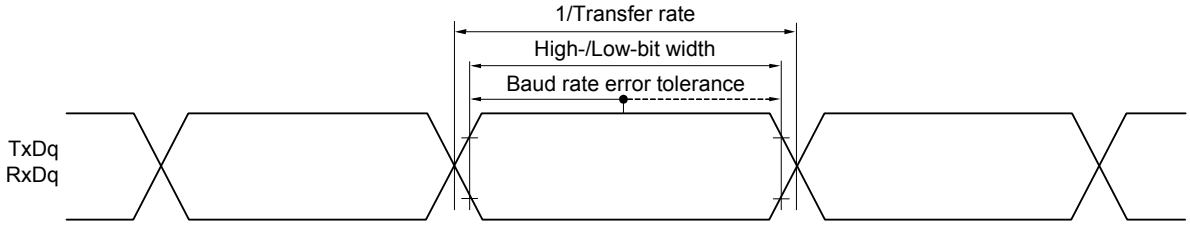
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(3/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD}$ = $EV_{DD1}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (-) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**Note 4.** When reference voltage (-) = $V_{SS}$, the MAX. values are as follows.

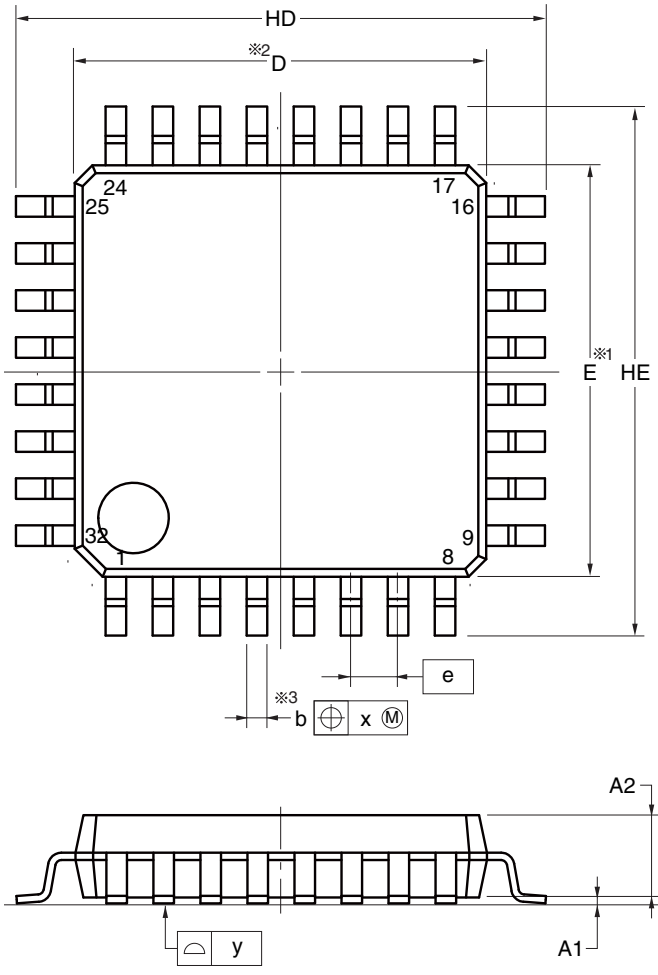
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = $AV_{REFM}$.

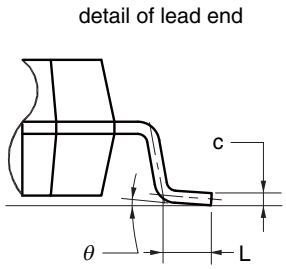
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

R5F104BAAFP, R5F104BCAFP, R5F104BDAFP, R5F104BEAFP, R5F104BFAFP, R5F104BGAFP
R5F104BADFP, R5F104BCDFP, R5F104BDDFP, R5F104BEDFP, R5F104BFDFP, R5F104BGDFP
R5F104BAGFP, R5F104BCGFP, R5F104BDGFP, R5F104BEGFP, R5F104BFGFP, R5F104BGGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP32-7x7-0.80 | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.10 |
| E | 7.00±0.10 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | 0.37±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

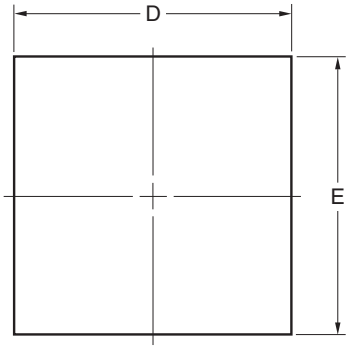
**NOTE**

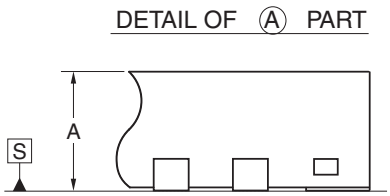
1.Dimensions "※1" and "※2" do not include mold flash.

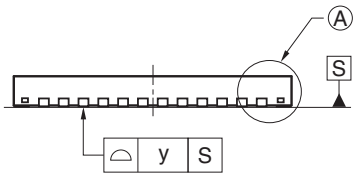
2.Dimension "※3" does not include trim offset.

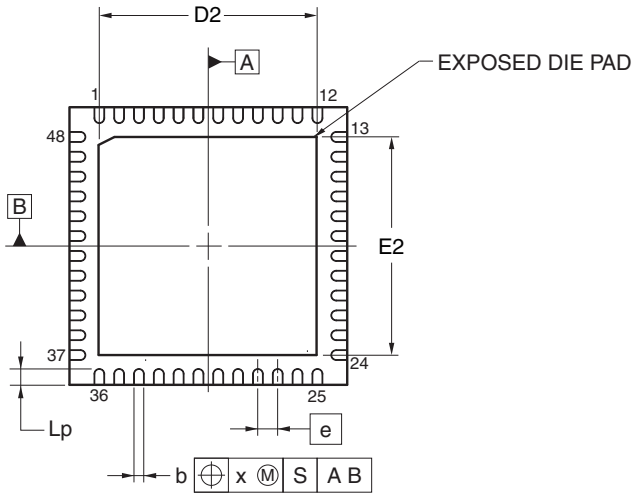
R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA, R5F104GHANA, R5F104GJANA
R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA, R5F104GHDNA, R5F104GJDNA
R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA, R5F104GHGNA, R5F104GJGNA
R5F104GKANA, R5F104GLANA
R5F104GKGNA, R5F104GLGNA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-5 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 5.45 | 5.50 | 5.55 | 5.45 | 5.50 | 5.55 |