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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-WFLGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104cfala-u0

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 1.3.2 32-pin products

• 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

#### Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 $\mu\text{F}).$

- Remark 1. For pin identification, see 1.4 Pin Identification.
- **Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).
- Remark 3. It is recommended to connect an exposed die pad to Vss.



## 1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		SCK00, SCK01, SCK10,:	Serial clock input/output
ANO0, ANO1:	Analog output	SCK11, SCK20, SCK21,	
AVREFM:	A/D converter reference	SCK30, SCK31	
	potential (– side) input	SCLA0, SCLA1,:	Serial clock input/output
AVREFP:	A/D converter reference	SCL00, SCL01, SCL10, SCL11,:	Serial clock output
	potential (+ side) input	SCL20, SCL21, SCL30,	
EVDD0, EVDD1:	Power supply for port	SCL31	
EVsso, EVss1:	Ground for port	SDAA0, SDAA1, SDA00,:	Serial data input/output
EXCLK:	External clock input	SDA01, SDA10, SDA11,	
	(main system clock)	SDA20, SDA21, SDA30,	
EXCLKS:	External clock input	SDA31	
	(subsystem clock)	SI00, SI01, SI10, SI11,:	Serial data input
INTP0 to INTP11:	External interrupt input	SI20, SI21, SI30, SI31	
IVCMP0, IVCMP1:	Comparator input	SO00, SO01, SO10,:	Serial data output
IVREF0, IVREF1:	Comparator reference input	SO11, SO20, SO21,	
KR0 to KR7:	Key return	SO30, SO31	
P00 to P06:	Port 0	SSI00:	Serial interface chip select input
P10 to P17:	Port 1	TI00 to TI03,:	Timer input
P20 to P27:	Port 2	TI10 to TI13	
P30, P31:	Port 3	TO00 to TO03,:	Timer output
P40 to P47:	Port 4	TO10 to TO13, TRJO0	
P50 to P57:	Port 5	TOOL0:	Data input/output for tool
P60 to P67:	Port 6	TOOLRxD, TOOLTxD:	Data input/output for external device
P70 to P77:	Port 7	TRDCLK, TRGCLKA,:	Timer external input clock
P80 to P87:	Port 8	TRGCLKB	
P100 to P102:	Port 10	TRDIOA0, TRDIOB0,:	Timer input/output
P110, P111:	Port 11	TRDIOC0, TRDIOD0,	
P120 to P124:	Port 12	TRDIOA1, TRDIOB1,	
P130, P137:	Port 13	TRDIOC1, TRDIOD1,	
P140 to P147:	Port 14	TRGIOA, TRGIOB, TRJIO0	
P150 to P156:	Port 15	TxD0 to TxD3:	Transmit data
PCLBUZ0, PCLBUZ1:	Programmable clock	VCOUT0, VCOUT1:	Comparator output
	output/buzzer output	Vdd:	Power supply
REGC:	Regulator capacitance	Vss:	Ground
RESET:	Reset	X1, X2:	Crystal oscillator (main system clock)
RTC1HZ:	Real-time clock correction	XT1, XT2:	Crystal oscillator (subsystem clock)
	clock		
	(1 Hz) output		



[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

# Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

			(1/2)			
		80-pin	100-pin			
	Item	R5F104Mx	R5F104Px			
		(x = K, L)	(x = K, L)			
Code flash men	nory (KB)	384 to 512	384 to 512			
Data flash mem	ory (KB)	8	8			
RAM (KB)		32 to 48 <sup>Note</sup>	32 to 48 Note			
Address space		1 MB				
Main system	High-speed system	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)				
clock	clock	HS (high-speed main) mode: 1 to 20 MHz (VDD = 2.7 to 5.5 V),				
		HS (high-speed main) mode: 1 to 16 MHz (VDD = 2.4 to 5.5 V),				
		LS (low-speed main) mode: 1 to 8 MHz (VD	DD = 1.8  to  5.5  V),			
		LV (low-voltage main) mode: 1 to 4 MHz (Vc	od = 1.6 to 5.5 V)			
	High-speed on-chip	HS (high-speed main) mode: 1 to 32 MHz (V	/DD = 2.7 to 5.5 V),			
	oscillator clock (fiH)	HS (high-speed main) mode: 1 to 16 MHz (V	′DD = 2.4 to 5.5 V),			
		LS (low-speed main) mode: 1 to 8 MHz (VD	D = 1.8  to  5.5  V),			
		LV (low-voltage main) mode: 1 to 4 MHz (VD	D = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem c	lock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): VDD = 1.6 to 5.5 V				
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 ba	nks)			
Minimum instruction execution time		$0.03125 \ \mu s$ (High-speed on-chip oscillator closed)	ck: fiн = 32 MHz operation)			
		0.05 $\mu$ s (High-speed system clock: fMX = 20 M	Hz operation)			
		30.5 $\mu$ s (Subsystem clock: fsub = 32.768 kHz	operation)			
Instruction set		Data transfer (8/16 bits)				
		Adder and subtractor/logical operation (8/16 bits)				
		• Multiplication (8 bits $\times$ 8 bits, 16 bits $\times$ 16 bits), Division (16 bits $\div$ 16 bits, 32 bits $\div$ 32 bits)				
		• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)				
	[	• Rotate, barrel sniπ, and bit manipulation (Se	t, reset, test, and Boolean operation), etc.			
I/O port	Total	74	92			
	CMOS I/O	64	82			
	CMOS input	5	5			
	CMOS output	1	1			
	N-ch open-drain I/O (6 V tolerance)	4	4			
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer	RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel				
	Real-time clock	1 channel				
	(RTC)					
	12-bit interval timer	1 channel				
	Timer output	Timer outputs: 18 channels				
		PWM outputs: 12 channels				
	RTC output	1 • 1 Hz (subsystem clock: fsub = 32.768 kHz)				

Note

In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

Items	Symbol	Conditi	ons		MIN.	TYP.	MAX.	Unit
Input leakage cur- rent, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVDD0				1	μA
	Ilih2	P20 to P27, P137, P150 to P156, RESET	VI = VDD				1	μA
Input leakage current, low	Ilih3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VDD In input port or external clock input				1	μA
				In resonator con- nection			10	μA
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVsso			-1	μΑ	
	ILIL2	P20 to P27, P137, P150 to P156, RESET	VI = VSS			-1	μA	
	Ililis	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VSS	In input port or external clock input			-1	μA
				In resonator con- nection			-10	μA
On-chip pull-up resistance	Ru	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVsso	, In input port	10	20	100	kΩ

(TA = -40 to +85°C, 1.6 V  $\leq$  EVDD0 = EVDD1  $\leq$  VDD  $\leq$  5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/5)

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



# 2.3.2 Supply current characteristics

## (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit	
Supply	IDD1	01 Operat- HS (high-speed main		fносо = 64 MHz,	Basic	VDD = 5.0 V		2.4		mA	
current		ing mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4			
NOLE I				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.1			
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1			
			HS (high-speed main)	fносо = 64 MHz,	Normal	VDD = 5.0 V		5.1	8.7	mA	
			mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		5.1	8.7		
				fносо = 32 MHz,	Normal	VDD = 5.0 V		4.8	8.1		
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		4.8	8.1		
				fносо = 48 MHz,	Normal	VDD = 5.0 V		4.0	6.9		
				fiH = 24 MHz Note 3	operation	VDD = 3.0 V		4.0	6.9		
		fносо = 24 MHz,	Normal	VDD = 5.0 V		3.8	6.3				
				fiH = 24 MHz Note 3	operation	VDD = 3.0 V		3.8	6.3		
				fносо = 16 MHz, fiн = 16 MHz <sup>Note 3</sup>	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fiH = 8 MHz <sup>Note 3</sup>	Normal operation	VDD = 3.0 V		1.3	2.0	mA	
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main)	fносо = 4 MHz,	Normal	VDD = 3.0 V		1.3	1.8	mA	
			mode Note 5	fiH = 4 MHz Note 3	operation	VDD = 2.0 V		1.3	1.8		
		HS (high-speed main)	fmx = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V	Normal	Square wave input		3.3	5.3	mA		
		mode Note 5		operation	Resonator connection		3.4	5.5			
				f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		3.3	5.3	-	
						Resonator connection		3.4	5.5		
				f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fmx = 10 MHz <sup>Note 2</sup> ,	Normal	Square wave input		2.0	3.1		
				VDD = 3.0 V	operation	Resonator connection		2.1	3.2		
			LS (low-speed main)	fmx = 8 MHz Note 2,	Normal	Square wave input		1.2	1.9	mA	
			mode Note 5	VDD = 3.0 V	operation	Resonator connection		1.2	2.0		
				fmx = 8 MHz Note 2,	Normal	Square wave input		1.2	1.9		
				VDD = 2.0 V	operation	Resonator connection		1.2	2.0		
			Subsystem clock	fsue = 32.768 kHz Note 4	Normal	Square wave input		4.7	6.1	μΑ	
			operation	TA = -40°C	operation	Resonator connection		4.7	6.1		
				fsue = 32.768 kHz Note 4	Normal	Square wave input		4.7	6.1		
			TA = +25°C	operation	Resonator connection		4.7	6.1			
			fsue = 32.768 kHz Note 4	Normal	Square wave input		4.8	6.7			
		· · · · · · · · · · · · · · · · · · ·	TA = +50°C	operation	Resonator connection		4.8	6.7			
			fs T	fsub = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = +70°C	Normal	Square wave input		4.8	7.5		
					operation	Resonator connection		4.8	7.5		
					fsuB = 32.768 kHz Note 4	e 4 Normal	Square wave input		5.4	8.9	
				T <sub>A</sub> = +85°C	operation	Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)





Parameter	Symbol	Cond	litions	HS (high-spee mode	d main)	LS (low-speed mode	LS (low-speed main) mode		LV (low-voltage main) mode	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle	tксү2	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	20 MHz < fмск	8/fмск		_		_		ns
time Note 5			fмск ≤ 20 MHz	6/fмск		6/fмск		6/fмск		ns
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	16 MHz < fмск	8/fмск		_		_		ns
			fмск ≤ 16 MHz	6/fмск		6/fмск		6/fмск		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		6/fмск and 500		6/fмск and 500		6/fмск and 500		ns
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		6/fмск and 750		6/fмск and 750		6/fмск and 750		ns
		$1.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	6/fмск and 1500		6/fмск and 1500		6/fмск and 1500		ns	
		$1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		_		6/fмск and 1500		6/fмск and 1500		ns
SCKp high-/ tkH2, low-level width tkL2	$4.0~V \leq EV_{\text{DD0}} \leq 5.5~V$	tĸcy2/2 - 7		tkcy2/2 - 7		tксү2/2 - 7		ns		
	TKL2	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V$		tkcy2/2 - 8		tkcy2/2 - 8		tkcy2/2 - 8		ns
		$1.8~V \leq EV_{\text{DD0}} \leq 5.5~V$		tксү2/2 - 18		tксү2/2 - 18		tксү2/2 - 18		ns
		$1.7~V \leq EV_{DD0} \leq 5.5~V$		tксү2/2 - 66		tkcy2/2 - 66		tkcy2/2 - 66		ns
		$1.6~V \leq EV_{\text{DD0}} \leq 5.5~V$		_		tkcy2/2 - 66		tkcy2/2 - 66		ns
SIp setup time	tsik2	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns	
(to SCKp↑) Note 1		$1.8~V \leq EV_{\text{DD0}} \leq 5.5~V$	1/fмск + 30		1/fмск + 30		1/fмск + 30		ns	
		$1.7~V \leq EV_{DD0} \leq 5.5~V$	1/fмск + 40		1/fмск + 40		1/fмск + 40		ns	
		$1.6~V \leq EV_{DD0} \leq 5.5~V$			1/fмск + 40		1/fмск + 40		ns	
SIp hold time	tksi2	$1.8~V \leq EV_{\text{DD0}} \leq 5.5~V$		1/fмск + 31		1/fмск + 31		1/fмск + 31		ns
(from SCKp↑) Note 2		$1.7~V \leq EV_{DD0} \leq 5.5~V$		1/fмск + 250		1/fмск + 250		1/fмск + 250		ns
		$1.6~V \leq EV_{\text{DD0}} \leq 5.5~V$				1/fмск + 250		1/fмск + 250		ns
Delay time from SCKp↓ to	tkso2	C = 30 pF Note 4	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		2/fмск + 44		2/fмск + 110		2/fмск + 110	ns
SOp output Note 3			$2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		2/fмск + 75		2/fмск + 110		2/fмск + 110	ns
			$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		2/fмск + 100		2/fмск + 110		2/fмск + 110	ns
			$1.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		2/fмск + 220		2/fмск + 220		2/fмск + 220	ns
			$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		_		2/fмск + 220		2/fмск + 220	ns

# (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

### UART mode connection diagram (during communication at different potential)



#### UART mode bit width (during communication at different potential) (reference)





**Remark 1.**  $Rb[\Omega]$ : Communication line (TxDq) pull-up resistance,

Cb[F]: Communication line (TxDq) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.



#### CSI mode connection diagram (during communication at different potential



- **Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
- Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
- Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.





CSI mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





- Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

### (1) I<sup>2</sup>C standard mode

#### (TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: dat	$2.7~V \leq EV_{DD0} \leq 5.5~V$	250		250		250		ns
		$1.8 \text{ V} \leq EV_{\text{DD0}} \leq 5.5 \text{ V}$	250		250		250		ns
		$1.7 \text{ V} \le EV_{DD0} \le 5.5 \text{ V}$	250		250		250		ns
		$1.6~V \leq EV_{DD0} \leq 5.5~V$	-	_	250		250		ns
Data hold time (transmission) Note 2	thd: dat	$2.7~V \leq EV_{DD0} \leq 5.5~V$	0	3.45	0	3.45	0	3.45	μs
		$1.8~V \leq EV_{DD0} \leq 5.5~V$	0	3.45	0	3.45	0	3.45	μs
		$1.7 \text{ V} \leq EV_{DD0} \leq 5.5 \text{ V}$	0	3.45	0	3.45	0	3.45	μs
		$1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	—		0	3.45	0	3.45	μs
Setup time of stop condition	tsu: sto	$2.7~V \leq EV_{DD0} \leq 5.5~V$	4.0		4.0		4.0		μs
		$1.8 \text{ V} \leq EV_{\text{DD0}} \leq 5.5 \text{ V}$	4.0		4.0		4.0		μs
		$1.7 \text{ V} \leq EV_{DD0} \leq 5.5 \text{ V}$	4.0		4.0		4.0		μs
		$1.6 \text{ V} \leq EV_{\text{DD0}} \leq 5.5 \text{ V}$	-	_	4.0		4.0		μs
Bus-free time	<b>t</b> BUF	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	4.7		4.7		4.7		μs
		$1.8 \text{ V} \leq EV_{\text{DD0}} \leq 5.5 \text{ V}$	4.7		4.7		4.7		μs
		$1.7 \text{ V} \leq EV_{DD0} \leq 5.5 \text{ V}$	4.7		4.7		4.7		μs
		$1.6~V \leq EV_{DD0} \leq 5.5~V$	-	_	4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of the DE DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

- Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.
- **Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 k $\Omega$ 



## 2.6.4 Comparator

Parameter	Symbol	Cor	nditions	MIN.	TYP.	MAX.	Unit
Input voltage range	lvref					EVDD0 - 1.4	V
	lvcmp			-0.3		EVDD0 + 0.3	V
Output delay	td	V <sub>DD</sub> = 3.0 V Input slew rate > 50 mV/µs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode	e, window mode		0.76 Vdd		V
Low-electric-potential ref- erence voltage	VTW-	Comparator high-speed mode	e, window mode		0.24 VDD		V
Operation stabilization wait time	tсмр			100			μs
Internal reference voltage Note	VBGR	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{HS}$ (h	nigh-speed main) mode	1.38	1.45	1.50	V

#### (TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Note Not usable in LS (low-speed main) mode, LV (low-voltage main) mode, sub-clock operation, or STOP mode.

## 2.6.5 POR circuit characteristics

#### (TA = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	VPDR	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW		300			μs

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).





Items	Symbol	Condit	ons		MIN.	TYP.	MAX.	Unit
Input leakage cur- rent, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVDD0				1	μΑ
Items Input leakage cur- rent, high Input leakage current, low On-chip pull-up resistance	Ilih2	P20 to P27, P137, P150 to P156, RESET	VI = VDD				1	μA
	Іцнз	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VDD In input port or external clock input				1	μA
Input leakage				In resonator con- nection			10	μA
Items Input leakage cur- rent, high Input leakage current, low On-chip pull-up resistance	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVsso			-1	μΑ	
	Ilil2	P20 to P27, P137, P150 to P156, RESET	VI = VSS			-1	μA	
	Ilil3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VSS	In input port or external clock input			-1	μA
				In resonator con- nection			-10	μA
On-chip pull-up resistance	Ru	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	VI = EVsso,	, In input port	10	20	100	kΩ

(TA = -40 to +105°C, 2.4 V  $\leq$  EVDD0 = EVDD1  $\leq$  VDD  $\leq$  5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



- Note 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or Vss, EVss0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 3.** When high-speed system clock and subsystem clock are stopped.
- **Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- **Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below. HS (high-speed main) mode:  $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$  to 32 MHz
  - 2.4 V  $\leq$  VDD  $\leq$  5.5 V@1 MHz to 16 MHz
- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHoco: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsuB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C



- Note 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or Vss, EVss0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2. During HALT instruction execution by flash memory.
- **Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4. When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.<br/>HS (high-speed main) mode:  $2.7 \text{ V} \le \text{Vdd} \le 5.5 \text{ V}$ @1 MHz to 32 MHz
  - 2.4 V  $\leq$  VDD  $\leq$  5.5 V@1 MHz to 16 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3. fill: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



(				-,			(
Items	Symbol	Conditio	ons	MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	ttdih, ttdi∟	TRDIOA0, TRDIOA1, TRDIOE TRDIOC0, TRDIOC1, TRDIO	IRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, IRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1				ns
Timer RD forced cutoff signal	<b>t</b> TDSIL	P130/INTP0	$2MHz < fclk \le 32 MHz$	1			μs
input low-level width			fclk ≤ 2 MHz	1/fclк + 1			
Timer RG input high-level	tтgiн,	TRGIOA, TRGIOB		2.5/fclk			ns
width, low-level width	t⊤GIL						
TO00 to TO03,	fто	HS (high-speed main) mode	$4.0~V \leq EV_{\text{DD0}} \leq 5.5~V$			16	MHz
TO10 to TO13,			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}$			8	MHz
TRJIO0, TRJO0,			$2.4 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V}$			4	MHz
TRDIOC0, TRDIOC1,							
TRDIOD0, TRDIOD1,							
TRGIOA, TRGIOB							
output frequency							
PCLBUZ0, PCLBUZ1 output	<b>f</b> PCL	HS (high-speed main) mode	$4.0~V \leq EV_{DD0} \leq 5.5~V$			16	MHz
frequency			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}$			8	MHz
			$2.4 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V}$			4	MHz
Interrupt input high-level	tinth,	INTP0	$2.4~V \le V \text{DD} \le 5.5~V$	1			μs
width, low-level width	tintl	INTP1 to INTP11	$2.4~V \leq EV_{DD0} \leq 5.5~V$	1			μs
Key interrupt input low-level width	tĸĸ	KR0 to KR7	$2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	250			ns
RESET low-level width	trsl			10			μs

#### (TA = -40 to +105°C, 2.4 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)



# (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) (TA = -40 to +105°C, 2.4 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	<b>t</b> КСҮ1	tĸcy1 ≥ 4/fcLĸ	$2.7 \text{ V} \leq \text{Evdd0} \leq 5.5 \text{ V}$	250		ns
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	500		ns
SCKp high-/low-level width	igh-/low-level width tkH1, tkL1 $4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		5.5 V	tксү1/2 - 24		ns
		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү1/2 - 36		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү1/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	tsıĸı	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		66		ns
		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		66		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		113		ns
SIp hold time (from SCKp <sup>↑</sup> ) Note 2	tksii			38		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 3</sup>	tkso1	C = 30 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

- Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).
- **Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)
- Remark 2. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))





### CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
 Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.



## 3.10 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions MIN.		TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuinit	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	thd	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

- **Remark** tsuinit. The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
  - tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
  - tHD: How long to keep the TOOL0 pin at the low level from when the external resets end
    - (excluding the processing time of the firmware to control the flash memory)



## 4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA

R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA

R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA, R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09











Referance Symbol	Dimension in Millimeters						
	Min	Nom	Max				
D	5.95	6.00	6.05				
E	5.95	6.00	6.05				
А	0.70	0.75	0.80				
b	0.18	0.25	0.30				
е		0.50					
Lp	0.30	0.40	0.50				
x		—	0.05				
У	—		0.05				

ITEM		D2			E2			
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED DIE PAD VARIATIONS	А	4.45	4.50	4.55	4.45	4.50	4.55	

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