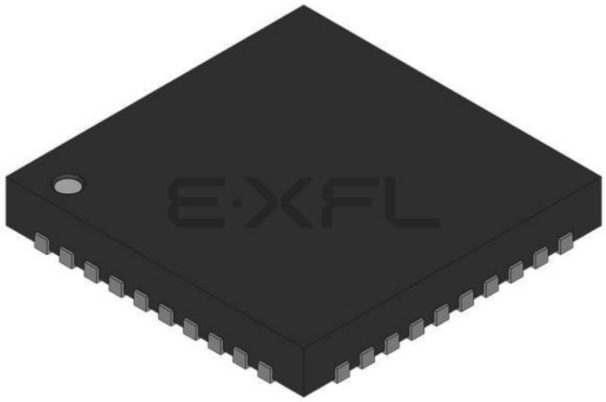

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What is "Embedded - Microcontrollers"?

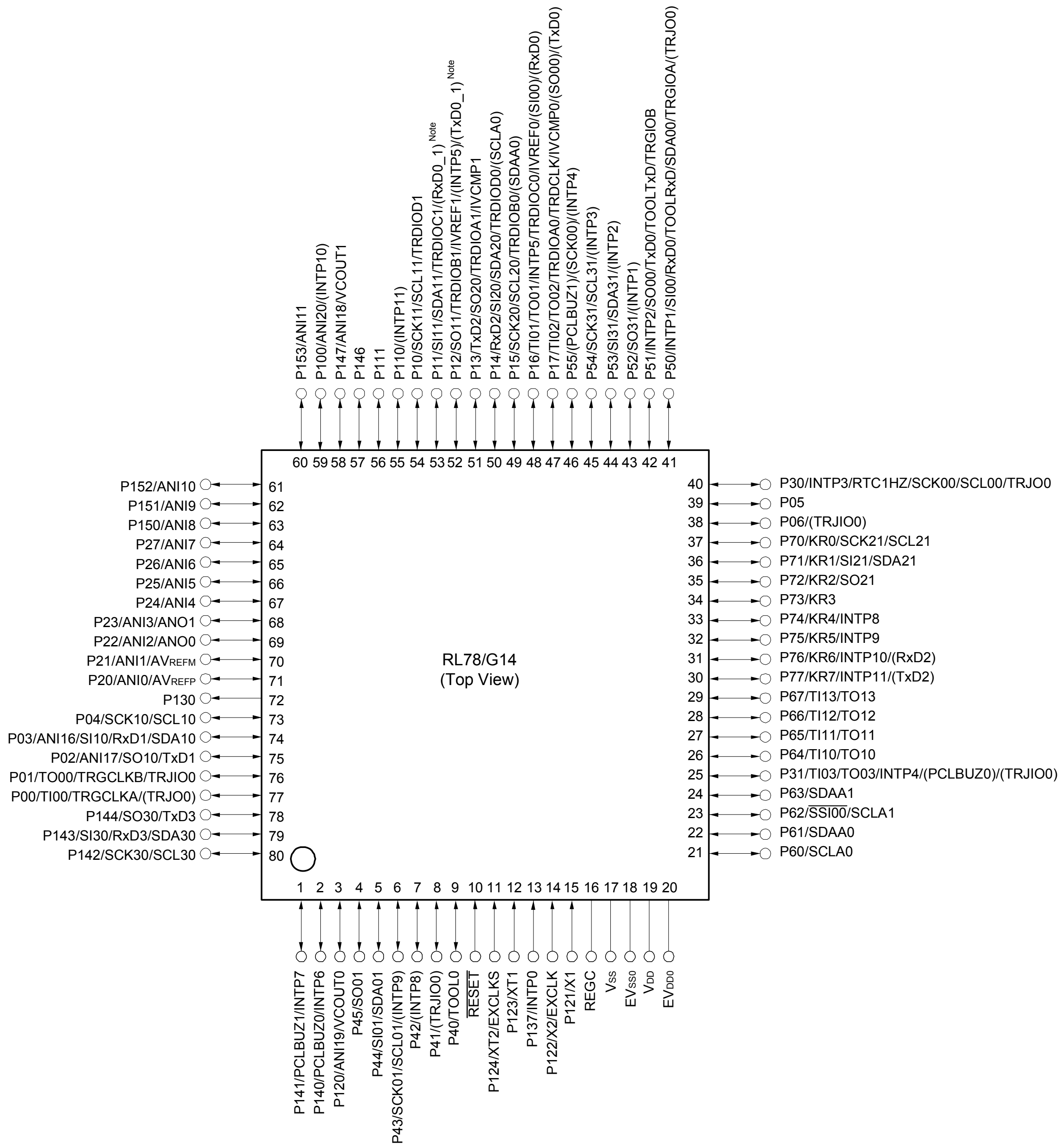
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ecana-u0

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

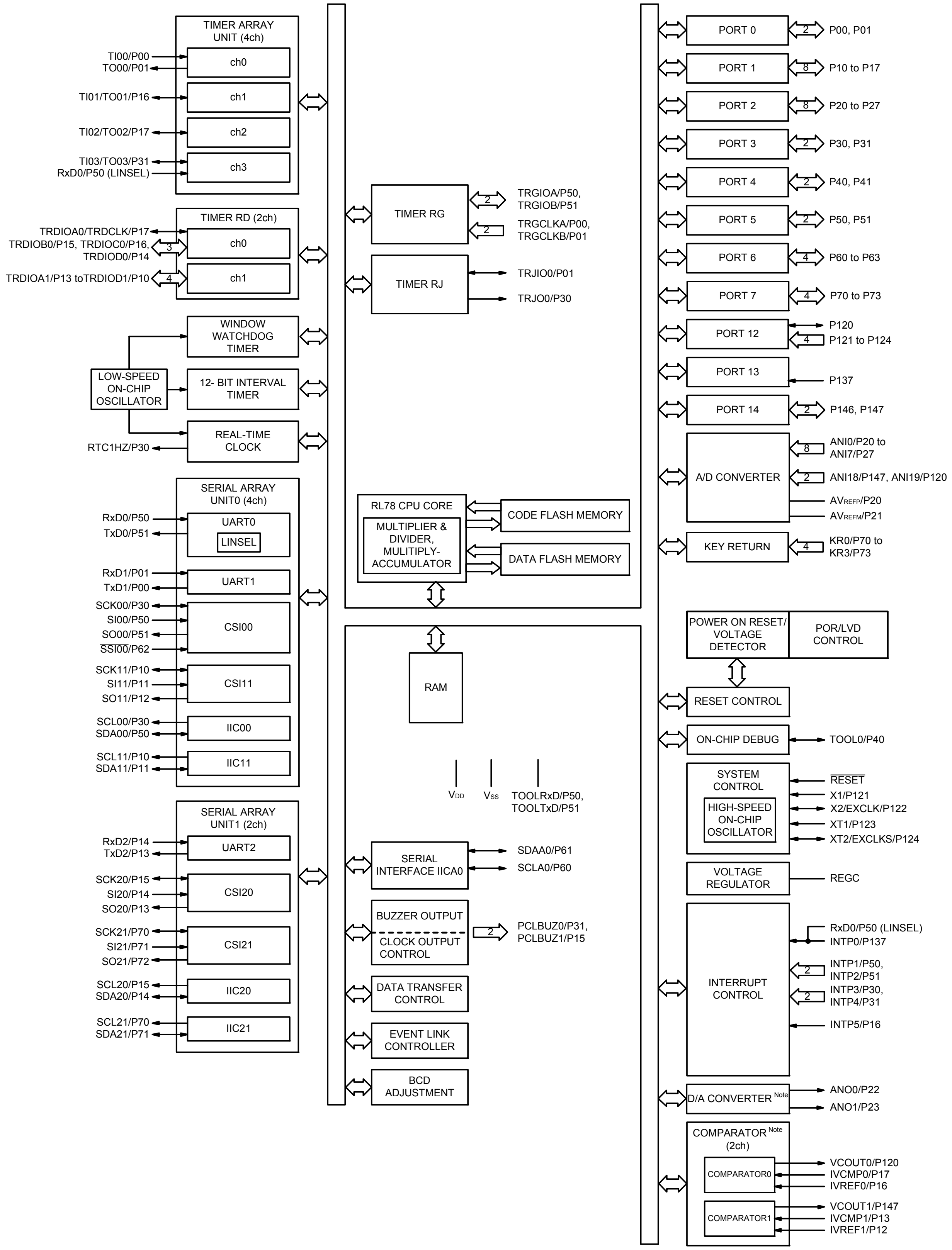
Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.5 44-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	16 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)

(**Note** is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[48-pin, 64-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		48-pin	64-pin
		R5F104Gx (x = K, L)	R5F104Lx (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 $^{\text{Note}}$	32 to 48 $^{\text{Note}}$
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	44	58
	CMOS I/O	34	48
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels	
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

(**Note** is listed on the next page.)

(2/2)

Item		48-pin	64-pin
		R5F104Gx (x = K, L)	R5F104Lx (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		10 channels	12 channels
D/A converter		2 channels	
Comparator		2 channels	
Serial interface		[48-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels	
	I^{2}C bus	1 channel	1 channel
Data transfer controller (DTC)		32 sources	33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9	
Vectored interrupt sources	Internal	24	24
	External	10	13
Key interrupt		6	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
	2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		ns
		1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		ns
SCKp low-level width	t_{KL1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 12		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 18		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns
		1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns

Note Use it with EV_{DD0} $\geq$ V_b.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

Operation of products rated “G: Industrial applications (T_A = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

Parameter	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	T_A = -40 to +85°C	T_A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V: ±1.0% @ T_A = -20 to +85°C ±1.5% @ T_A = -40 to -20°C 1.6 V ≤ V_{DD} < 1.8 V: ±5.0% @ T_A = -20 to +85°C ±5.5% @ T_A = -40 to -20°C	2.4 V ≤ V_{DD} ≤ 5.5 V: ±2.0% @ T_A = +85 to +105°C ±1.0% @ T_A = -20 to +85°C ±1.5% @ T_A = -40 to -20°C
Serial array unit	UART CSI: f_{CLK}/2 (16 Mbps supported), f_{CLK}/4 Simplified I^2C communication	UART CSI: f_{CLK}/4 Simplified I^2C communication
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fast mode
Voltage detector	• Rising: 1.67 V to 4.06 V (14 stages) • Falling: 1.63 V to 3.98 V (14 stages)	• Rising: 2.61 V to 4.06 V (8 stages) • Falling: 2.55 V to 3.98 V (8 stages)

Remark The electrical characteristics of products rated “G: Industrial applications (T_A = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to **3.1** to **3.10**.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147				8.5 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				80.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1}, and V_{SS} pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 32 MHz
$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

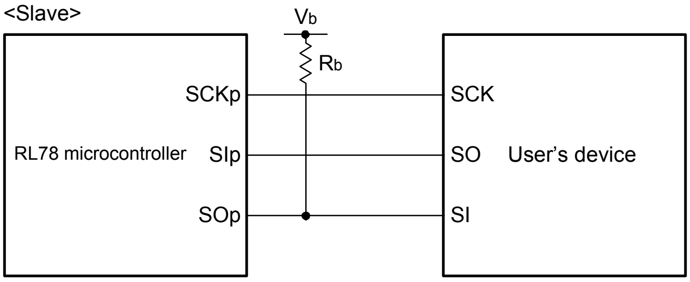
Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 2		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note 2		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-)= AVREFM
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI20	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±1.5	LSB
Analog input voltage	VAIN	ANI2 to ANI14		0		AVREFP	V
		Internal reference voltage output (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VBGR Note 4			V
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VTMPS25 Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

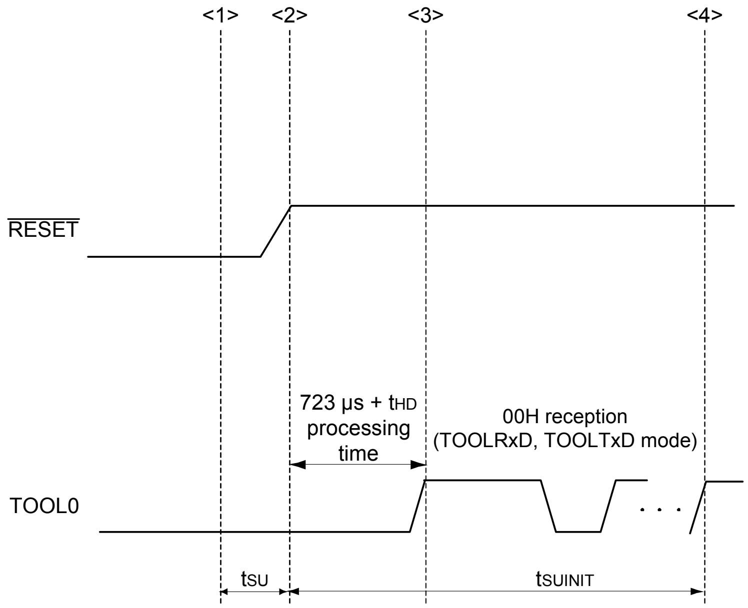
Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

3.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			µs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

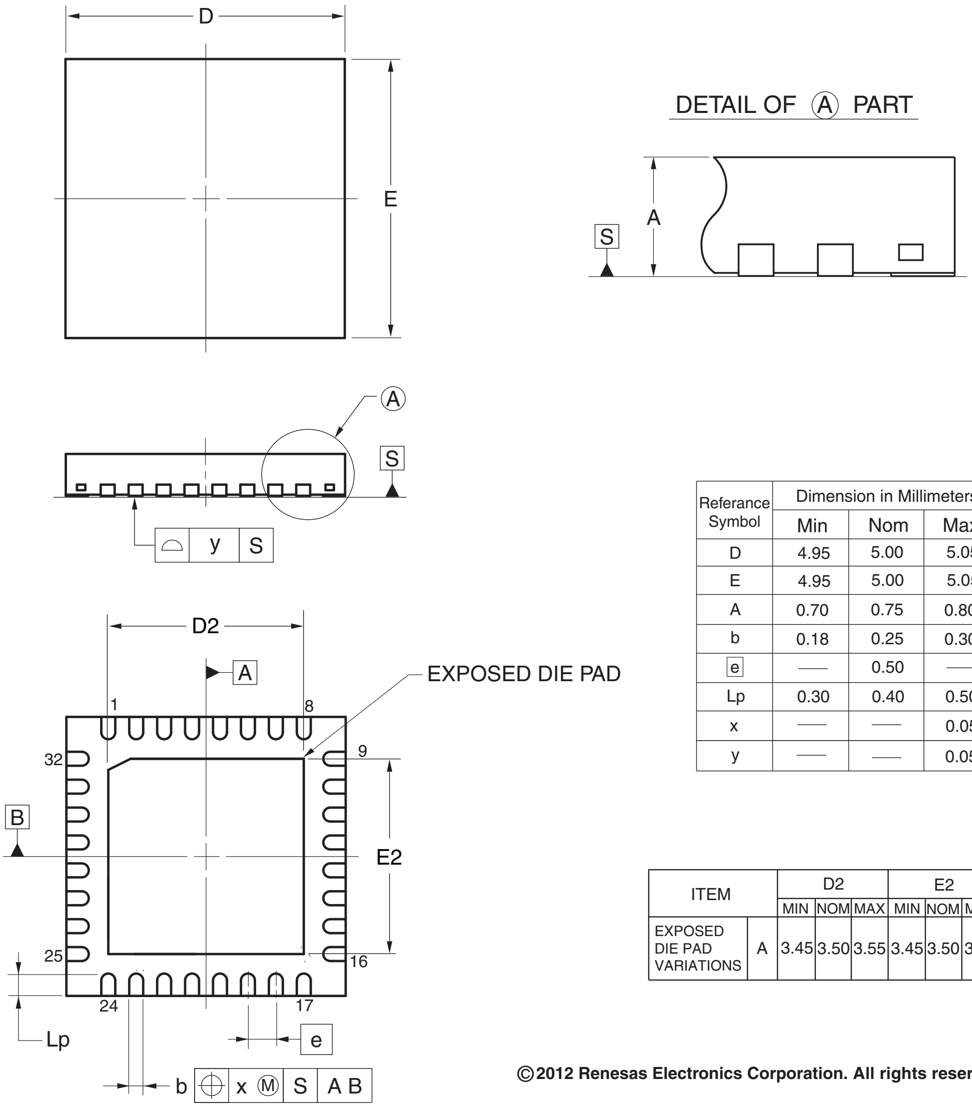
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4.2 32-pin products

R5F104BAANA, R5F104BCANA, R5F104BDANA, R5F104BEANA, R5F104BFANA, R5F104BGANA
R5F104BADNA, R5F104BCDNA, R5F104BDDNA, R5F104BEDNA, R5F104BFDNA, R5F104BGDNA
R5F104BAGNA, R5F104BCGNA, R5F104BDGNA, R5F104BEGNA, R5F104BFGNA, R5F104BGGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-4	0.06



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

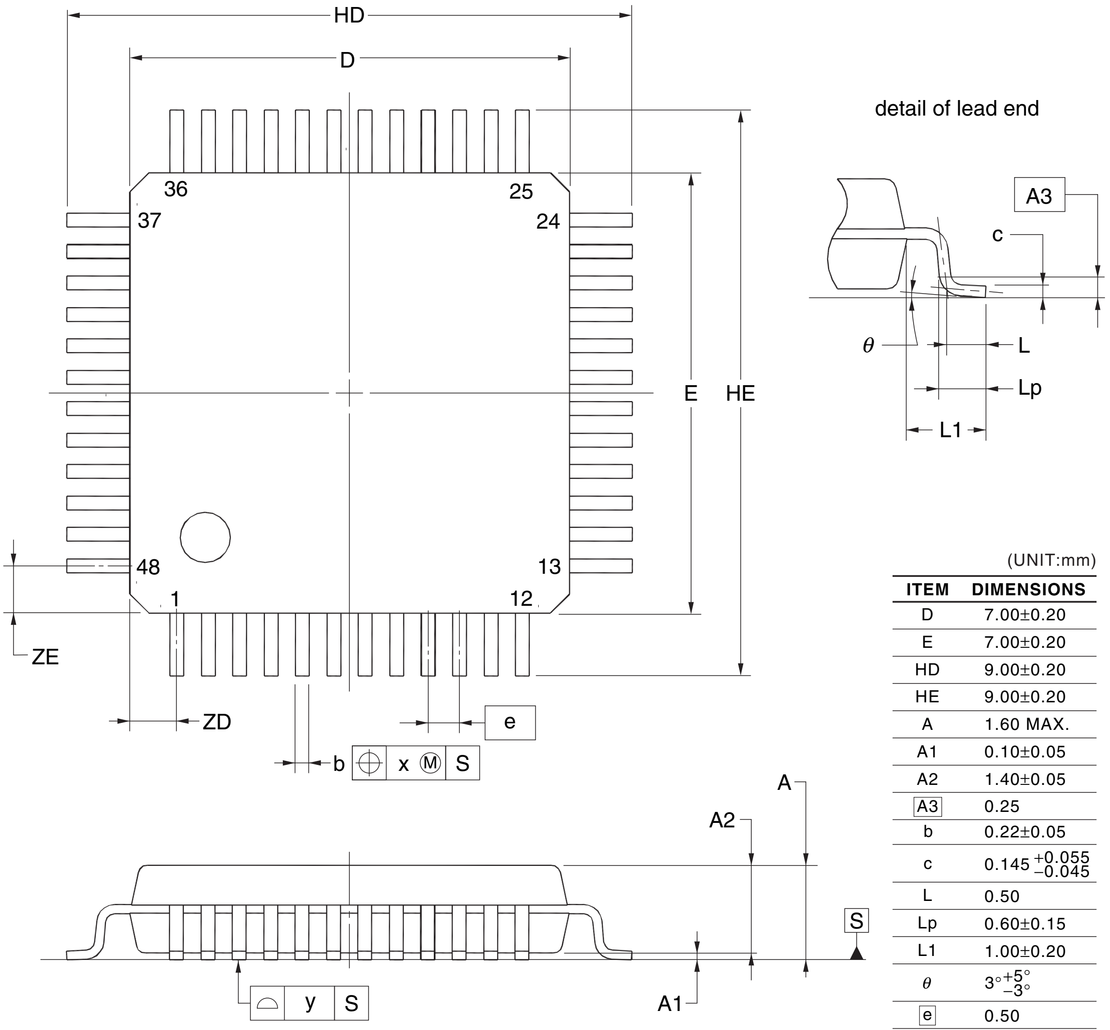
4.6 48-pin products

R5F104GAAFB, R5F104GCAFB, R5F104GDAFB, R5F104GEAFB, R5F104GFAFB, R5F104GGAFB, R5F104GHAFB, R5F104GJAFB

R5F104GADFB, R5F104GCDFB, R5F104GDDFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB, R5F104GHDFB, R5F104GJDFB

R5F104GAGFB, R5F104GCGFB, R5F104GDGFB, R5F104GEGFB, R5F104GFGFB, R5F104GGGFB, R5F104GHGFB, R5F104GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



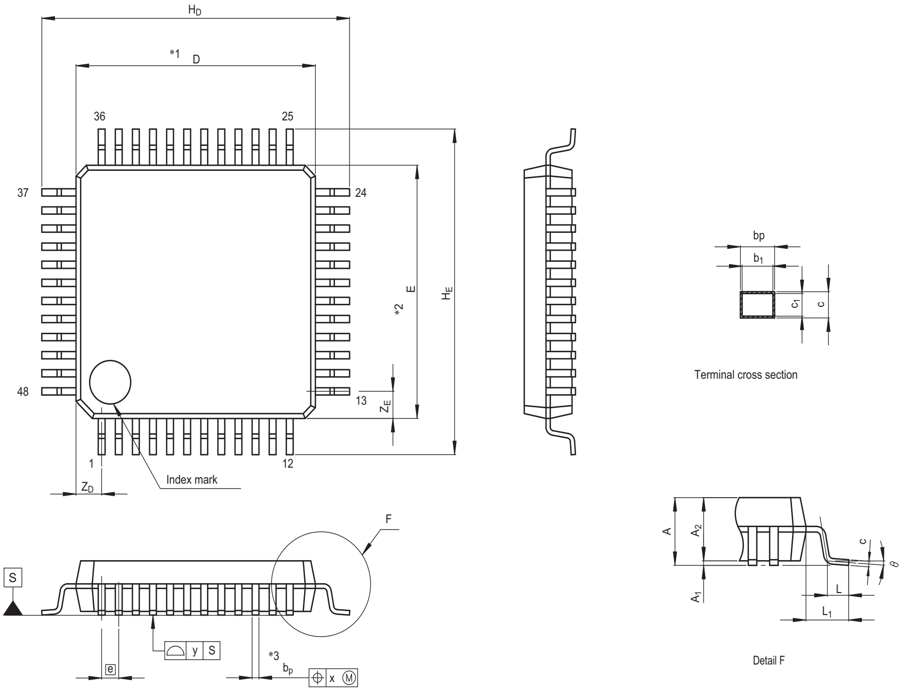
(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145\,^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}\,^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104GKAFB, R5F104GLAFB
R5F104GKGFB, R5F104GLGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—