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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104eeana-u0

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Pin count	Package	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0
			R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0
			R5F104GKAFB#30, R5F104GLAFB#30
			R5F104GKAFB#50, R5F104GLAFB#50
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GFDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0
			R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GFDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0
			R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0
			R5F104GKGFB#30, R5F104GLGFB#30
			R5F104GKGFB#50, R5F104GLGFB#50
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0
			R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0
			R5F104GKANA#U0, R5F104GLANA#U0
			R5F104GKANA#W0, R5F104GLANA#W0
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0
			R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0
			R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0
			R5F104GKGNA#U0, R5F104GLGNA#U0
			R5F104GKGNA#W0, R5F104GLGNA#W0
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0
			R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0
			R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0
			R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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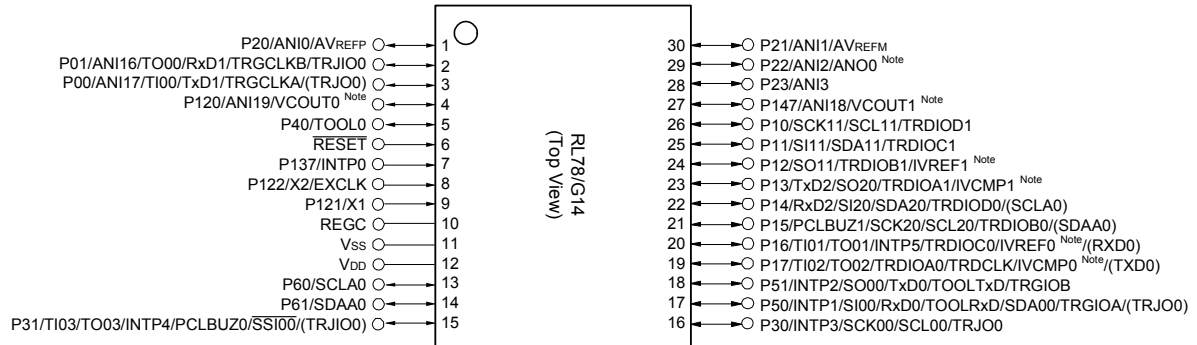| Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAFA#V0, R5F104LHAFA#V0, R5F104LJAFA#V0
			R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAFA#X0, R5F104LHAFA#X0, R5F104LJAFA#X0
			R5F104LKAFA#30, R5F104LLAFA#30
			R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFA#V0, R5F104LHDFA#V0, R5F104LJDFA#V0
			R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFA#X0, R5F104LHDFA#X0, R5F104LJDFA#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0
			R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0
			R5F104LKGFA#30, R5F104LLGFA#30
			R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0
			R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0
			R5F104LKAFB#30, R5F104LLAFB#30
			R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LFDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0
			R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LFDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0
			R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0
			R5F104LKGFB#30, R5F104LLGFB#30
			R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0
			R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0
			R5F104LKALA#U0, R5F104LLALA#U0
			R5F104LKALA#W0, R5F104LLALA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0
			R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0
			R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LFDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0
			R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LFDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0
			R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

1.3　Pin Configuration (Top View)

1.3.1　30-pin products

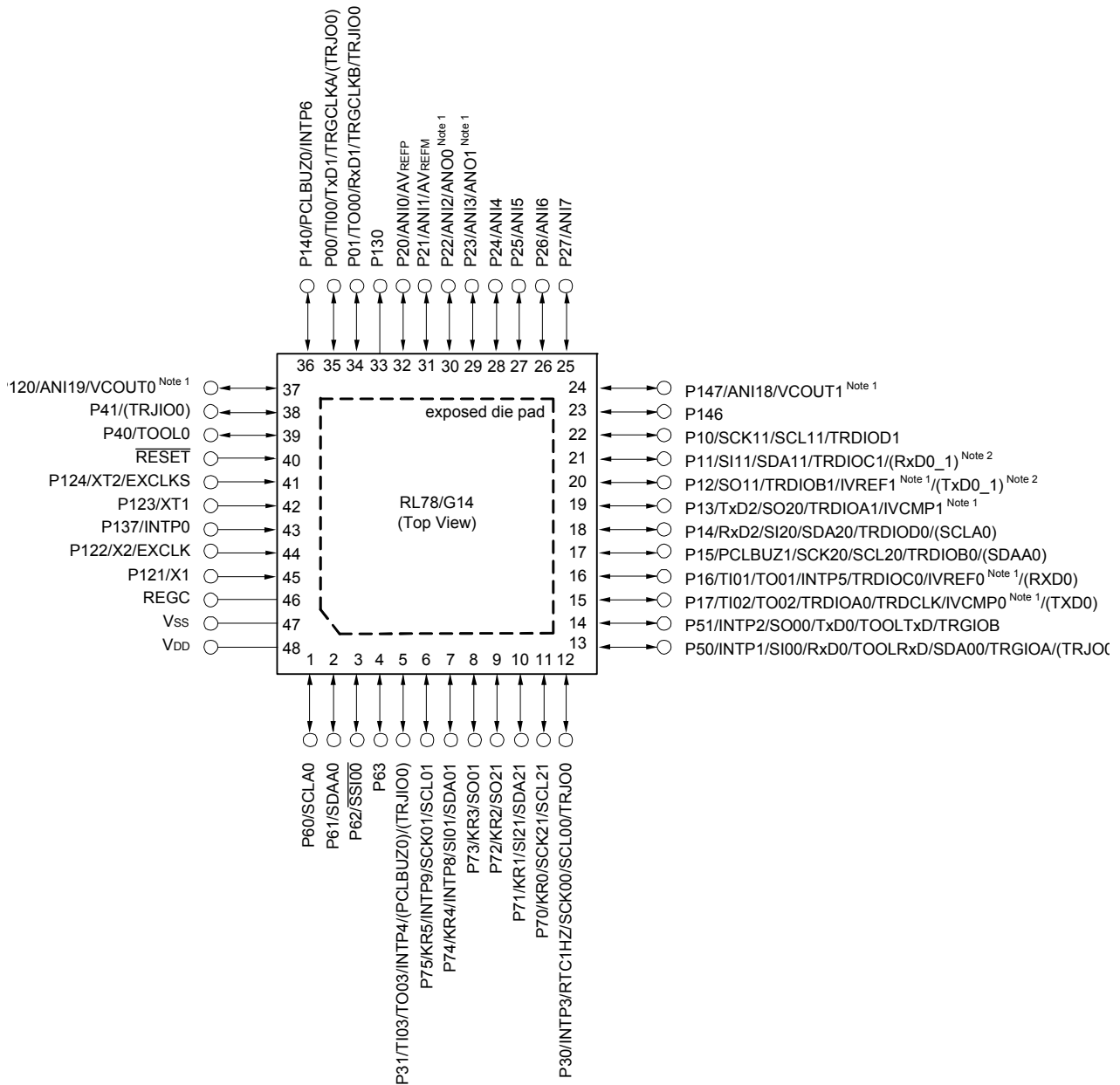• 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

Left side pins (1–15):

- P20/ANI0/AV$_{REFP}$ — 1
- P01/ANI16/TO00/RxD1/TRGCLKB/TRJIO0 — 2
- P00/ANI17/TI00/TxD1/TRGCLKA/(TRJO0) — 3
- P120/ANI19/VCOUT0 ^{Note} — 4
- P40/TOOL0 — 5
- RESET — 6
- P137/INTP0 — 7
- P122/X2/EXCLK — 8
- P121/X1 — 9
- REGC — 10
- V$_{SS}$ — 11
- V$_{DD}$ — 12
- P60/SCLA0 — 13
- P61/SDAA0 — 14
- P31/TI03/TO03/INTP4/PCLBUZ0/SSI00/(TRJIO0) — 15

Center: RL78/G14 (Top View)

Right side pins (16–30):

- 30 — P21/ANI1/AV$_{REFM}$
- 29 — P22/ANI2/ANO0 ^{Note}
- 28 — P23/ANI3
- 27 — P147/ANI18/VCOUT1 ^{Note}
- 26 — P10/SCK11/SCL11/TRDIOD1
- 25 — P11/SI11/SDA11/TRDIOC1
- 24 — P12/SO11/TRDIOB1/IVREF1 ^{Note}
- 23 — P13/TxD2/SO20/TRDIOA1/IVCMP1 ^{Note}
- 22 — P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
- 21 — P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
- 20 — P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 ^{Note}/(RXD0)
- 19 — P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 ^{Note}/(TXD0)
- 18 — P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
- 17 — P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)
- 16 — P30/INTP3/SCK00/SCL00/TRJO0

Note　Mounted on the 96 KB or more code flash memory products.

Caution　**Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**
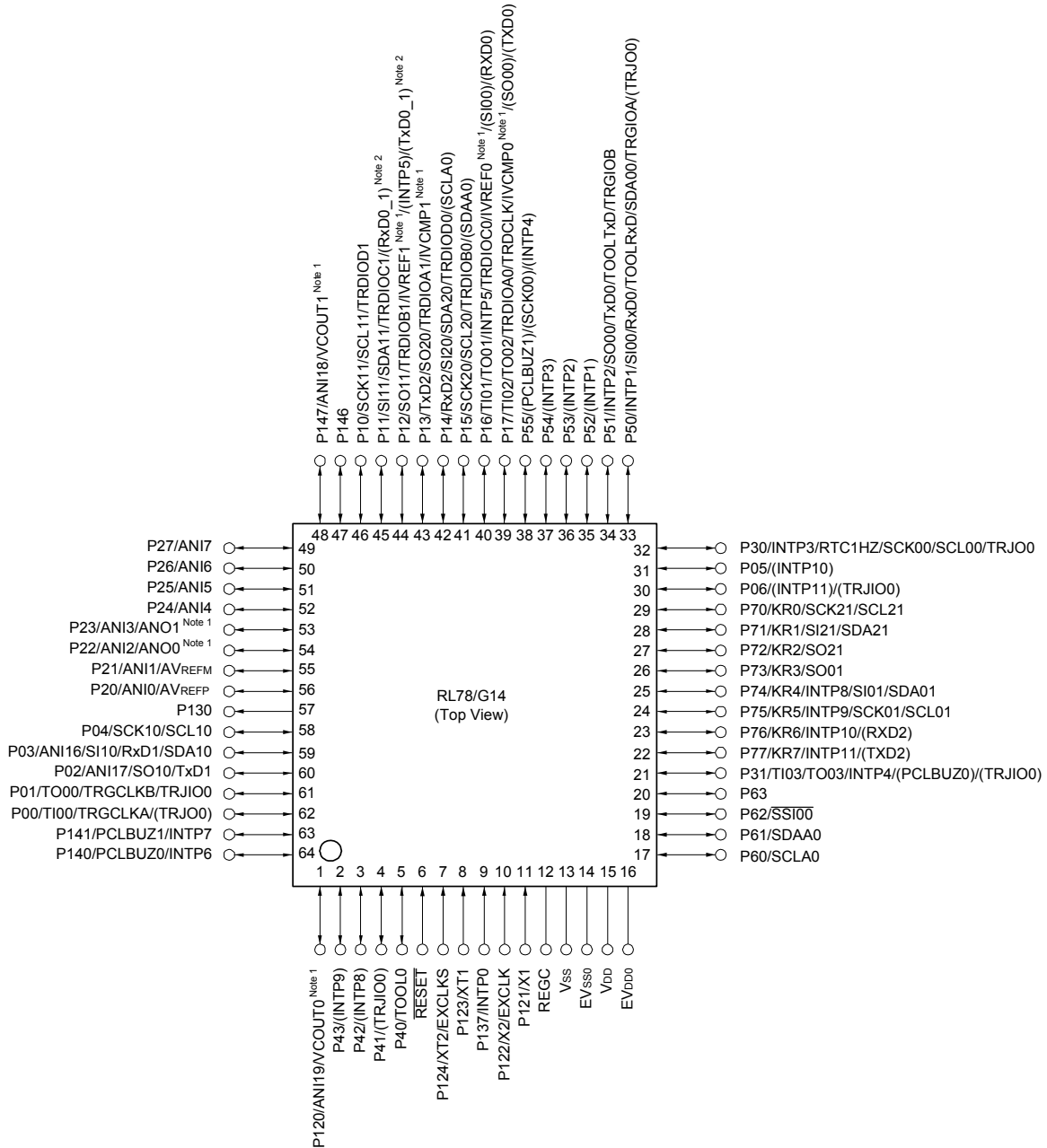
Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).
Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.8   64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

RL78/G14 (Top View)

Top side pins (left to right, pins 48–33):
- 48 — P147/ANI18/VCOUT1 [Note 1]
- 47 — P146
- 46 — P10/SCK11/SCL11/TRDIOD1
- 45 — P11/SI11/SDA11/TRDIOC1/(RxD0_1) [Note 2]
- 44 — P12/SO11/TRDIOB1/IVREF1 [Note 1]/(INTP5)/(TxD0_1) [Note 2]
- 43 — P13/TxD2/SO20/TRDIOA1/IVCMP1 [Note 1]
- 42 — P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
- 41 — P15/SCK20/SCL20/TRDIOB0/(SDAA0)
- 40 — P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 [Note 1]/(SI00)/(RXD0)
- 39 — P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 [Note 1]/(SO00)/(TXD0)
- 38 — P55/(PCLBUZ1)/(SCK00)/(INTP4)
- 37 — P54/(INTP3)
- 36 — P53/(INTP2)
- 35 — P52/(INTP1)
- 34 — P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
- 33 — P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)

Left side pins (top to bottom, pins 49–64):
- 49 — P27/ANI7
- 50 — P26/ANI6
- 51 — P25/ANI5
- 52 — P24/ANI4
- 53 — P23/ANI3/ANO1 [Note 1]
- 54 — P22/ANI2/ANO0 [Note 1]
- 55 — P21/ANI1/AVREFM
- 56 — P20/ANI0/AVREFP
- 57 — P130
- 58 — P04/SCK10/SCL10
- 59 — P03/ANI16/SI10/RxD1/SDA10
- 60 — P02/ANI17/SO10/TxD1
- 61 — P01/TO00/TRGCLKB/TRJIO0
- 62 — P00/TI00/TRGCLKA/(TRJO0)
- 63 — P141/PCLBUZ1/INTP7
- 64 — P140/PCLBUZ0/INTP6

Right side pins (top to bottom, pins 32–17):
- 32 — P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0
- 31 — P05/(INTP10)
- 30 — P06/(INTP11)/(TRJIO0)
- 29 — P70/KR0/SCK21/SCL21
- 28 — P71/KR1/SI21/SDA21
- 27 — P72/KR2/SO21
- 26 — P73/KR3/SO01
- 25 — P74/KR4/INTP8/SI01/SDA01
- 24 — P75/KR5/INTP9/SCK01/SCL01
- 23 — P76/KR6/INTP10/(RXD2)
- 22 — P77/KR7/INTP11/(TXD2)
- 21 — P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)
- 20 — P63
- 19 — P62/SSI00
- 18 — P61/SDAA0
- 17 — P60/SCLA0

Bottom side pins (left to right, pins 1–16):
- 1 — P120/ANI19/VCOUT0 [Note 1]
- 2 — P43/(INTP9)
- 3 — P42/(INTP8)
- 4 — P41/(TRJIO0)
- 5 — P40/TOOL0
- 6 — RESET
- 7 — P124/XT2/EXCLKS
- 8 — P123/XT1
- 9 — P137/INTP0
- 10 — P122/X2/EXCLK
- 11 — P121/X1
- 12 — REGC
- 13 — VSS
- 14 — EVSS0
- 15 — VDD
- 16 — EVDD0

Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.
Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Item		44-pin R5F104Fx (x = F to H, J)	48-pin R5F104Gx (x = F to H, J)	52-pin R5F104Jx (x = F to H, J)	64-pin R5F104Lx (x = F to H, J)
Clock output/buzzer output		2	2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		10 channels	10 channels	12 channels	12 channels
D/A converter		2 channels			
Comparator		2 channels			
Serial interface		[44-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels [48-pin, 52-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels			
	I^{2}C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		31 sources	32 sources		33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9			
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt		4	6	8	8
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			

Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = −40 to +85°C)
		                       1.51 ±0.06 V (T_A = −40 to +105°C)
		• Power-down-reset: 1.50 ±0.04 V (T_A = −40 to +85°C)
		                          1.50 ±0.06 V (T_A = −40 to +105°C)			

Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)			
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note   The illegal instruction is generated when instruction code FFH is executed.

              Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		17 channels	20 channels
D/A converter		2 channels	2 channels
Comparator		2 channels	2 channels
Serial interface		[80-pin, 100-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels	
	I^2C bus	2 channels	2 channels
Data transfer controller (DTC)		39 sources	39 sources
Event link controller (ELC)		Event input: 26 Event trigger output: 9	
Vectored interrupt sources	Internal	32	32
	External	13	13
Key interrupt		8	8
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access	

Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = −40 to +85°C)
		                                 1.51 ±0.06 V (T_A = −40 to +105°C)
		 • Power-down-reset: 1.50 ±0.04 V (T_A = −40 to +85°C)
		                                 1.50 ±0.06 V (T_A = −40 to +105°C)	

Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note   The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz 　(Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz 　(Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		17 channels	20 channels
D/A converter		2 channels	2 channels
Comparator		2 channels	2 channels
Serial interface		[80-pin, 100-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels	
	I^2C bus	2 channels	2 channels
Data transfer controller (DTC)		39 sources	39 sources
Event link controller (ELC)		Event input: 26 Event trigger output: 9	
Vectored inter-rupt sources	Internal	32	32
	External	13	13
Key interrupt		8	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset:　　1.51 ±0.04 V (T_A = −40 to +85°C) 　　　　　　　　　　 1.51 ±0.06 V (T_A = −40 to +105°C) • Power-down-reset:　1.50 ±0.04 V (T_A = −40 to +85°C) 　　　　　　　　　　 1.50 ±0.06 V (T_A = −40 to +105°C)	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note　　The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.3　DC Characteristics

2.3.1　Pin characteristics

(T$_A$ = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high [Note 1]	I$_{OH1}$	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq$ 70% [Note 3])	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			-55.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			-10.0	mA
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			-5.0	mA
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq$ 70% [Note 3])	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			-80.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			-19.0	mA
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			-10.0	mA
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			-5.0	mA
		Total of all pins (When duty $\leq$ 70% [Note 3])	1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			-135.0 Note 4	mA
	I$_{OH2}$	Per pin for P20 to P27, P150 to P156	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			-0.1 Note 2	mA
		Total of all pins (When duty $\leq$ 70% [Note 3])	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EV$_{DD0}$, EV$_{DD1}$, V$_{DD}$ pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor $\leq$ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OH}$ × 0.7)/(n × 0.01)
  - \<Example\>　　Where n = 80% and I$_{OH}$ = -10.0 mA
  　　　　　　　　Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) $\approx$ -8.7 mA

　　　However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
　　　A current higher than the absolute maximum rating must not flow into one pin.

Note 4. -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

Caution　**P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark　Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1.   Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2.   When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3.   When high-speed system clock and subsystem clock are stopped.

Note 4.   When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 5.   Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T$_A$ = -40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 1	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		25		25		25	ns

Note 1.   When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2.   Use it with EV$_{DD0}$ ≥ V$_b$.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode)

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 Note 3		1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 Note 3		1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		ns
		4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		ns
		1.8 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		1/f$_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The value must also be equal to or less than f$_{MCK}$/4.

Note 2. Use it with EV$_{DD0}$ $\geq$ V$_b$.

Note 3. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

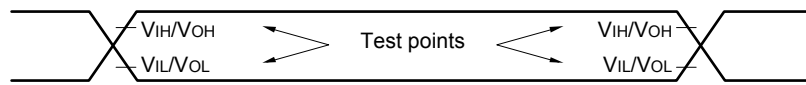(**Remarks** are listed on the next page.)

2.5.2　Serial interface IICA

(1)　I2C standard mode

(TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Standard mode: fCLK $\geq$ 1 MHz	2.7 V $\leq$ EVDD0 $\leq$ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V $\leq$ EVDD0 $\leq$ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V $\leq$ EVDD0 $\leq$ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V $\leq$ EVDD0 $\leq$ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	tSU: STA	2.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.8 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.6 V $\leq$ EVDD0 $\leq$ 5.5 V		—		4.7		4.7		µs
Hold time Note 1	tHD: STA	2.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.8 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.6 V $\leq$ EVDD0 $\leq$ 5.5 V		—		4.0		4.0		µs
Hold time when SCLA0 = "L"	tLOW	2.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.8 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.7		4.7		4.7		µs
		1.6 V $\leq$ EVDD0 $\leq$ 5.5 V		—		4.7		4.7		µs
Hold time when SCLA0 = "H"	tHIGH	2.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.8 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.7 V $\leq$ EVDD0 $\leq$ 5.5 V		4.0		4.0		4.0		µs
		1.6 V $\leq$ EVDD0 $\leq$ 5.5 V		—		4.0		4.0		µs

(**Notes**, **Caution**, and **Remark** are listed on the next page.)
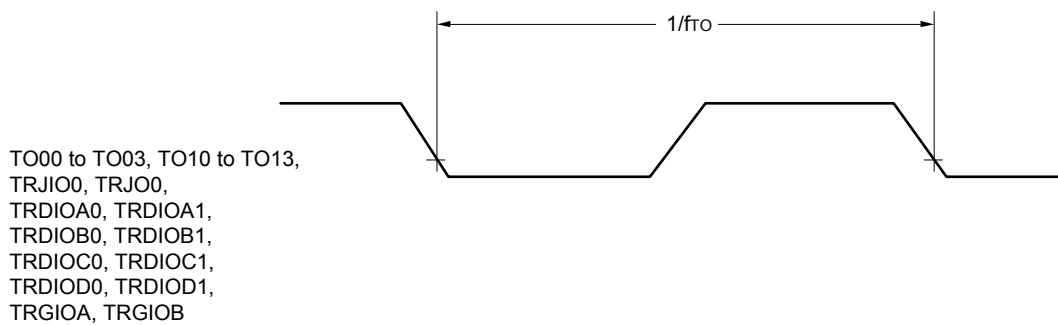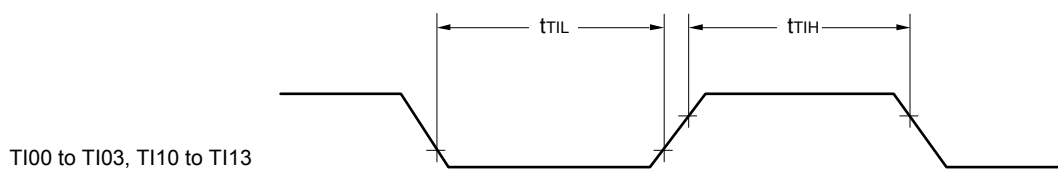
AC Timing Test Points

External System Clock Timing

TI/TO Timing

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) **(1/2)**

Parameter	Symbol	Conditions			HS (high-speed main) mode		Unit
					MIN.	MAX.	
Transfer rate		reception	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		2.6	Mbps
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		2.6	Mbps
			2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V			f_{MCK}/12 [Notes 1, 2]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
　　　　　However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EV$_{DD0}$ < V$_{DD}$.
　　　　　2.4 V $\leq$ EV$_{DD0}$ < 2.7 V: MAX. 1.3 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
　　　　　HS (high-speed main) mode:　　32 MHz (2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)
　　　　　　　　　　　　　　　　　　　　16 MHz (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

Remark 1. V$_b$ [V]: Communication line voltage
Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)
Remark 3. f_{MCK}: Serial array unit operation clock frequency
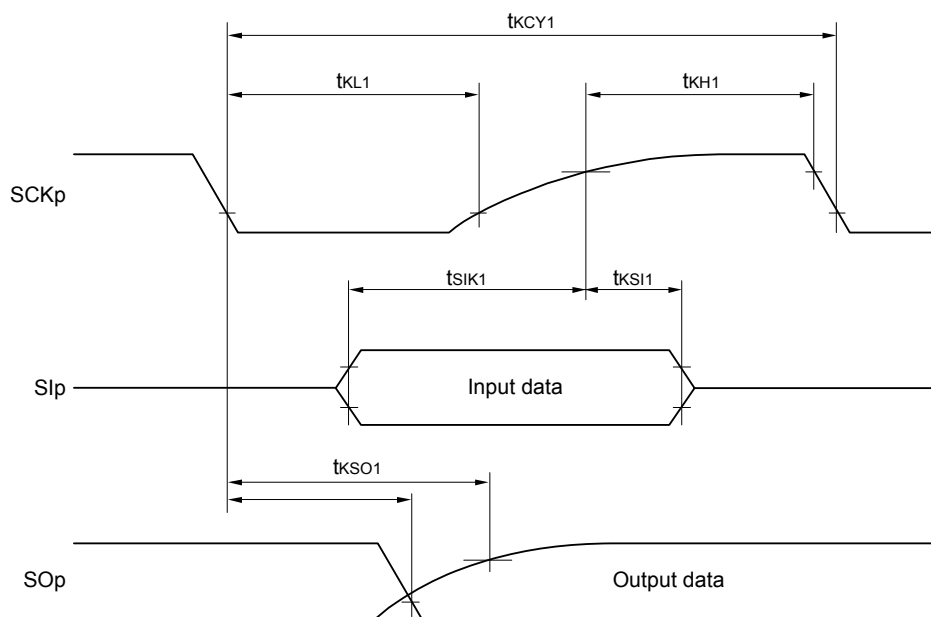　　　　　　 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
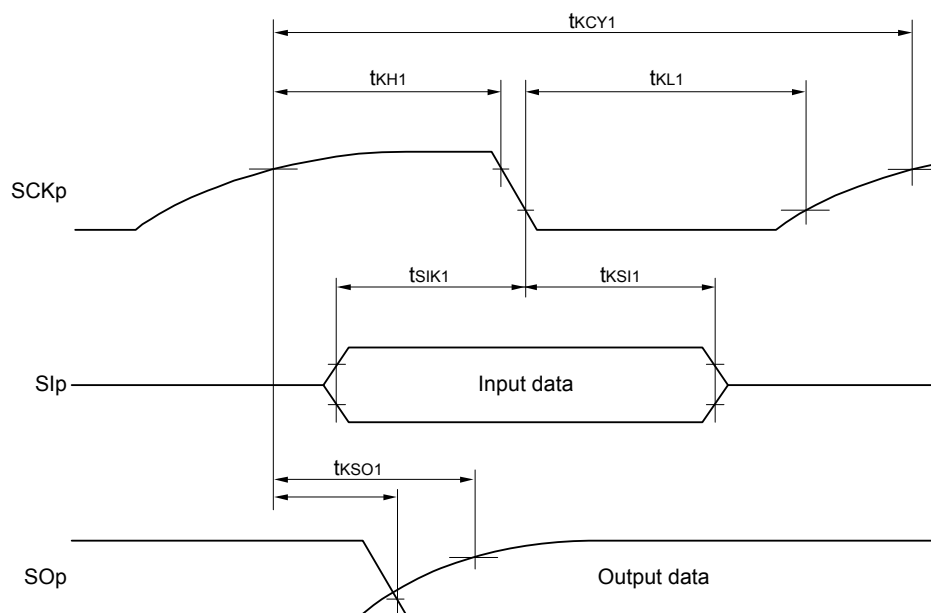　　　　　　 n: Channel number (mn = 00 to 03, 10 to 13)
Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

t$_{KCY1}$

t$_{KL1}$ t$_{KH1}$

SCKp

t$_{SIK1}$ t$_{KSI1}$

SIp   Input data

t$_{KSO1}$

SOp   Output data

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

t$_{KCY1}$

t$_{KH1}$ t$_{KL1}$

SCKp

t$_{SIK1}$ t$_{KSI1}$

SIp   Input data

t$_{KSO1}$

SOp   Output data

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for
communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	12/f$_{MCK}$		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ $\leq$ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	12/f$_{MCK}$		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ $\leq$ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		t$_{KCY2}$/2 - 24		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		t$_{KCY2}$/2 - 36		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		t$_{KCY2}$/2 - 100		ns
SIp setup time (to SCKp↑) [Note 2]	t$_{SIK2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V, C$_b$ = 30 pF, R$_v$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

3.6   Analog Characteristics

3.6.1   A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (-) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (-) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (-)= AV$_{REFM}$
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI20	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ AV$_{REFP}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (-) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V		1.2	±3.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	2.125		39	µs
			2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	3.1875		39	µs
			2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	µs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	2.375		39	µs
			2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	3.5625		39	µs
			2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	µs
Zero-scale error [Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±0.25	%FSR
Full-scale error [Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±0.25	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±1.5	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage output (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 4]		V
		Temperature sensor output voltage (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 4]		V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3.   When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
     Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
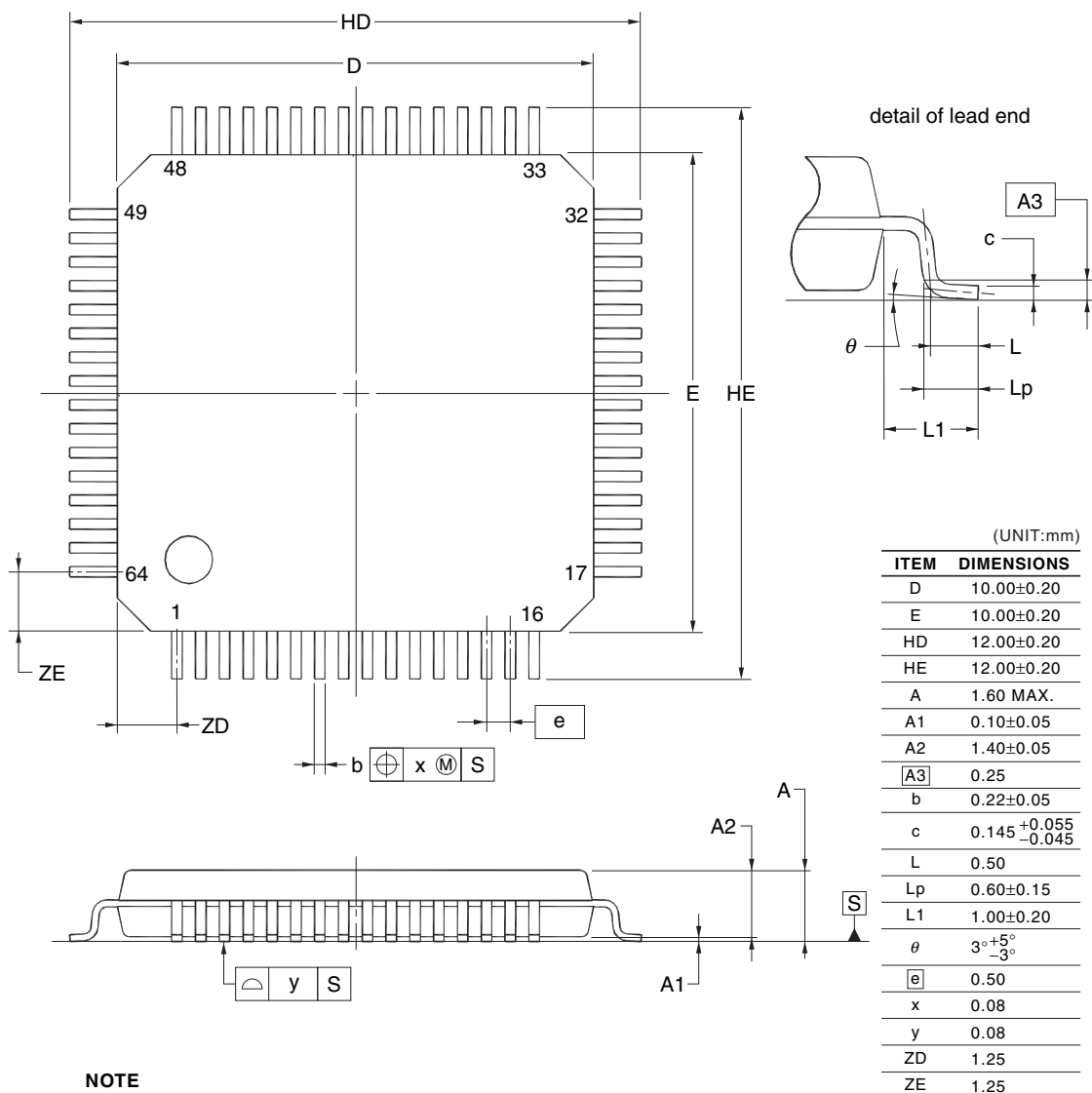   Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
     Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Note 4.   Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB, R5F104LJAFB

R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB, R5F104LJDFB

R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB, R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

detail of lead end

	(UNIT:mm)
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 ^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° ^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.