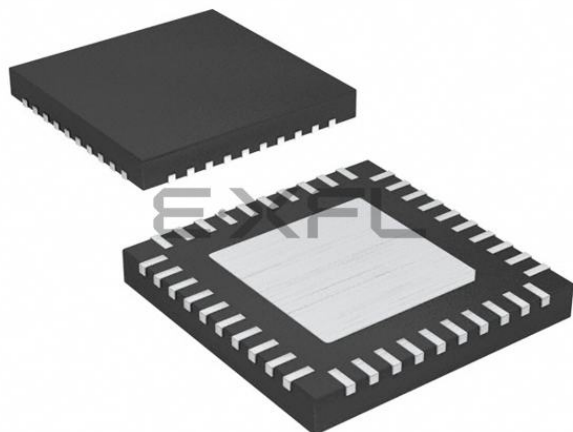




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104efana-u0

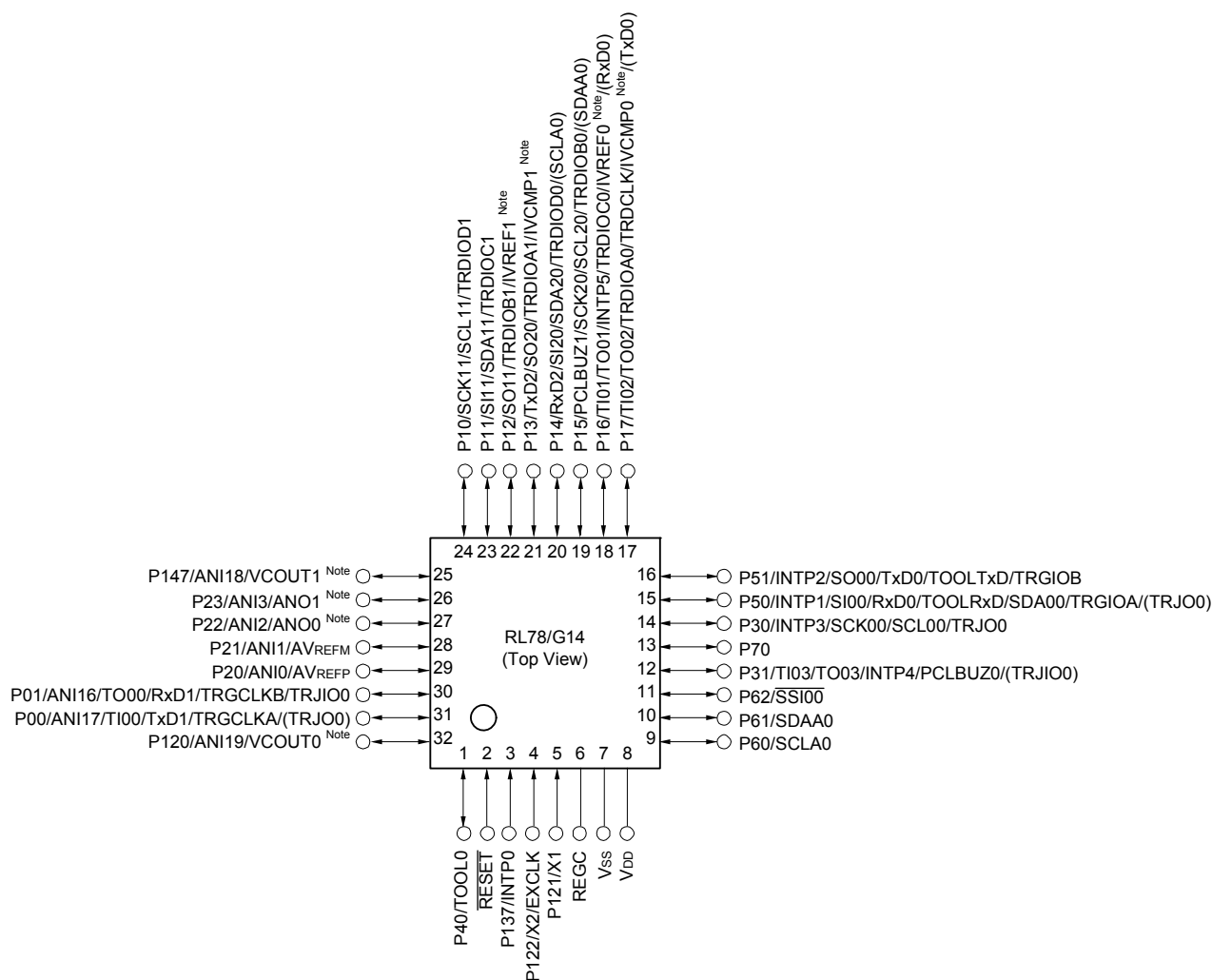
(2/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	A	R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0 R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0
		D	R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0 R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0
		G	R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0 R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0
44 pins	44-pin plastic LQFP (10 × 10, 0.8 mm pitch)	A	R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0 R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0
		D	R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0 R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0
		G	R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0 R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

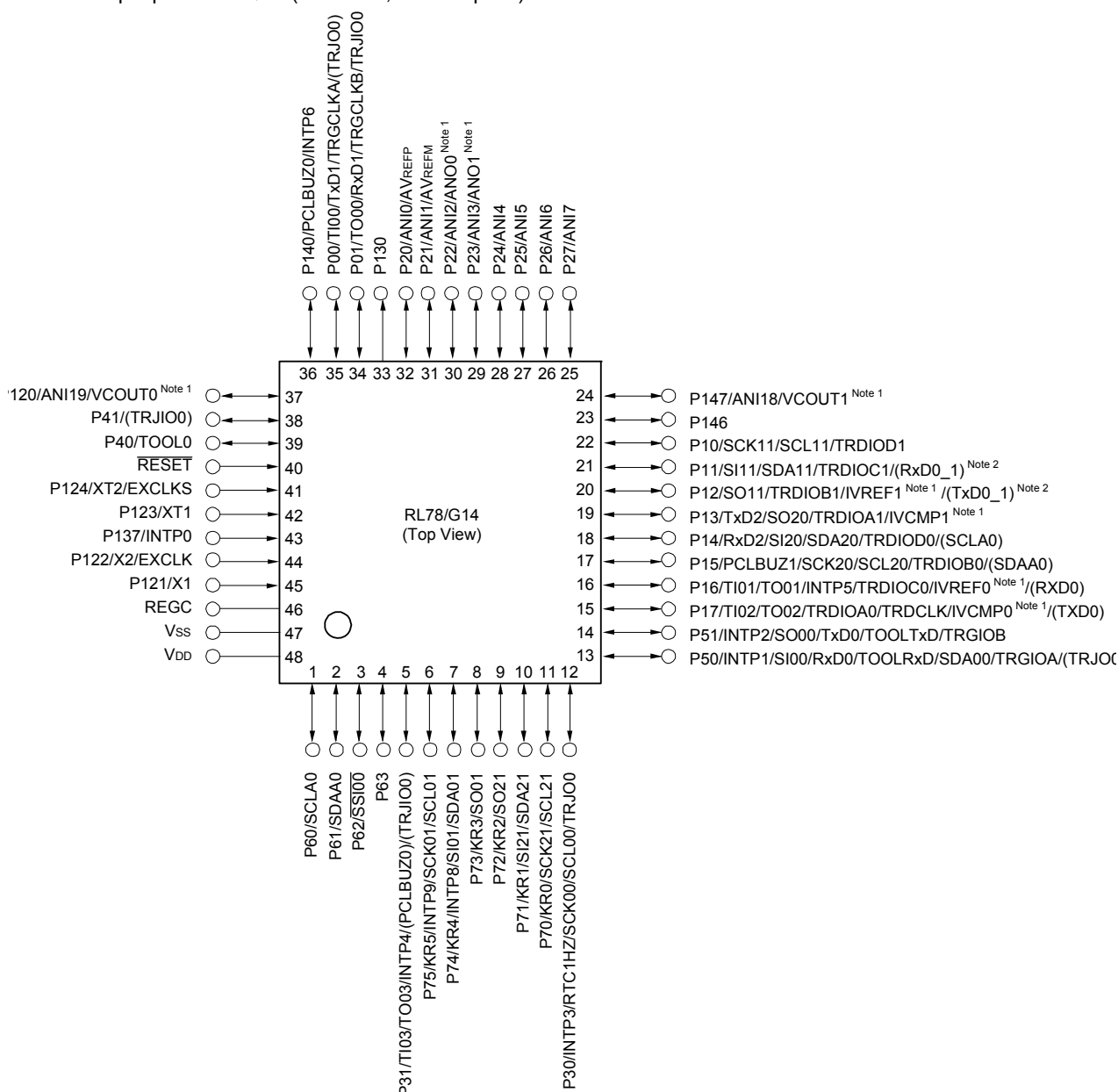
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

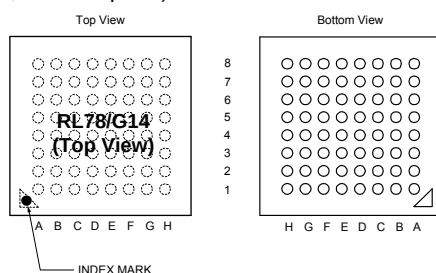
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)



	A	B	C	D	E	F	G	H	
8	EVDD0	EVSS0	P121/X1	P122/X2/ EXCLK	P137/INTP0	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ VCOUT0 Note 1	8
7	P60/SCLA0	VDD	VSS	REGC	RESET	P01/TO00/ TRGCLKB/ TRJIO0	P00/TIO0/ TRGCLKA/ (TRJIO0)	P140/ PCLBUZ0/ INTP6	7
6	P61/SDAA0	P62/SSI00	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/ SO10/TxD1	P141/ PCLBUZ1/ INTP7	6
5	P77/KR7/ INTP11/(TXD2)	P31/TIO3/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AVREFP	5
4	P75/KR5/ INTP9/ SCK01/ SCL01	P76/KR6/ INTP10/ (RxD2)	P52/(INTP1)	P54/(INTP3)	P16/TIO1/ TO01/INTP5/ TRDI0C0/ IVREF0 Note 1/ (SI00)/(RxD0)	P21/ANI1/ AVREFM	P22/ANI2/ ANO0 Note 1	P23/ANI3/ ANO1 Note 1	4
3	P70/KR0/ SCK21/ SCL21	P73/KR3/ SO01	P74/KR4/ INTP8/SI01/ SDA01	P17/TIO2/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note 1/ (SO00)/(TXD0)	P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0)	P12/SO11/ TRDIOB1/ IVREF1 Note 1/ (INTP5)/ (TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJIO0	P72/KR2/ SO21	P71/KR1/ SI21/SDA21	P06/(INTP11)/ (TRJIO0)	P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)	P11/SI11/ SDA11/ TRDI0C1/ (RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJIO0)	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P55/ (PCLBUZ1)/ (SCK00)/ (INTP4)	P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 Note 1	P10/SCK11/ SCL11/ TRDIOD1	P146	P147/ANI18/ VCOUT1 Note 1	1
	A	B	C	D	E	F	G	H	

Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

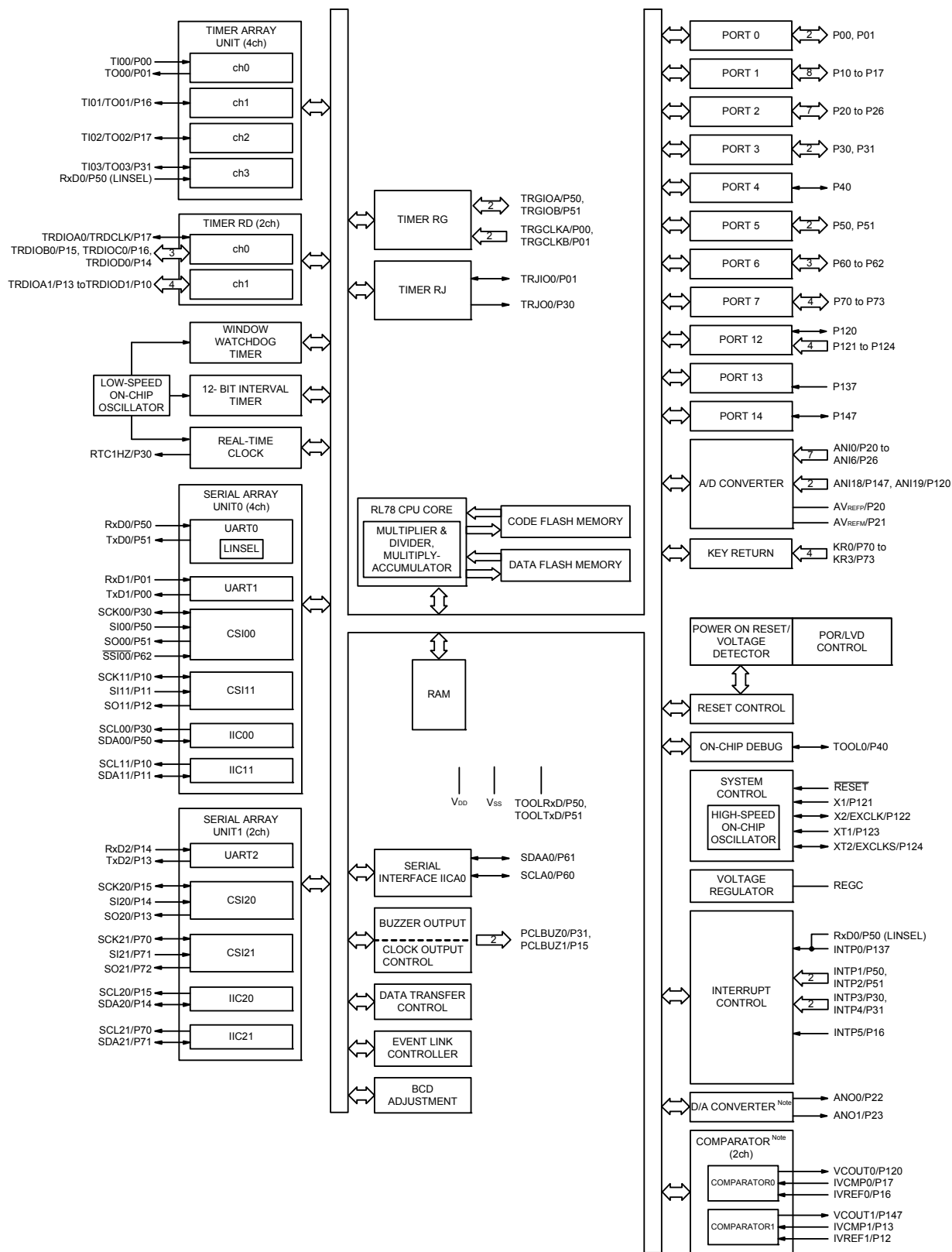
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

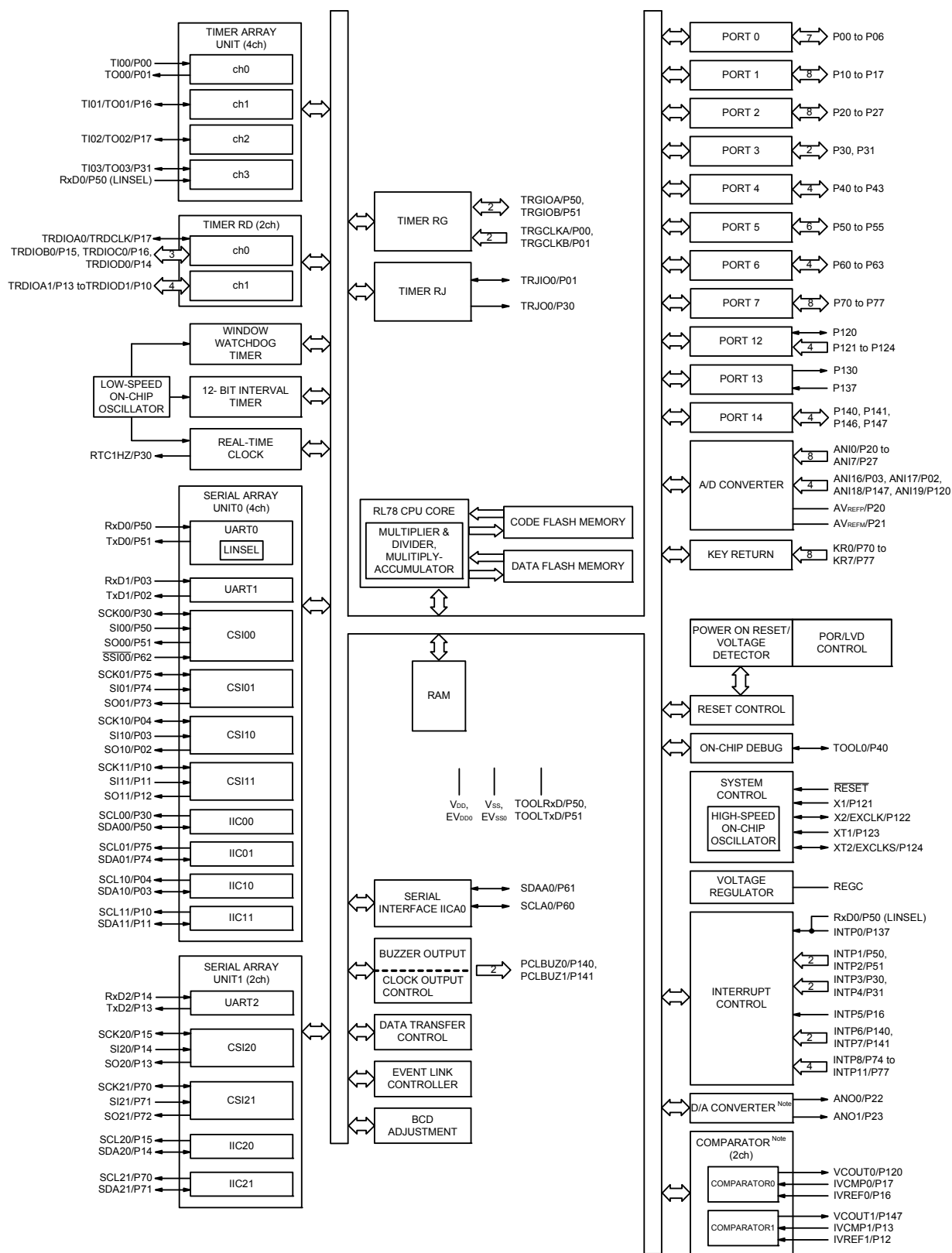
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.4 40-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.5.8 64-pin products



Note Mounted on the 96 KB or more code flash memory products.

(2/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
D/A converter		1 channel	2 channels		
Comparator		2 channels			
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources			31 sources
Event link controller (ELC)		Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V ($T_A = -40$ to +85°C) 1.51 ±0.06 V ($T_A = -40$ to +105°C) • Power-down-reset: 1.50 ±0.04 V ($T_A = -40$ to +85°C) 1.50 ±0.06 V ($T_A = -40$ to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to +85°C) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to +105°C)			
Operating ambient temperature		$T_A = -40$ to +85°C (A: Consumer applications, D: Industrial applications), $T_A = -40$ to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7		mA
						VDD = 3.0 V		5.1	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9		
						VDD = 3.0 V		4.0	6.9		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3		
						VDD = 3.0 V		3.8	6.3		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0		mA
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8		mA
						VDD = 2.0 V		1.3	1.8		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3		mA
						Resonator connection		3.4	5.5		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3		
						Resonator connection		3.4	5.5		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
			LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9		mA
						Resonator connection		1.2	2.0		
				fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9		
						Resonator connection		1.2	2.0		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.79	3.32	mA			
					V _{DD} = 3.0 V		0.79	3.32				
				f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.49	2.63				
					V _{DD} = 3.0 V		0.49	2.63				
				f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.62	2.57				
					V _{DD} = 3.0 V		0.62	2.57				
				f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.4	2.00				
					V _{DD} = 3.0 V		0.4	2.00				
				f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.38	1.49				
					V _{DD} = 3.0 V		0.38	1.49				
			LS (low-speed main) mode Note 7	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 4	V _{DD} = 3.0 V		250	800	μA			
					V _{DD} = 2.0 V		250	800				
			LV (low-voltage main) mode Note 7	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 4	V _{DD} = 3.0 V		420	755	μA			
					V _{DD} = 2.0 V		420	755				
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.30	1.63	mA			
						Resonator connection		0.40		1.85		
					f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.30		1.63		
						Resonator connection		0.40		1.85		
					f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.20		0.89		
						Resonator connection		0.25		0.97		
					f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.20		0.89		
						Resonator connection		0.25		0.97		
					LS (low-speed main) mode Note 7	f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V	Square wave input			110	580	μA
							Resonator connection			140	630	
			f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V	Square wave input			110	580				
				Resonator connection			140	630				
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5, T _A = -40°C	Square wave input		0.28	0.66	μA			
					Resonator connection		0.47	0.85				
				f _{SUB} = 32.768 kHz Note 5, T _A = +25°C	Square wave input		0.34	0.66				
					Resonator connection		0.53	0.85				
				f _{SUB} = 32.768 kHz Note 5, T _A = +50°C	Square wave input		0.37	2.35				
					Resonator connection		0.56	2.54				
				f _{SUB} = 32.768 kHz Note 5, T _A = +70°C	Square wave input		0.61	4.08				
					Resonator connection		0.80	4.27				
				f _{SUB} = 32.768 kHz Note 5, T _A = +85°C	Square wave input		1.55	8.09				
					Resonator connection		1.74	8.28				
			I _{DD3} Note 6	STOP mode Note 8	T _A = -40°C					0.19	0.57	μA
					T _A = +25°C					0.25	0.57	
					T _A = +50°C					0.33	2.26	
					T _A = +70°C					0.52	3.99	
					T _A = +85°C					1.46	8.00	

(Notes and Remarks are listed on the next page.)

(4) Peripheral Functions (Common to all products)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDOT Notes 1, 2, 5	fIL = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	
		DTC operation			3.10		

Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
- Note 8.** Current flowing during programming of the data flash.
- Note 9.** Current flowing during self-programming.
- Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.
- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{CMP} when the comparator circuit is in operation.
- Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125	1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125	1	μs
			LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.25	1	μs
		Subsystem clock (fSUB) operation		1.8 V ≤ VDD ≤ 5.5 V	28.5	30.5	31.3 μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125	1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125	1	μs
			LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.25	1	μs
External system clock frequency	fex	2.7 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ VDD ≤ 2.7 V		1.0		16.0	MHz
		1.8 V ≤ VDD < 2.4 V		1.0		8.0	MHz
		1.6 V ≤ VDD < 1.8 V		1.0		4.0	MHz
	fexs			32		35	kHz
External system clock input high-level width, low-level width	texH, texL	2.7 V ≤ VDD ≤ 5.5 V		24			ns
		2.4 V ≤ VDD ≤ 2.7 V		30			ns
		1.8 V ≤ VDD < 2.4 V		60			ns
		1.6 V ≤ VDD < 1.8 V		120			ns
	texHS, texLS			13.7			μs
Ti00 to Ti03, Ti10 to Ti13 input high-level width, low-level width	ttrH, ttrL			1/fMCK + 10 Note			ns
Timer RJ input cycle	fc	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	100		ns
				1.8 V ≤ EVDD0 < 2.7 V	300		ns
				1.6 V ≤ EVDD0 < 1.8 V	500		ns
Timer RJ input high-level width, low-level width	trjIH, trjIL	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	40		ns
				1.8 V ≤ EVDD0 < 2.7 V	120		ns
				1.6 V ≤ EVDD0 < 1.8 V	200		ns

Note The following conditions are required for low voltage interface when EVDD0 < VDD

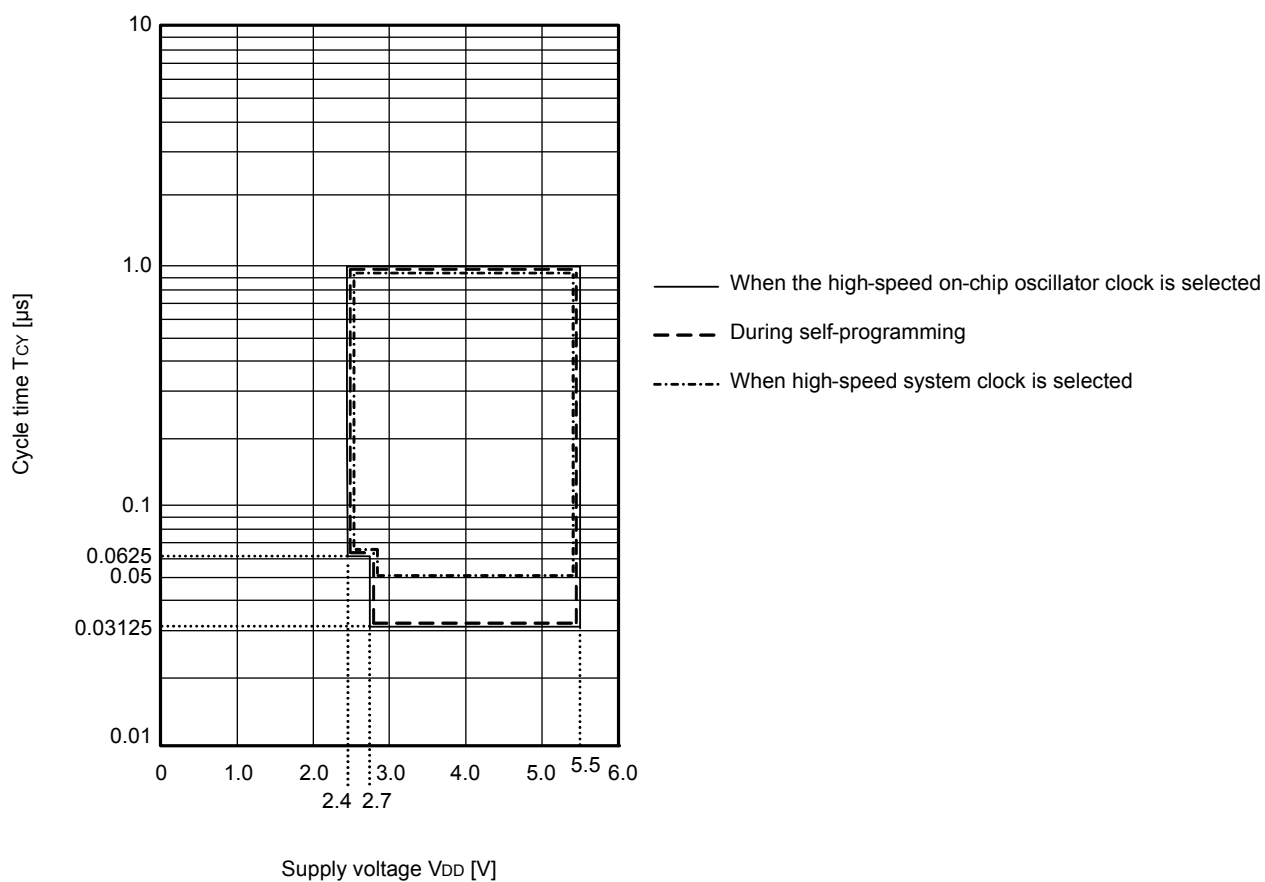
1.8 V ≤ EVDD0 < 2.7 V: MIN. 125 ns

1.6 V ≤ EVDD0 < 1.8 V: MIN. 250 ns

Remark fMCK: Timer array unit operation clock frequency

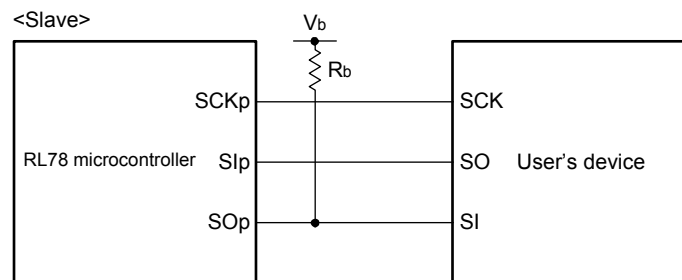
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation

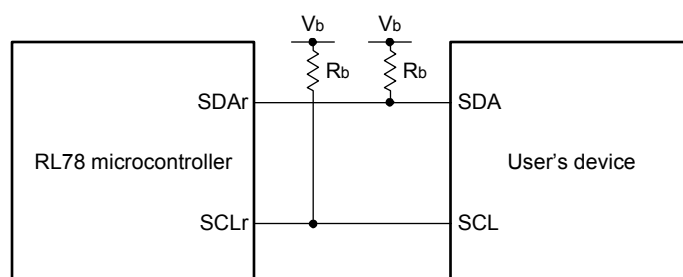
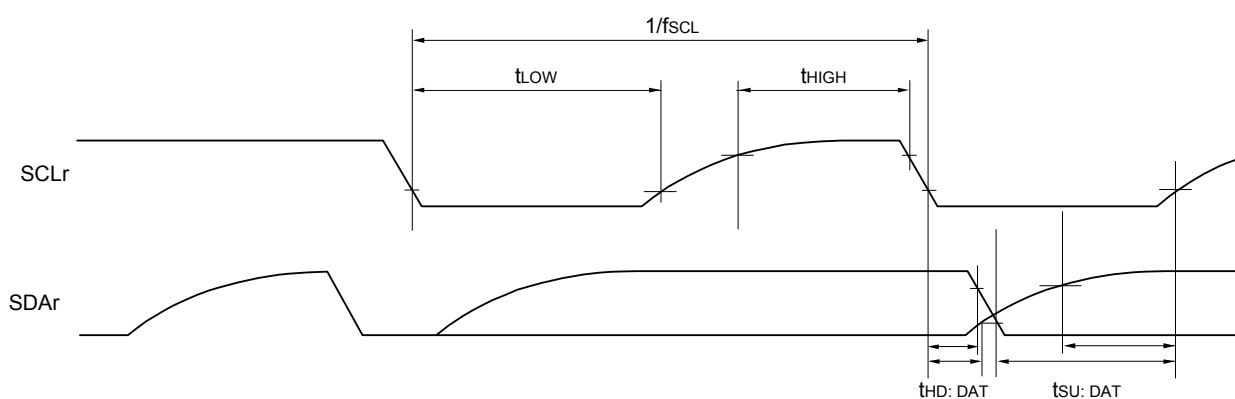
T_{CY} vs V_{DD} (HS (high-speed main) mode)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD0} \geq V_b$.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remark 1.** R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r : IIC number ($r = 00, 01, 10, 11, 20, 30, 31$), g : PIM, POM number ($g = 0, 1, 3$ to $5, 14$)

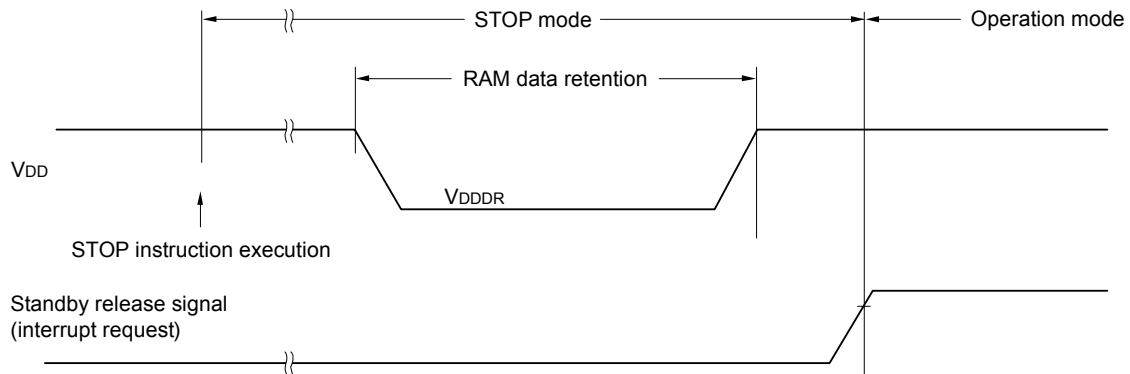
Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m : Unit number ($m = 0, 1$),
 n : Channel number ($n = 0, 2$), $mn = 00, 01, 02, 10, 12, 13$)

2.7 RAM Data Retention Characteristics

(TA = -40 to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

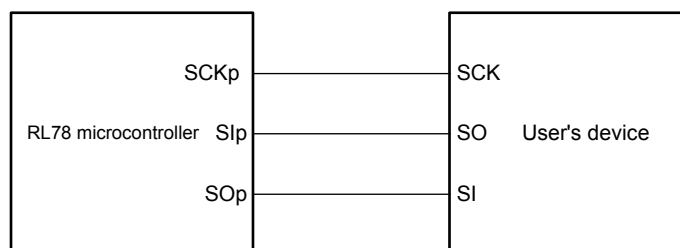
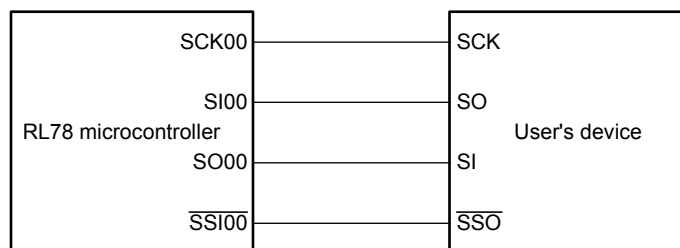
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{\text{SSI00}}$ setup time	t_{SSIK}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
$\overline{\text{SSI00}}$ hold time	t_{kSSI}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)
CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))


Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V	2.6 Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V	1.2 Note 4	Mbps
			2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V	0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using fmCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB

