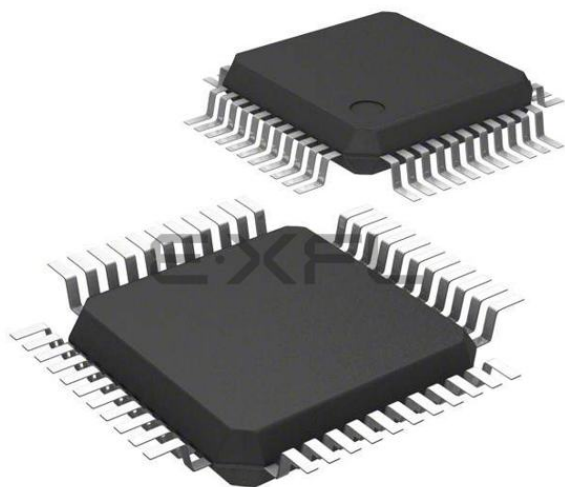




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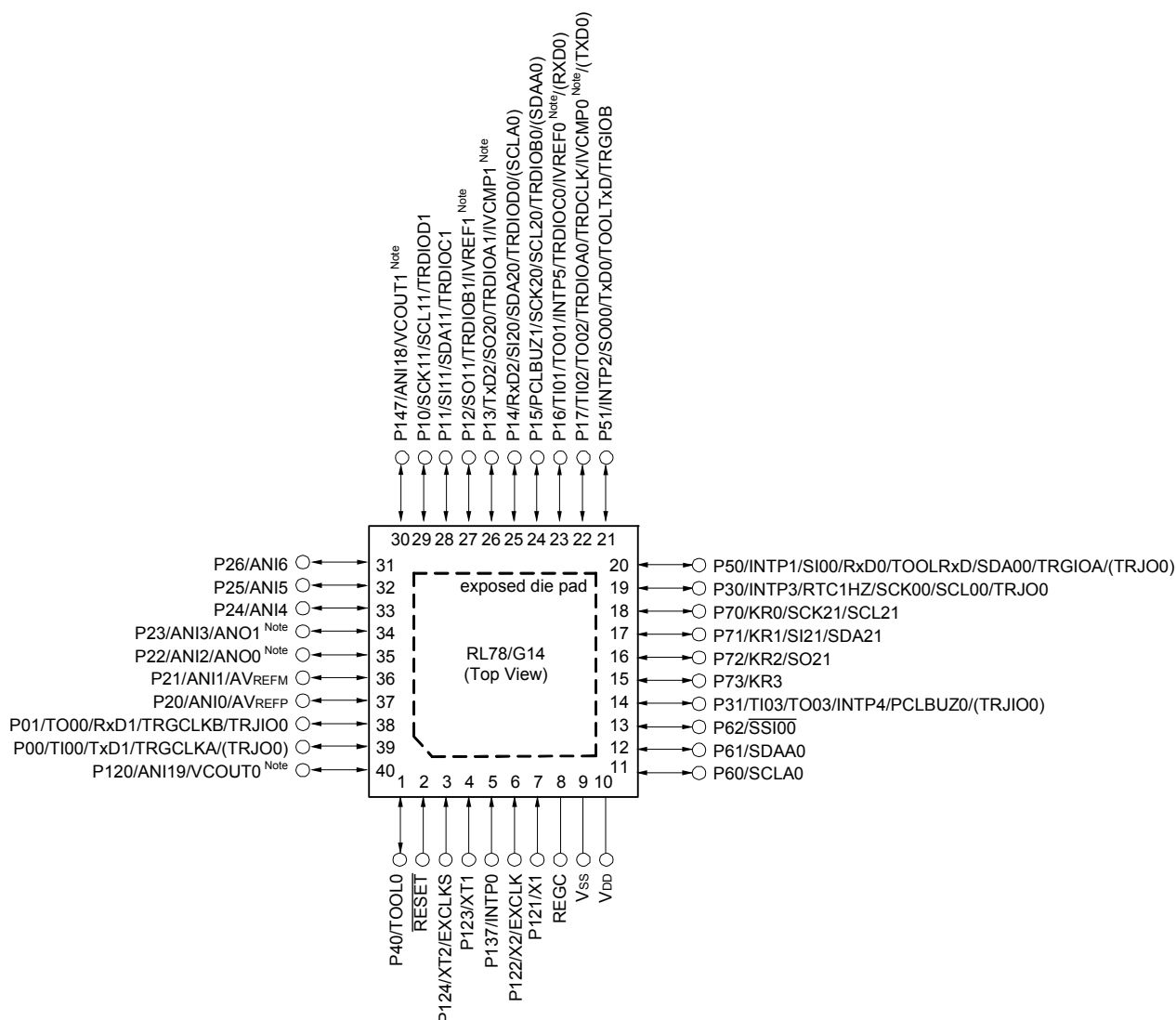
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fadfp-v0

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

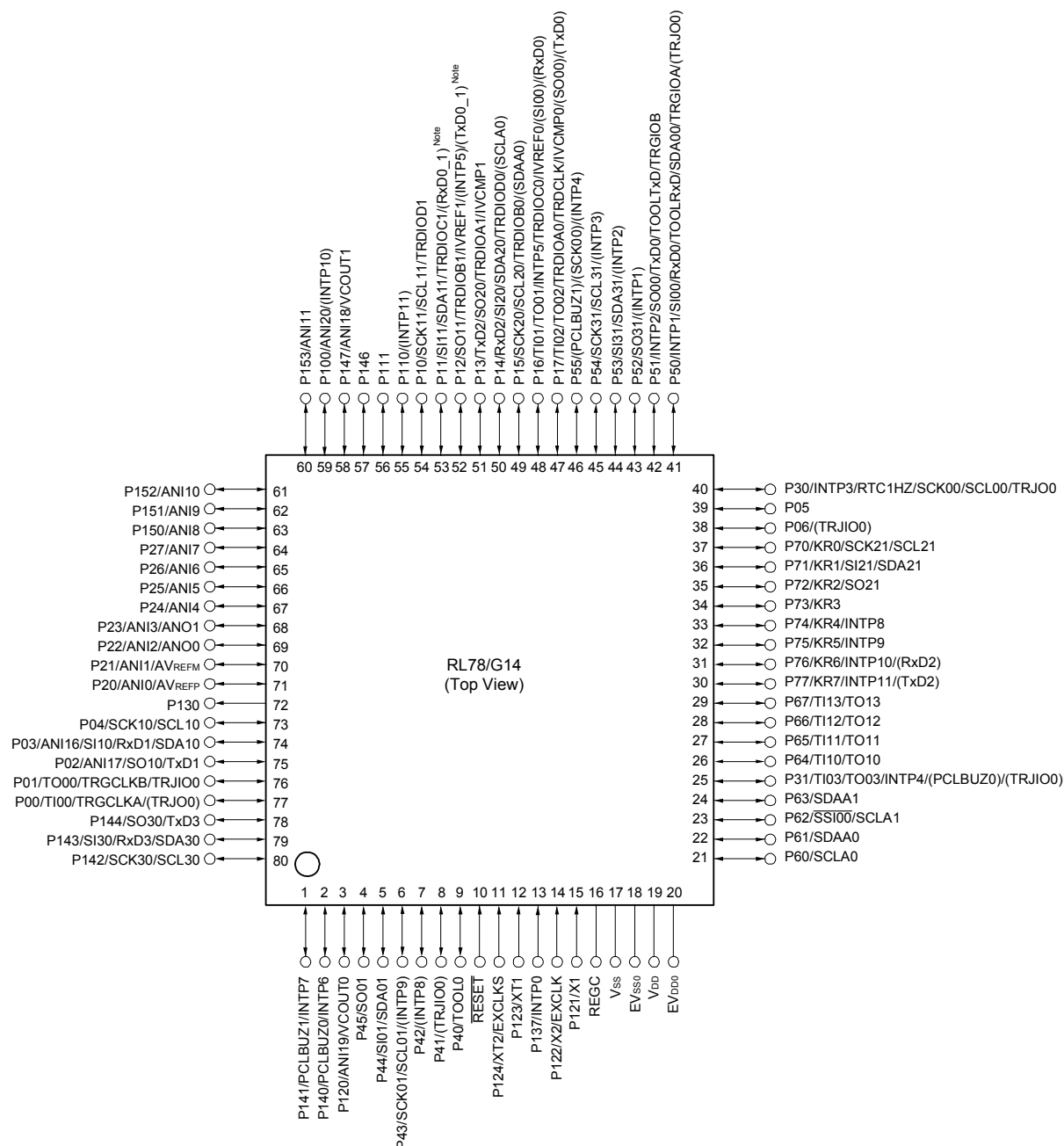
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

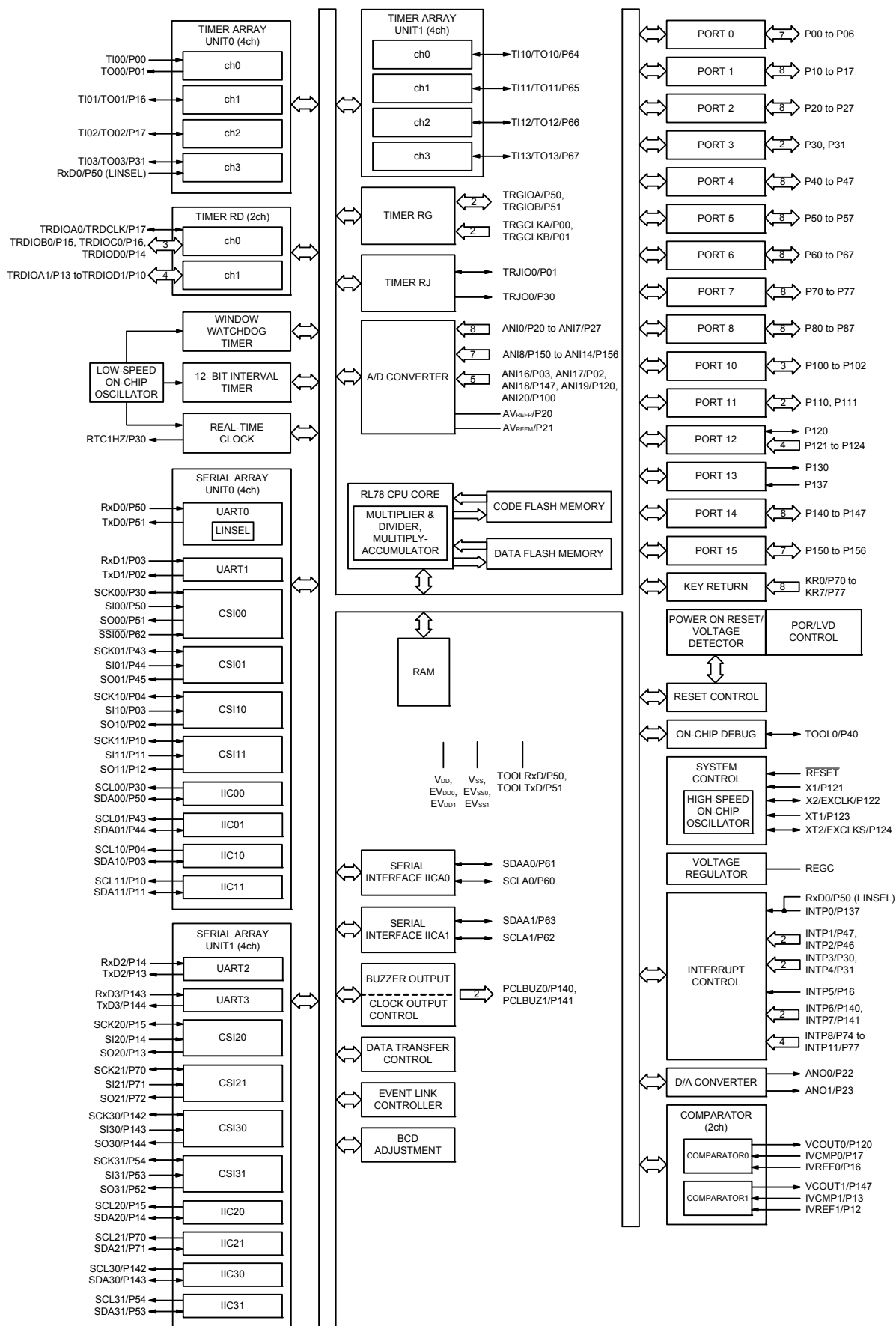
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

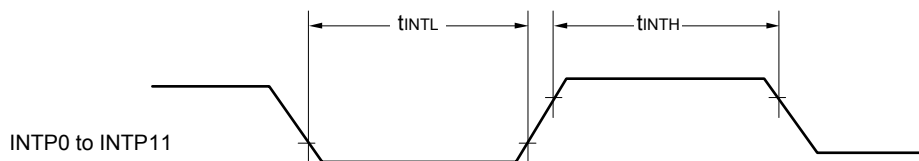
1.5.10 100-pin products



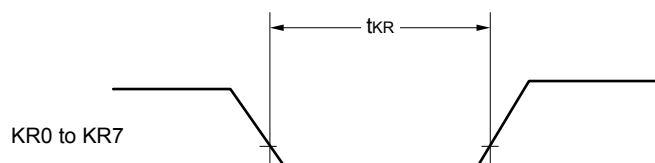
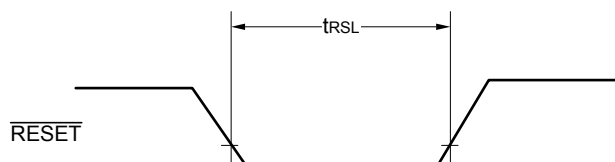
Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
		I ² C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)		28 sources			29 sources
Event link controller (ELC)		Event input: 19 Event trigger output: 7			Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T _A = −40 to +85°C) 1.51 ±0.06 V (T _A = −40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T _A = −40 to +85°C) 1.50 ±0.06 V (T _A = −40 to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = −40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = −40 to +105°C)			
Operating ambient temperature		T _A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = −40 to +105°C (G: Industrial applications)			

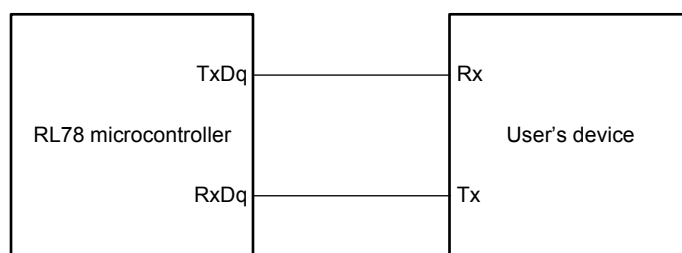
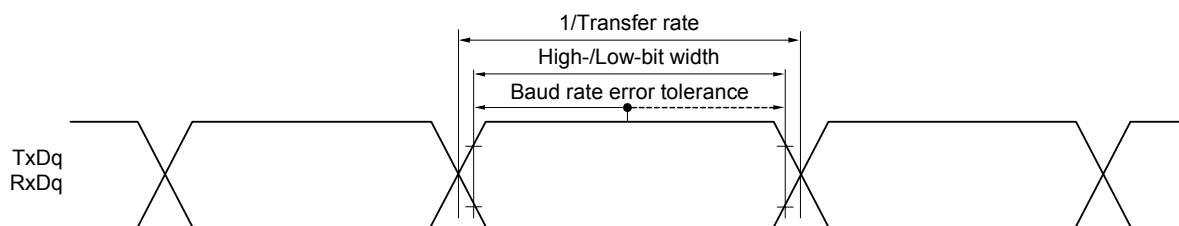
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Interrupt Request Input Timing



Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

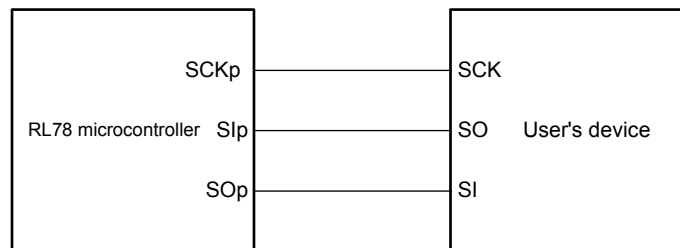
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

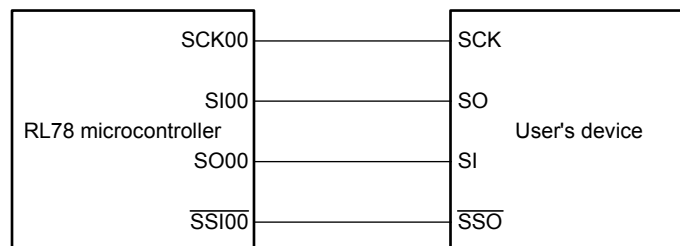
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SSI00 setup time	tSSIK	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
SSI00 hold time	tKSSI	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)

CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns

Note Use it with EVDD0 ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(1) I²C standard mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) Note 2	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		0	3.45	0	3.45	μs
Setup time of stop condition	tsu: STO	2.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.0		4.0		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

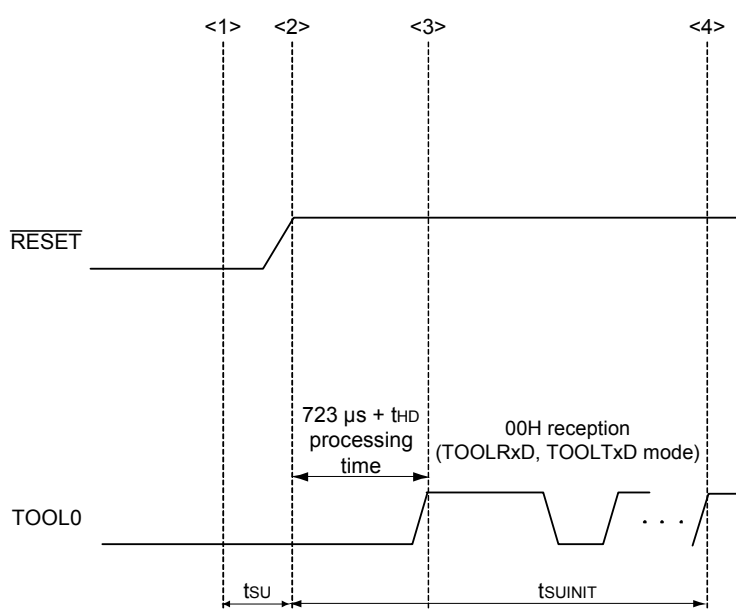
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

Absolute Maximum Ratings**(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +105
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{DD0}				1 μA
	ILI _{H2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{DD}				1 μA
	ILI _{H3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{DD}	In input port or external clock input			1 μA
				In resonator connection			10 μA
Input leakage current, low	ILI _{L1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0}				-1 μA
	ILI _{L2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{SS}				-1 μA
	ILI _{L3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{SS}	In input port or external clock input			-1 μA
				In resonator connection			-10 μA
On-chip pull-up resistance	R _U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100 kΩ

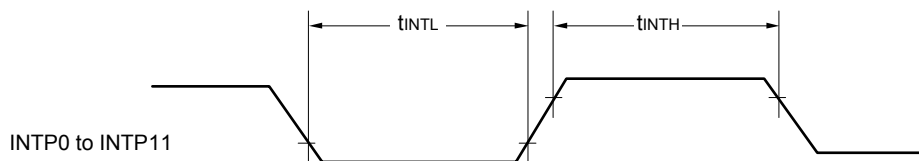
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)(2/2)**

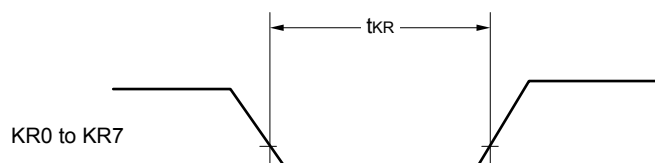
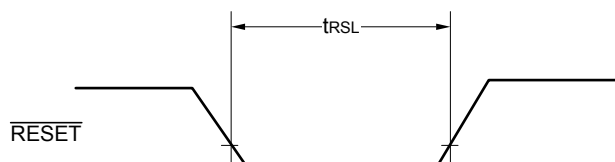
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	4.36	mA	
					VDD = 3.0 V		0.80	4.36		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	3.67		
					VDD = 3.0 V		0.49	3.67		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.42		
					VDD = 3.0 V		0.62	3.42		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.85		
					VDD = 3.0 V		0.4	2.85		
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	2.08			
				VDD = 3.0 V		0.37	2.08			
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	2.45	mA	
					Resonator connection		0.40	2.57		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28	2.45		
					Resonator connection		0.40	2.57		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19	1.28		
					Resonator connection		0.25	1.36		
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input		0.19	1.28			
				Resonator connection		0.25	1.36			
		Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA		
				Resonator connection		0.44	0.76			
			fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57			
				Resonator connection		0.49	0.76			
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17			
				Resonator connection		0.59	1.36			
			fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97			
				Resonator connection		0.72	2.16			
			fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37			
				Resonator connection		1.16	3.56			
			fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		3.20	17.10			
				Resonator connection		3.40	17.50			
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
			TA = +25°C					0.24	0.51	
			TA = +50°C					0.29	1.10	
			TA = +70°C					0.41	1.90	
			TA = +85°C					0.90	3.30	
			TA = +105°C					3.10	17.00	

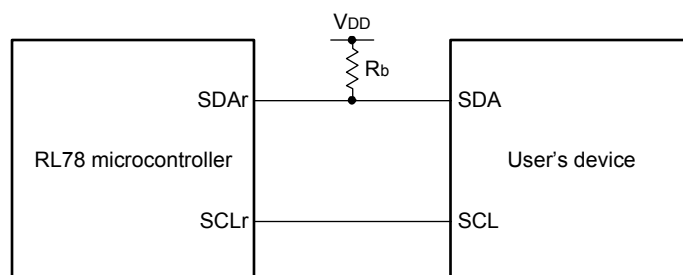
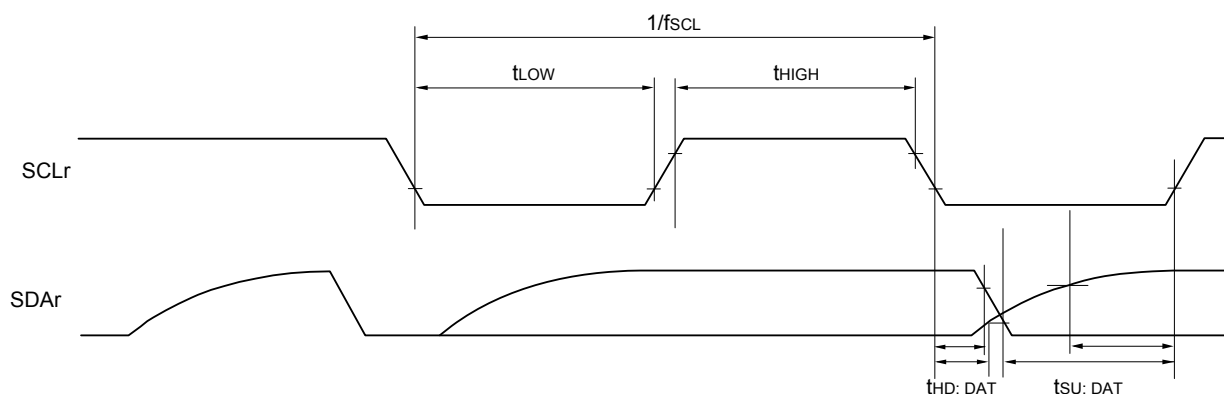
(Notes and Remarks are listed on the next page.)

Interrupt Request Input Timing



Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Remark 1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance

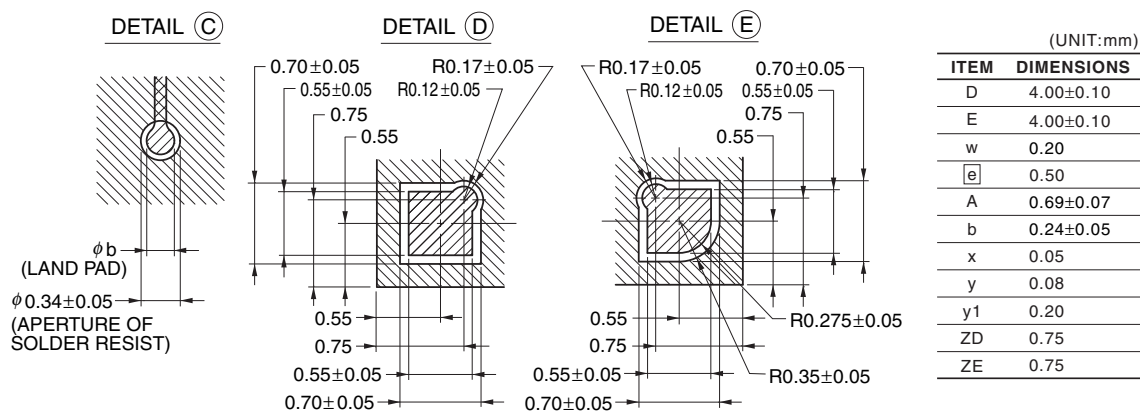
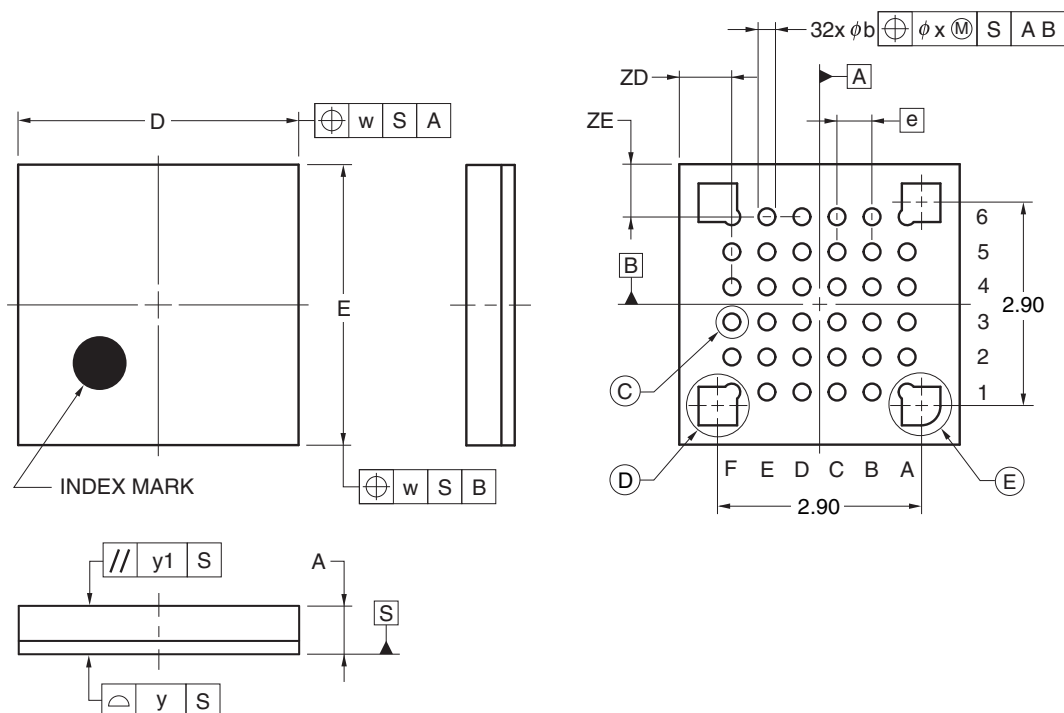
Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

4.3 36-pin products

R5F104CAALA, R5F104CCALA, R5F104CDALA, R5F104CEALA, R5F104CFALA, R5F104CGALA
R5F104CAGLA, R5F104CCGLA, R5F104CDGLA, R5F104CEGLA, R5F104CFGLA, R5F104CGGLA

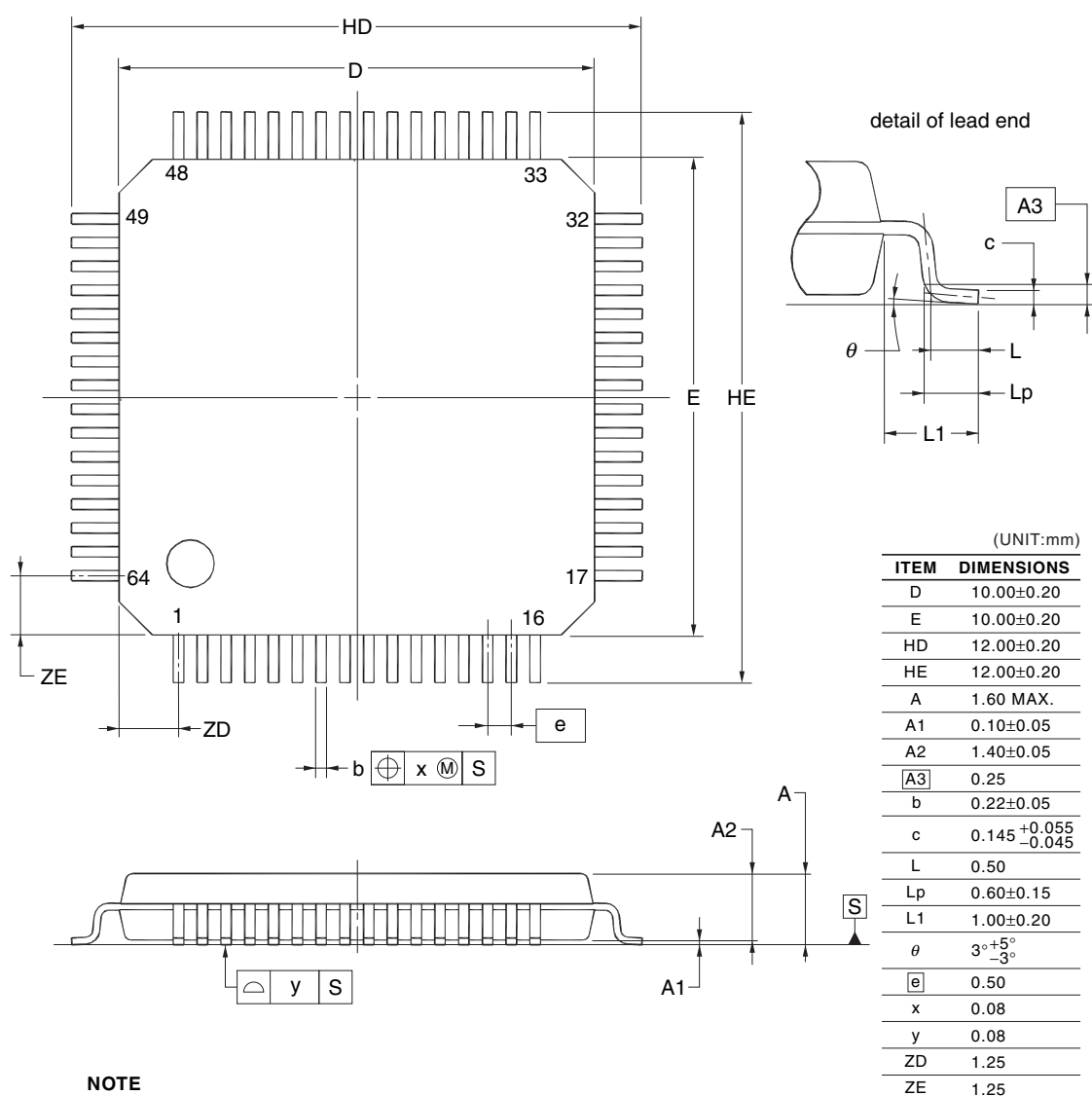
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023



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R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB,
 R5F104LJAFB
 R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB,
 R5F104LJDFB
 R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB,
 R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB

