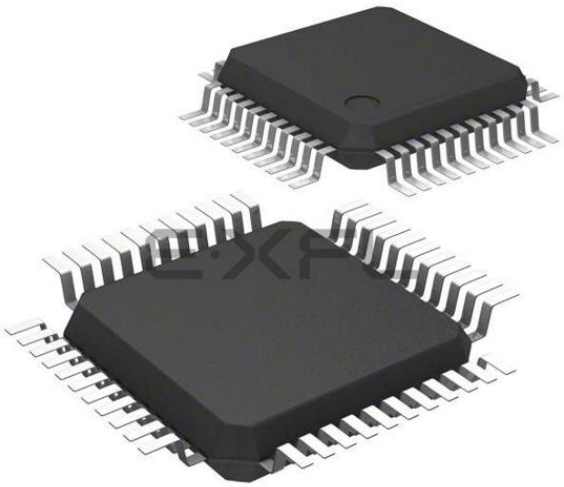
Renesas Electronics America Inc - R5F104FDAFP#X0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fdafp-x0

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Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAFA#V0, R5F104LHAFA#V0, R5F104LJAFA#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAFA#X0, R5F104LHAFA#X0, R5F104LJAFA#X0 R5F104LKAFA#30, R5F104LLAFA#30 R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFA#V0, R5F104LHDFA#V0, R5F104LJDFA#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFA#X0, R5F104LHDFA#X0, R5F104LJDFA#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LFDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LFDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0 R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0 R5F104LKALA#U0, R5F104LLALA#U0 R5F104LKALA#W0, R5F104LLALA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LFDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LFDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

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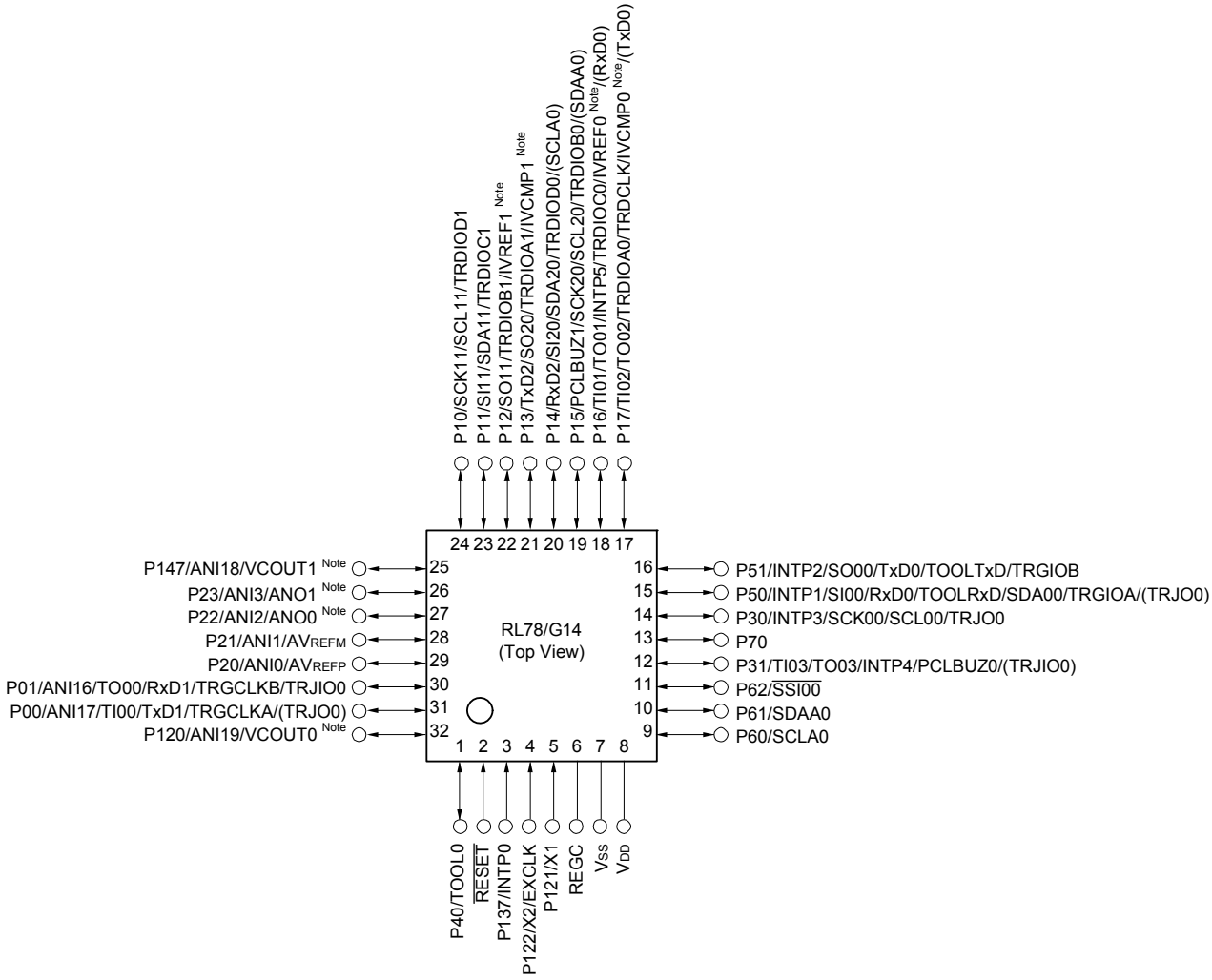
Pin count	Package	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFB#V0, R5F104MJAFB#V0 R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFB#X0, R5F104MJAFB#X0 R5F104MKAFB#30, R5F104MLAFB#30 R5F104MKAFB#50, R5F104MLAFB#50
		D	R5F104MFDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0 R5F104MFDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0
		G	R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0 R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0 R5F104MKGFB#30, R5F104MLGFB#30 R5F104MKGFB#X0, R5F104MLGFB#50
	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	A	R5F104MFAFA#V0, R5F104MGAFA#V0, R5F104MHAFA#V0, R5F104MJAFA#V0 R5F104MFAFA#X0, R5F104MGAFA#X0, R5F104MHAFA#X0, R5F104MJAFA#X0 R5F104MKAFA#30, R5F104MLAFA#30 R5F104MKAFA#50, R5F104MLAFA#50
		D	R5F104MFDFA#V0, R5F104MGDFA#V0, R5F104MHDFA#V0, R5F104MJDFA#V0 R5F104MFDFA#X0, R5F104MGDFA#X0, R5F104MHDFA#X0, R5F104MJDFA#X0
		G	R5F104MFGFA#V0, R5F104MGGFA#V0, R5F104MHGFA#V0, R5F104MJGFA#V0 R5F104MFGFA#X0, R5F104MGGFA#X0, R5F104MHGFA#X0, R5F104MJGFA#X0 R5F104MKGFA#30, R5F104MLGFA#30 R5F104MKGFA#50, R5F104MLGFA#50
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F104PFAFB#V0, R5F104PGAFB#V0, R5F104PHAFB#V0, R5F104PJAFB#V0 R5F104PFAFB#X0, R5F104PGAFB#X0, R5F104PHAFB#X0, R5F104PJAFB#X0 R5F104PKAFB#30, R5F104PLAFB#30 R5F104PKAFB#50, R5F104PLAFB#50
		D	R5F104PFDFB#V0, R5F104PGDFB#V0, R5F104PHDFB#V0, R5F104PJDFB#V0 R5F104PFDFB#X0, R5F104PGDFB#X0, R5F104PHDFB#X0, R5F104PJDFB#X0
		G	R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0 R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0 R5F104PKGFB#30, R5F104PLGFB#30 R5F104PKGFB#50, R5F104PLGFB#50
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	A	R5F104PFAFA#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFA#V0 R5F104PFAFA#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFA#X0 R5F104PKAFA#30, R5F104PLAFA#30 R5F104PKAFA#50, R5F104PLAFA#50
		D	R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFA#V0 R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFA#X0
		G	R5F104PFGFA#V0, R5F104PGGFA#V0, R5F104PHGFA#V0, R5F104PJGFA#V0 R5F104PFGFA#X0, R5F104PGGFA#X0, R5F104PHGFA#X0, R5F104PJGFA#X0 R5F104PKGFA#30, R5F104PLGFA#30 R5F104PKGFA#50, R5F104PLGFA#50

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

• 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

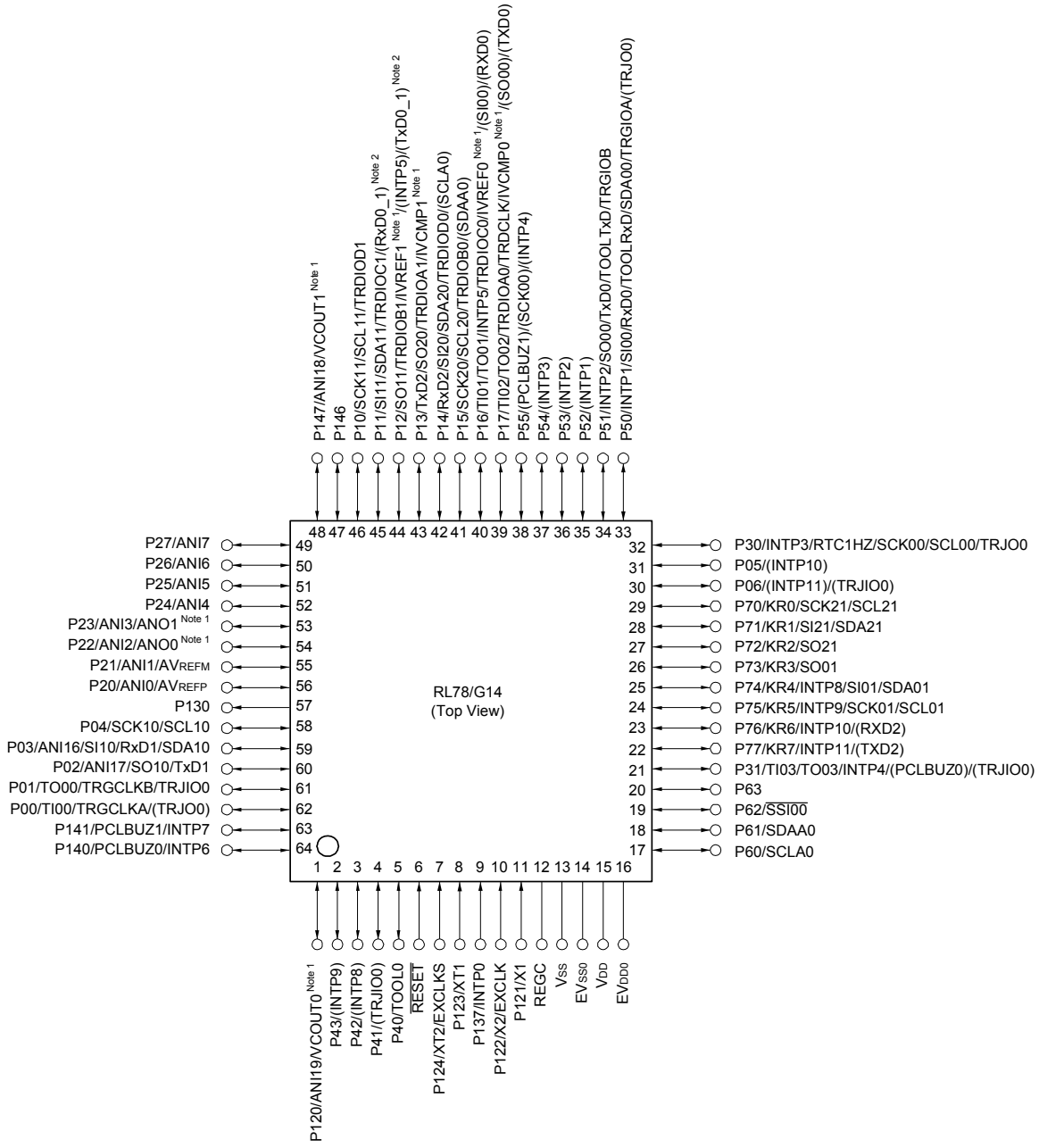
Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

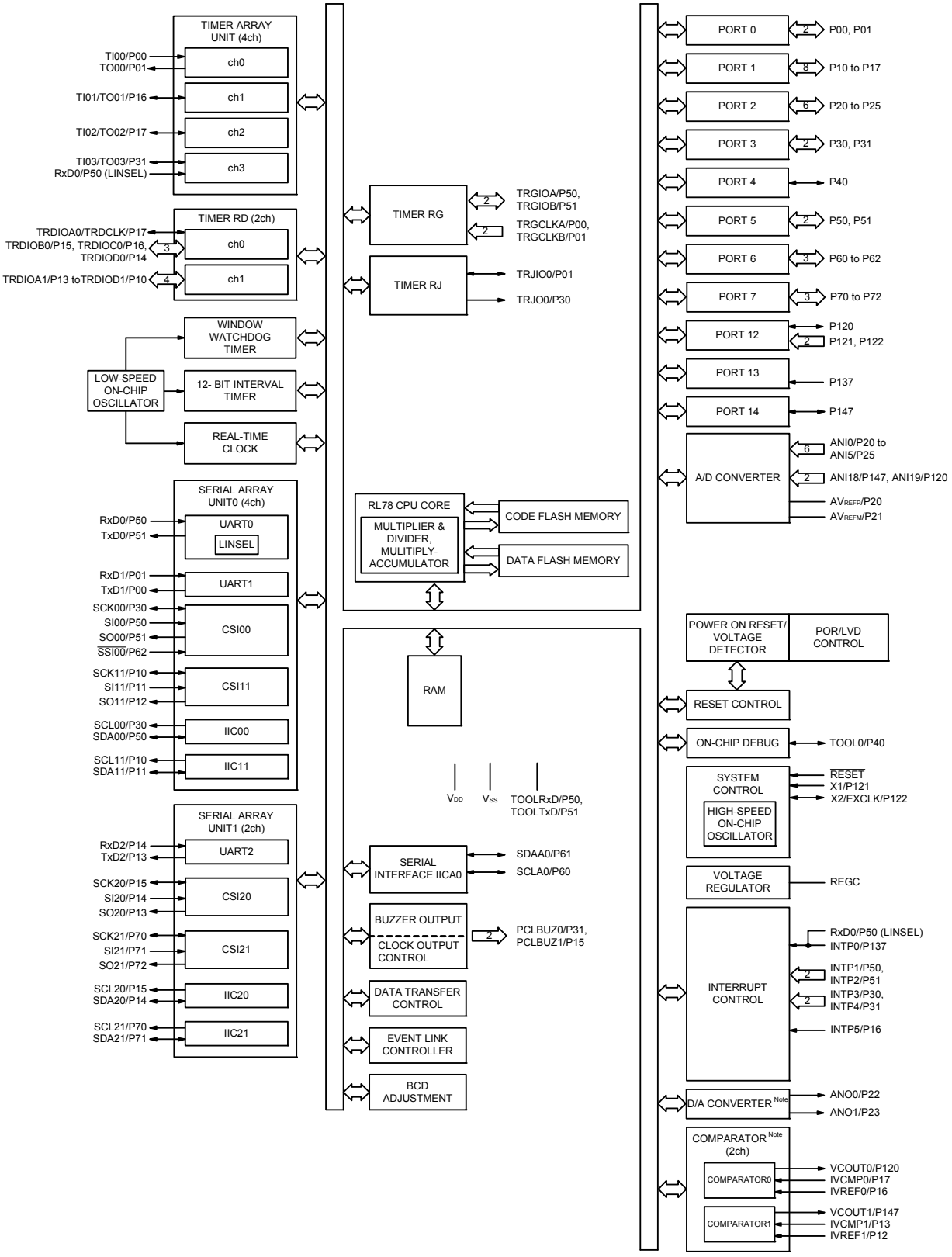
Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.3 36-pin products



Note Mounted on the 96 KB or more code flash memory products.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

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Item		44-pin R5F104Fx (x = F to H, J)	48-pin R5F104Gx (x = F to H, J)	52-pin R5F104Jx (x = F to H, J)	64-pin R5F104Lx (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256	96 to 256	96 to 256
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 24 Note	12 to 24 Note	12 to 24 Note	12 to 24 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)			

(**Note** is listed on the next page.)

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Item		48-pin R5F104Gx (x = K, L)	64-pin R5F104Lx (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		10 channels	12 channels
D/A converter		2 channels	
Comparator		2 channels	
Serial interface		[48-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels	
	I^2C bus	1 channel	1 channel
Data transfer controller (DTC)		32 sources	33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9	
Vectored interrupt sources	Internal	24	24
	External	10	13
Key interrupt		6	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.0		+5.0	%
		-40 to -20°C	1.8 V ≤ V_{DD} < 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.4		mA
						V_{DD} = 3.0 V		2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		
						V_{DD} = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.1	8.7	mA
						V_{DD} = 3.0 V		5.1	8.7	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	8.1	
						V_{DD} = 3.0 V		4.8	8.1	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	6.9	
						V_{DD} = 3.0 V		4.0	6.9	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.8	6.3	
						V_{DD} = 3.0 V		3.8	6.3	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.6	
						V_{DD} = 3.0 V		2.8	4.6	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.0	mA
						V_{DD} = 2.0 V		1.3	2.0	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA
						Resonator connection		3.4	5.5	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.3	
						Resonator connection		3.4	5.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA
						Resonator connection		1.2	2.0	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.2	1.9	
						Resonator connection		1.2	2.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.7	6.1	µA
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.7	6.1	
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.8	6.7	
						Resonator connection		4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.8	7.5	
						Resonator connection		4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.4	8.9	
						Resonator connection		5.4	8.9	

(**Notes** and **Remarks** are listed on the next page.)

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.9		mA
						V_{DD} = 3.0 V		2.9		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.5		
						V_{DD} = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		6.0	11.2	mA
						V_{DD} = 3.0 V		6.0	11.2	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.5	10.6	
						V_{DD} = 3.0 V		5.5	10.6	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.7	8.6	
						V_{DD} = 3.0 V		4.7	8.6	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.4	8.2	
						V_{DD} = 3.0 V		4.4	8.2	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.3	5.9	
						V_{DD} = 3.0 V		3.3	5.9	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.5	mA
						V_{DD} = 2.0 V		1.5	2.5	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.1	mA
						V_{DD} = 2.0 V		1.5	2.1	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8	
						Resonator connection		3.9	7.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.2		µA
						Resonator connection		5.2		
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(**Notes** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(1) I^2C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		0	3.45	0	3.45	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		4.0		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		4.7		4.7		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

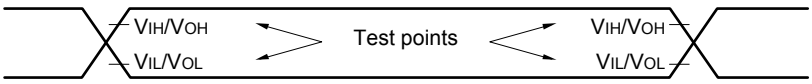
Absolute Maximum Ratings **(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

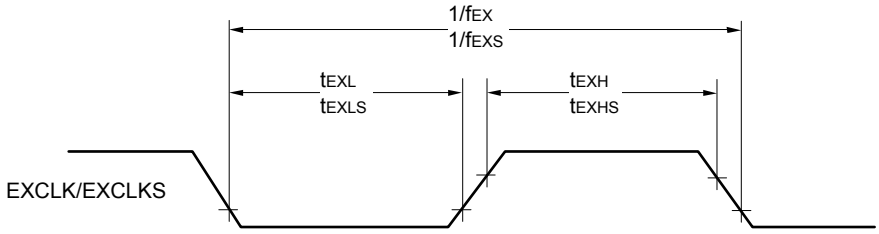
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

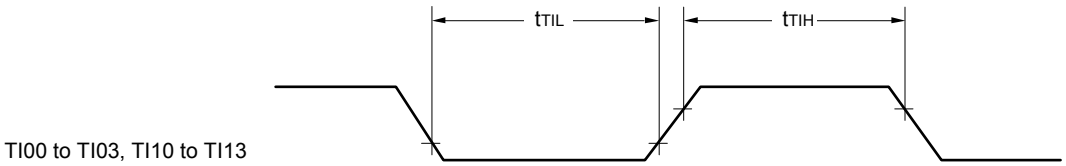
AC Timing Test Points

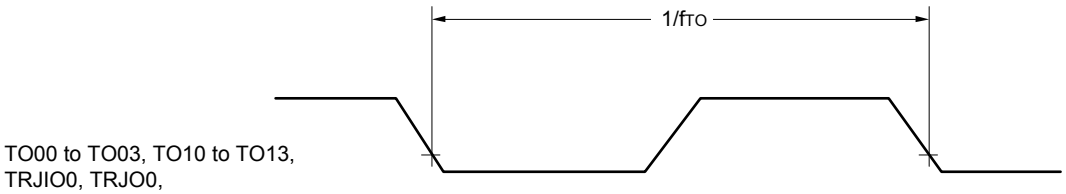


External System Clock Timing



TI/TO Timing





(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	28/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_v = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

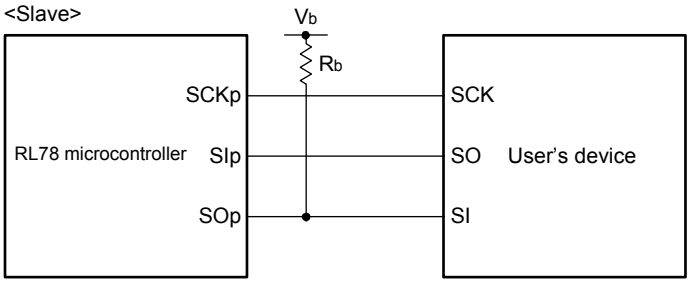
Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		µs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

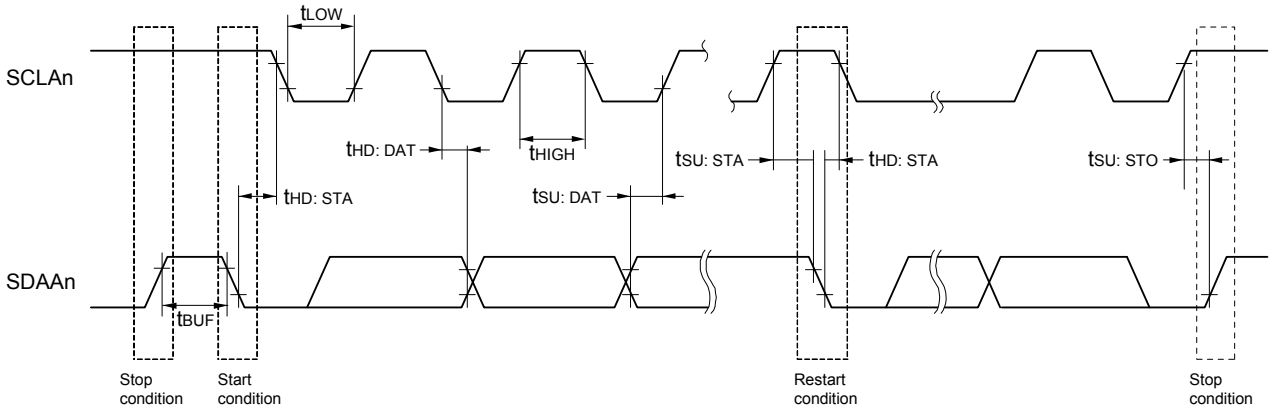
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

3.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

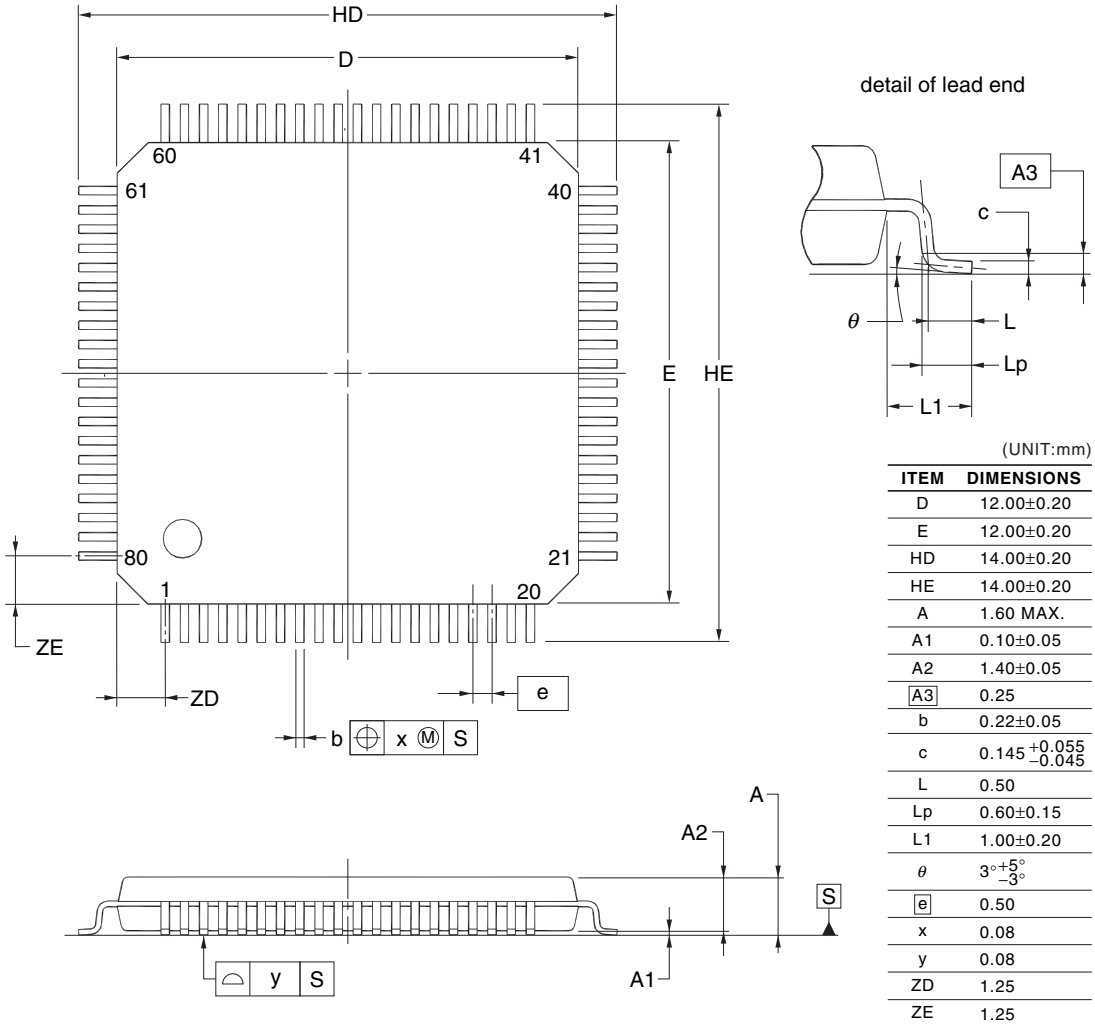
(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	3.90	4.06	4.22	V
			Falling edge	3.83	3.98	4.13	V
		V_{LVD1}	Rising edge	3.60	3.75	3.90	V
			Falling edge	3.53	3.67	3.81	V
		V_{LVD2}	Rising edge	3.01	3.13	3.25	V
			Falling edge	2.94	3.06	3.18	V
		V_{LVD3}	Rising edge	2.90	3.02	3.14	V
			Falling edge	2.85	2.96	3.07	V
		V_{LVD4}	Rising edge	2.81	2.92	3.03	V
			Falling edge	2.75	2.86	2.97	V
		V_{LVD5}	Rising edge	2.70	2.81	2.92	V
			Falling edge	2.64	2.75	2.86	V
		V_{LVD6}	Rising edge	2.61	2.71	2.81	V
			Falling edge	2.55	2.65	2.75	V
		V_{LVD7}	Rising edge	2.51	2.61	2.71	V
			Falling edge	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

4.9 80-pin products

R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
R5F104MFDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.