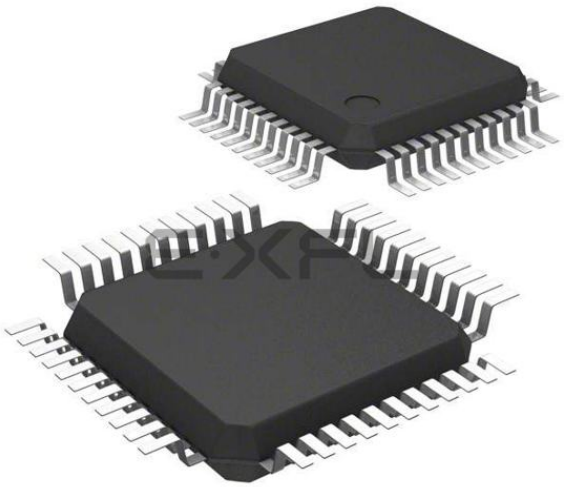
Renesas Electronics America Inc - R5F104FEAFP#50 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104feafp-50

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G14			
			30 pins	32 pins	36 pins	40 pins
192 KB	8 KB	20 KB	—	—	—	R5F104EH
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA

Flash ROM	Data flash	RAM	RL78/G14			
			44 pins	48 pins	52 pins	64 pins
512 KB	8 KB	48 KB Note	—	R5F104GL	—	R5F104LL
384 KB	8 KB	32 KB	—	R5F104GK	—	R5F104LK
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	—	—

Flash ROM	Data flash	RAM	RL78/G14	
			80 pins	100 pins
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL
384 KB	8 KB	32 KB	R5F104MK	R5F104PK
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

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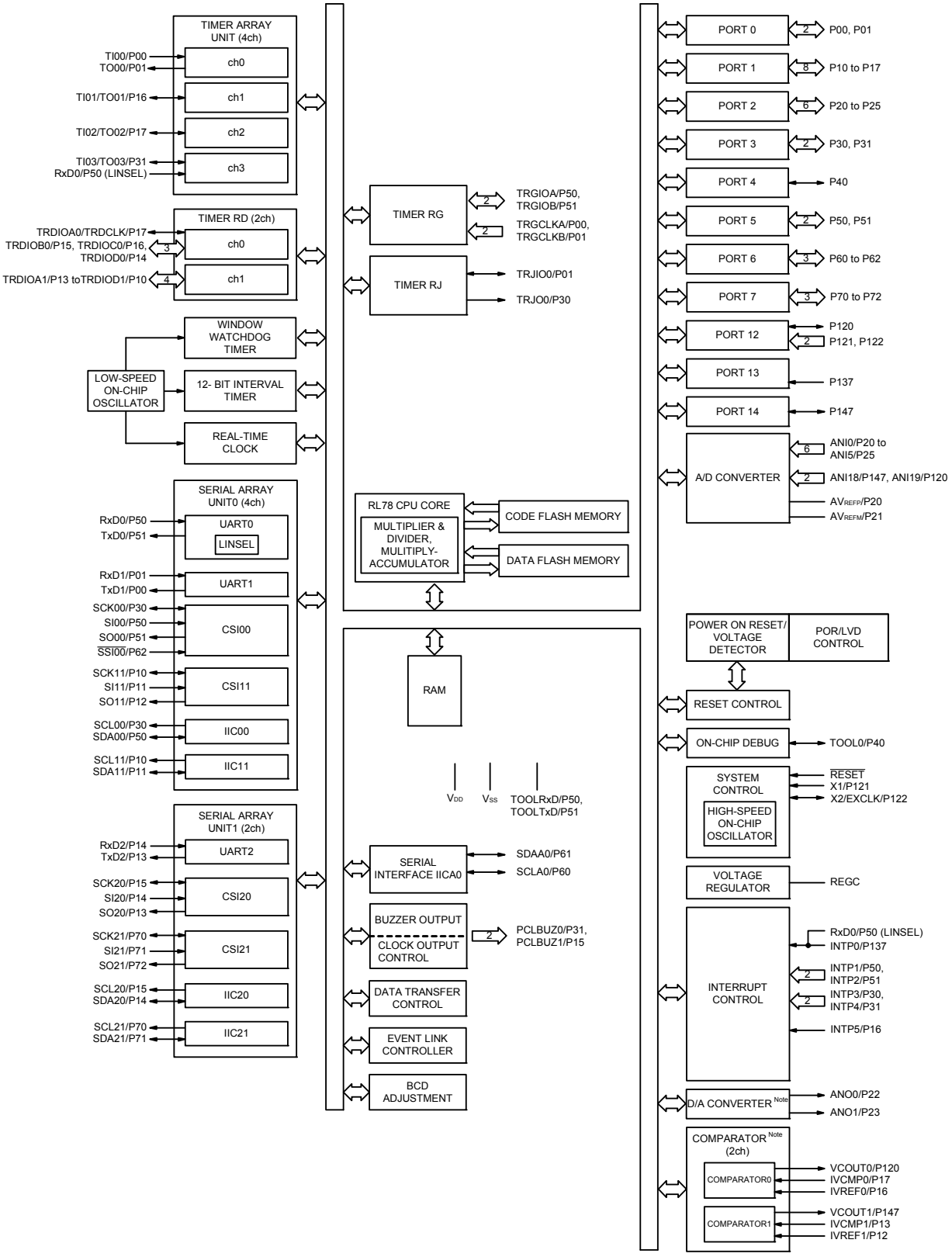
Pin count	Package	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFB#V0, R5F104MJAFB#V0 R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFB#X0, R5F104MJAFB#X0 R5F104MKAFB#30, R5F104MLAFB#30 R5F104MKAFB#50, R5F104MLAFB#50
		D	R5F104MFDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0 R5F104MFDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0
		G	R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0 R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0 R5F104MKGFB#30, R5F104MLGFB#30 R5F104MKGFB#X0, R5F104MLGFB#50
	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	A	R5F104MFAFA#V0, R5F104MGAFA#V0, R5F104MHAFA#V0, R5F104MJAFA#V0 R5F104MFAFA#X0, R5F104MGAFA#X0, R5F104MHAFA#X0, R5F104MJAFA#X0 R5F104MKAFA#30, R5F104MLAFA#30 R5F104MKAFA#50, R5F104MLAFA#50
		D	R5F104MFDFA#V0, R5F104MGDFA#V0, R5F104MHDFA#V0, R5F104MJDFA#V0 R5F104MFDFA#X0, R5F104MGDFA#X0, R5F104MHDFA#X0, R5F104MJDFA#X0
		G	R5F104MFGFA#V0, R5F104MGGFA#V0, R5F104MHGFA#V0, R5F104MJGFA#V0 R5F104MFGFA#X0, R5F104MGGFA#X0, R5F104MHGFA#X0, R5F104MJGFA#X0 R5F104MKGFA#30, R5F104MLGFA#30 R5F104MKGFA#50, R5F104MLGFA#50
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F104PFAFB#V0, R5F104PGAFB#V0, R5F104PHAFB#V0, R5F104PJAFB#V0 R5F104PFAFB#X0, R5F104PGAFB#X0, R5F104PHAFB#X0, R5F104PJAFB#X0 R5F104PKAFB#30, R5F104PLAFB#30 R5F104PKAFB#50, R5F104PLAFB#50
		D	R5F104PFDFB#V0, R5F104PGDFB#V0, R5F104PHDFB#V0, R5F104PJDFB#V0 R5F104PFDFB#X0, R5F104PGDFB#X0, R5F104PHDFB#X0, R5F104PJDFB#X0
		G	R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0 R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0 R5F104PKGFB#30, R5F104PLGFB#30 R5F104PKGFB#50, R5F104PLGFB#50
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	A	R5F104PFAFA#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFA#V0 R5F104PFAFA#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFA#X0 R5F104PKAFA#30, R5F104PLAFA#30 R5F104PKAFA#50, R5F104PLAFA#50
		D	R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFA#V0 R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFA#X0
		G	R5F104PFGFA#V0, R5F104PGGFA#V0, R5F104PHGFA#V0, R5F104PJGFA#V0 R5F104PFGFA#X0, R5F104PGGFA#X0, R5F104PHGFA#X0, R5F104PJGFA#X0 R5F104PKGFA#30, R5F104PLGFA#30 R5F104PKGFA#50, R5F104PLGFA#50

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

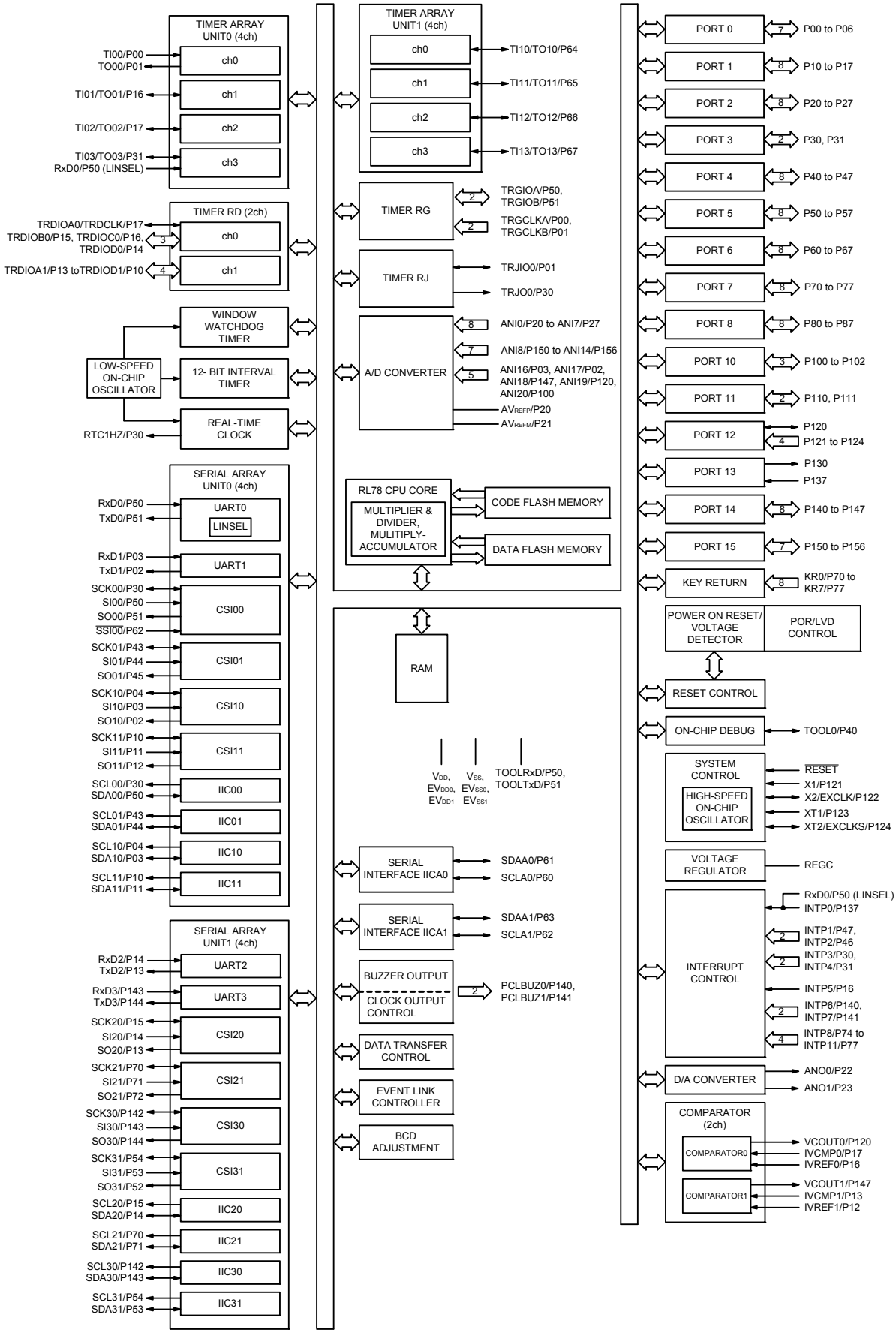
Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

1.5.3 36-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.5.10 100-pin products



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Item		30-pin R5F104Ax (x = F, G)	32-pin R5F104Bx (x = F, G)	36-pin R5F104Cx (x = F, G)	40-pin R5F104Ex (x = F to H)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
D/A converter		1 channel	2 channels		
Comparator		2 channels			
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels			
	I^2C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources			31 sources
Event link controller (ELC)		Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = –40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = –40 to +105°C)			
Operating ambient temperature		T_A = –40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item		80-pin R5F104Mx (x = K, L)	100-pin R5F104Px (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		17 channels	20 channels
D/A converter		2 channels	2 channels
Comparator		2 channels	2 channels
Serial interface		[80-pin, 100-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels	
	I^2C bus	2 channels	2 channels
Data transfer controller (DTC)		39 sources	39 sources
Event link controller (ELC)		Event input: 26 Event trigger output: 9	
Vectored interrupt sources	Internal	32	32
	External	13	13
Key interrupt		8	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. Use it with EV_{DD0} ≥ V_b.

Note 3. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ EV_{DD0} < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_v = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		V_{LVD12}	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		V_{LVD13}	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/2)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV_{DD0} +0.3 and -0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV_{DD0} +0.3 and -0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI20	-0.3 to EV_{DD0} +0.3 and -0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} +0.3 and -0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147				8.5 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				80.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1}, and V_{SS} pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 24		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 36		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

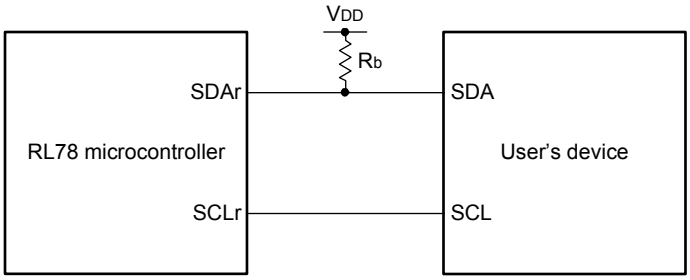
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

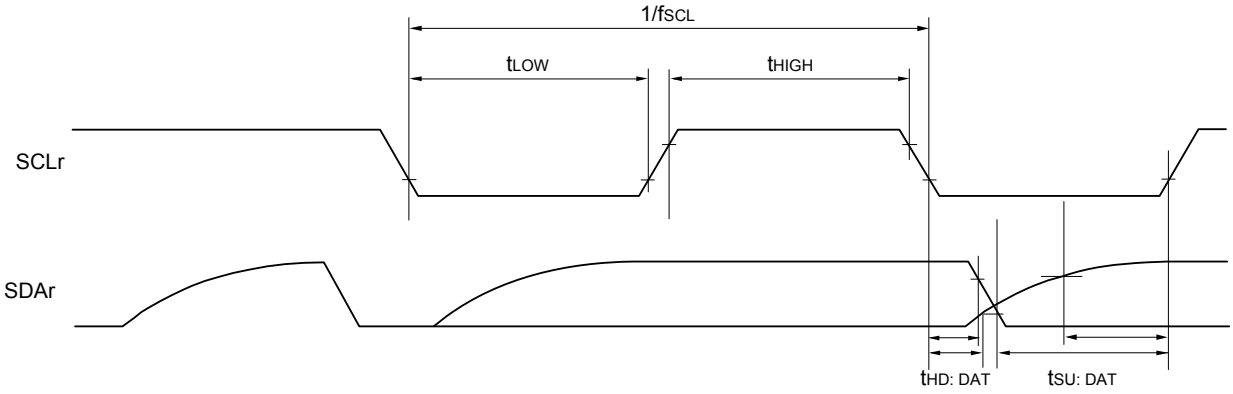
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

Note 5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD0} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

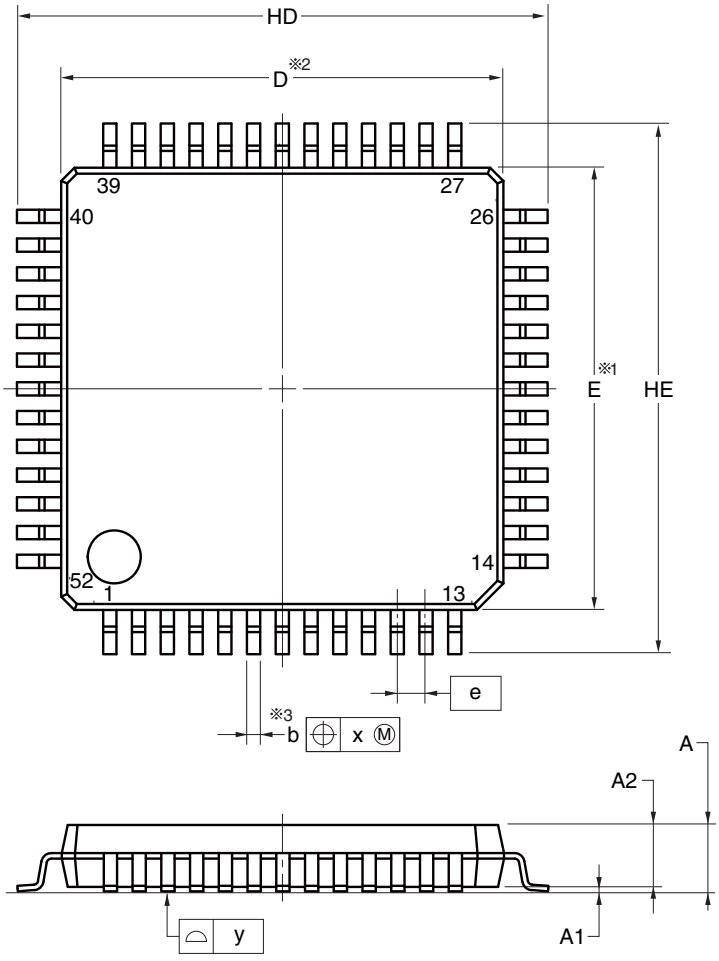
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

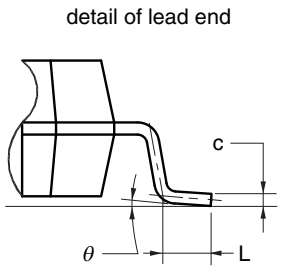
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

REVISION HISTORY	RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Oct 25, 2013	112 to 169	Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS
		171 to 187	Modification of 4.1 30-pin products to 4.10 100-pin products
3.00	Feb 07, 2014	All	Addition of products with maximum 512 KB flash ROM and 48 KB RAM
		1	Modification of 1.1 Features
		2	Modification of ROM, RAM capacities and addition of note 3
		3	Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14
		6 to 8	Addition of part number
		15, 16	Modification of 1.3.6 48-pin products
		17	Modification of 1.3.7 52-pin products
		18, 19	Modification of 1.3.8 64-pin products
		20	Modification of 1.3.9 80-pin products
		21, 22	Modification of 1.3.10 100-pin products
		35, 37, 39, 41, 43, 45, 47	Modification of operating ambient temperature in 1.6 Outline of Functions
		42, 43	Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB)
		46, 47	Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB)
		65 to 68	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products
		118	Modification of 2.7 Data Memory Retention Characteristics
		137 to 140	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products
		180	Modification of 3.7 Data Memory Retention Characteristics
		189, 190	Addition and modification of 4.6 48-pin products
		191	Modification of 4.7 52-pin products
		193 to 195	Addition and modification of 4.8 64-pin products
		198, 199	Addition and modification of 4.9 80-pin products
		201, 202	Addition and modification of 4.10 100-pin products
3.20	Jan 05, 2015	p.2	Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note
		p.6	Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information
		p.6 to 8	Deletion of note 2 in 1.2 Ordering Information
		p.17	Deletion of note 2 in 1.3.7 52-pin products
		p.36, 39, 42, 45, 48, 50, 52	Modification of description in 1.6 Outline of Functions
		p.46, 48	Deletion of description of 52-pin in 1.6 Outline of Functions
		p.47	Modification of note of 1.6 Outline of Functions
		p.62, 64, 66, 68, 70, 72	Modification of specifications in 2.3.2 Supply current characteristics