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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104feafp-v0

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G14			
			30 pins	32 pins	36 pins	40 pins
192 KB	8 KB	20 KB	—	—	—	R5F104EH
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA

Flash ROM	Data flash	RAM	RL78/G14			
			44 pins	48 pins	52 pins	64 pins
512 KB	8 KB	48 KB Note	—	R5F104GL	—	R5F104LL
384 KB	8 KB	32 KB	—	R5F104GK	—	R5F104LK
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	—	—

Flash ROM	Data flash	RAM	RL78/G14	
			80 pins	100 pins
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL
384 KB	8 KB	32 KB	R5F104MK	R5F104PK
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

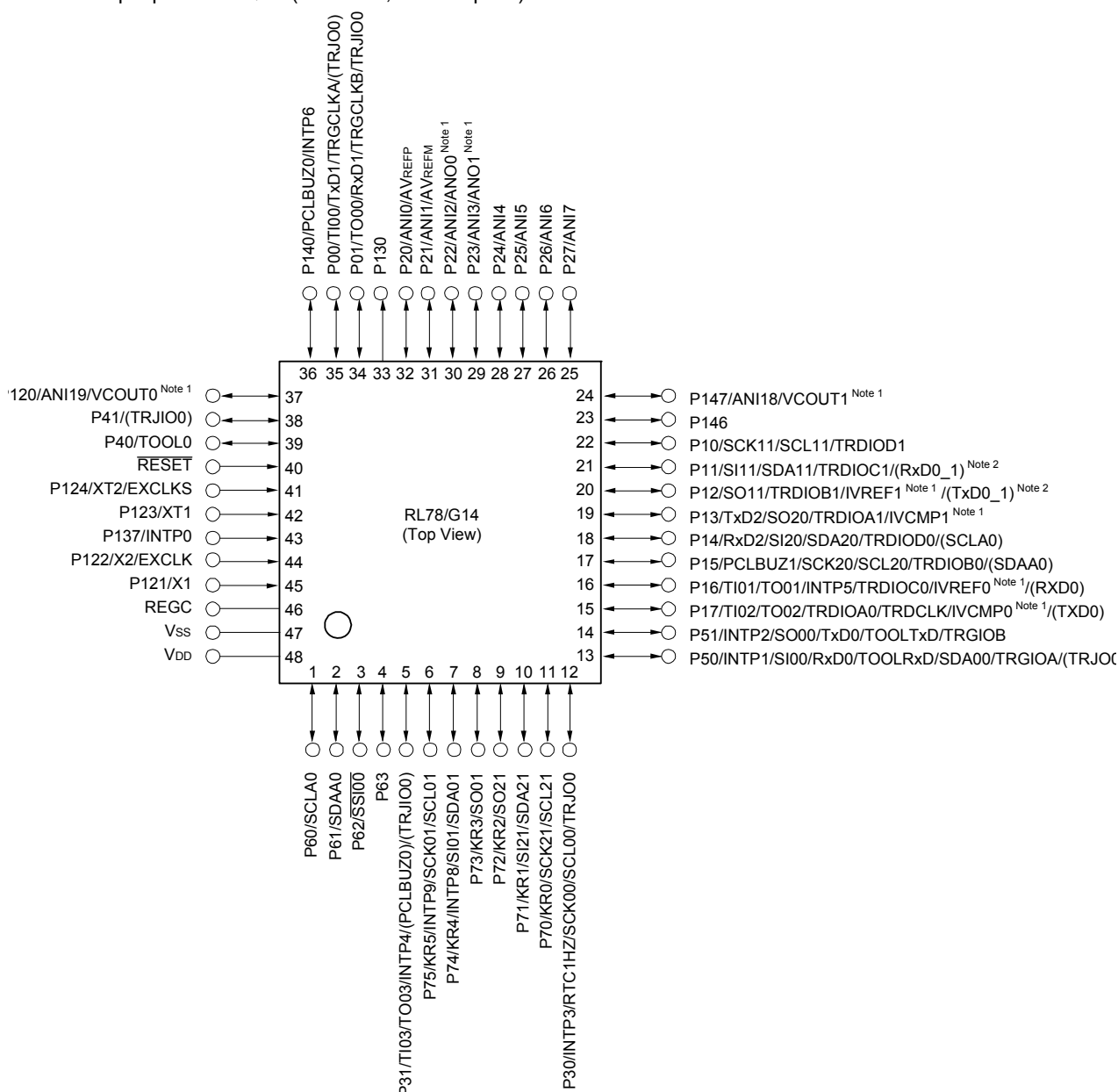R5F104xE (x = A to C, E to G, J, L): Start address FE900H

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.3.6   48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

RL78/G14
(Top View)

Top pins (left to right, 36–25):
- 36 P140/PCLBUZ0/INTP6
- 35 P00/TI00/TxD1/TRGCLKA(TRJIO0)
- 34 P01/TO00/RxD1/TRGCLKB/TRJIO0
- 33 P130
- 32 P20/ANI0/AV$_{REFP}$
- 31 P21/ANI1/AV$_{REFM}$
- 30 P22/ANI2/ANO0 $^{Note 1}$
- 29 P23/ANI3/ANO1 $^{Note 1}$
- 28 P24/ANI4
- 27 P25/ANI5
- 26 P26/ANI6
- 25 P27/ANI7

Left pins (top to bottom, 37–48):
- 37 P120/ANI19/VCOUT0 $^{Note 1}$
- 38 P41/(TRJIO0)
- 39 P40/TOOL0
- 40 $\overline{RESET}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 V$_{SS}$
- 48 V$_{DD}$

Right pins (top to bottom, 24–13):
- 24 P147/ANI18/VCOUT1 $^{Note 1}$
- 23 P146
- 22 P10/SCK11/SCL11/TRDIOD1
- 21 P11/SI11/SDA11/TRDIOC1/(RxD0_1) $^{Note 2}$
- 20 P12/SO11/TRDIOB1/IVREF1 $^{Note 1}$/(TxD0_1) $^{Note 2}$
- 19 P13/TxD2/SO20/TRDIOA1/IVCMP1 $^{Note 1}$
- 18 P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
- 17 P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
- 16 P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 $^{Note 1}$/(RXD0)
- 15 P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 $^{Note 1}$/(TXD0)
- 14 P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
- 13 P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0

Bottom pins (left to right, 1–12):
- 1 P60/SCLA0
- 2 P61/SDAA0
- 3 P62/$\overline{SSI00}$
- 4 P63
- 5 P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)
- 6 P75/KR5/INTP9/SCK01/SCL01
- 7 P74/KR4/INTP8/SI01/SDA01
- 8 P73/KR3/SO01
- 9 P72/KR2/SO21
- 10 P71/KR1/SI21/SDA21
- 11 P70/KR0/SCK21/SCL21
- 12 P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0

Note 1.   Mounted on the 96 KB or more code flash memory products.
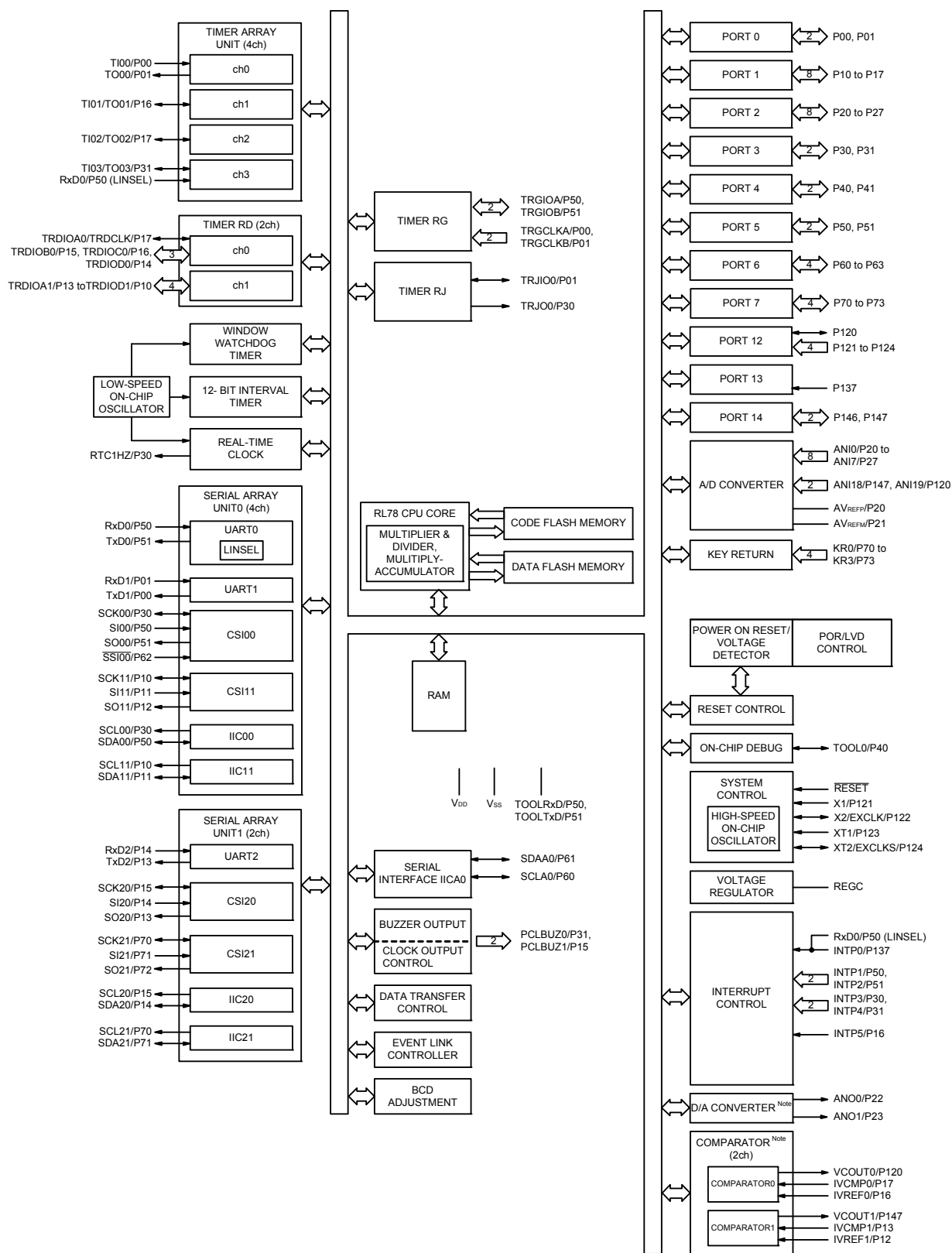**Note 2.**   Mounted on the 384 KB or more code flash memory products.

Caution   Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.5   44-pin products

Note   Mounted on the 96 KB or more code flash memory products.

Note   The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

   R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[80-pin, 100-pin products (code flash memory 96 KB to 256 KB)]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256
Data flash memory (KB)		8	8
RAM (KB)		12 to 24 Note	12 to 24 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 µs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)	
		0.05 µs (High-speed system clock: f_{MX} = 20 MHz operation)	
		30.5 µs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Note   In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(T$_A$ = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I$_{OL1}$	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147				20.0 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			70.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			15.0	mA
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			9.0	mA
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			80.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			35.0	mA
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			20.0	mA
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			10.0	mA
		Total of all pins (When duty $\leq$ 70% Note 3)				150.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P156				0.4 Note 2	mA
		Total of all pins (When duty $\leq$ 70% Note 3)	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$, EV$_{SS1}$, and V$_{SS}$ pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor $\leq$ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)
   <Example>   Where n = 80% and I$_{OL}$ = 10.0 mA
                Total output current of pins = (10.0 × 0.7)/(80 × 0.01) $\approx$ 8.7 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4		mA
						VDD = 3.0 V		2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1		
						VDD = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7	mA
						VDD = 3.0 V		5.1	8.7	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1	
						VDD = 3.0 V		4.8	8.1	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9	
						VDD = 3.0 V		4.0	6.9	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3	
						VDD = 3.0 V		3.8	6.3	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6	
						VDD = 3.0 V		2.8	4.6	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0	mA
						VDD = 2.0 V		1.3	2.0	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8	mA
						VDD = 2.0 V		1.3	1.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA
						Resonator connection		3.4	5.5	
				f_{MX} = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3	
						Resonator connection		3.4	5.5	
				f_{MX} = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
				f_{MX} = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA
						Resonator connection		1.2	2.0	
				f_{MX} = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9	
						Resonator connection		1.2	2.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4, TA = -40°C	Normal operation	Square wave input		4.7	6.1	μA
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4, TA = +25°C	Normal operation	Square wave input		4.7	6.1	
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4, TA = +50°C	Normal operation	Square wave input		4.8	6.7	
						Resonator connection		4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4, TA = +70°C	Normal operation	Square wave input		4.8	7.5	
						Resonator connection		4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4, TA = +85°C	Normal operation	Square wave input		5.4	8.9	
						Resonator connection		5.4	8.9	

(**Notes** and **Remarks** are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = -40 to +85°C, 2.7 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ 2/f$_{CLK}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	62.5		250		500		ns
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 7		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 10		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		23		110		110		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 20 pF Note 4			10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with EV$_{DD0}$ ≥ V$_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)
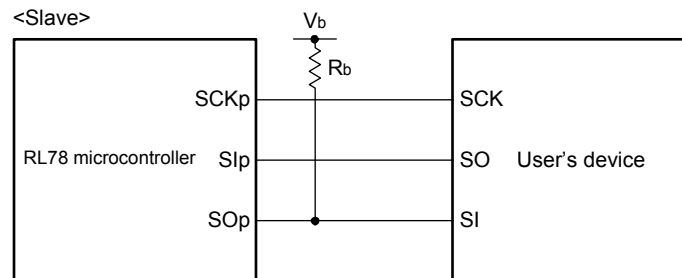
Remark 1. R$_b$[Ω]: Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(T$_A$ = -40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 [Note 1]		300 [Note 1]		300 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 [Note 1]		300 [Note 1]		300 [Note 1]	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		400 [Note 1]		300 [Note 1]		300 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		400 [Note 1]		300 [Note 1]		300 [Note 1]	kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		300 [Note 1]		300 [Note 1]		300 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	610		610		610		ns

3.2 Oscillator Characteristics

3.2.1 X1, XT1 characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, Vss = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (fxT) Note	Crystal resonator		32	32.768	35	kHz

Note   Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

3.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, Vss = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fIH			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ VDD ≤ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	2.4 V ≤ VDD ≤ 5.5 V	-1.5		+1.5	%
		+85 to +105°C	2.4 V ≤ VDD ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1.   High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2.   This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(T_A = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0.8 EV$_{DD0}$		EV$_{DD0}$	V
	V$_{IH2}$	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	2.2		EV$_{DD0}$	V
			TTL input buffer 3.3 V $\leq$ EV$_{DD0}$ < 4.0 V	2.0		EV$_{DD0}$	V
			TTL input buffer 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V	1.5		EV$_{DD0}$	V
	V$_{IH3}$	P20 to P27, P150 to P156		0.7 V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P63		0.7 EV$_{DD0}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8 V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0		0.2 EV$_{DD0}$	V
	V$_{IL2}$	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V $\leq$ EV$_{DD0}$ < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P27, P150 to P156		0		0.3 V$_{DD}$	V
	V$_{IL4}$	P60 to P63		0		0.3 EV$_{DD0}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2 V$_{DD}$	V

Caution   **The maximum value of V$_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EV$_{DD0}$, even in the N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = -40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.6		mA
						V_{DD} = 3.0 V		2.6		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.3		
						V_{DD} = 3.0 V		2.3		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.4	10.9	mA
						V_{DD} = 3.0 V		5.4	10.9	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.0	10.3	
						V_{DD} = 3.0 V		5.0	10.3	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.2	8.2	
						V_{DD} = 3.0 V		4.2	8.2	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	7.8	
						V_{DD} = 3.0 V		4.0	7.8	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.0	5.6	
						V_{DD} = 3.0 V		3.0	5.6	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	6.6	mA
						Resonator connection		3.6	6.7	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	6.6	
						Resonator connection		3.6	6.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.9	
						Resonator connection		2.2	4.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.9	
						Resonator connection		2.2	4.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.9	7.1	µA
						Resonator connection		4.9	7.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	7.1	
						Resonator connection		4.9	7.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.1	8.8	
						Resonator connection		5.1	8.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	10.5	
						Resonator connection		5.5	10.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.5	14.5	
						Resonator connection		6.5	14.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		13.0	58.0	
						Resonator connection		13.0	58.0	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
                                 2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 [Note 1]	kHz
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU: DAT}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 [Note 2]		ns
		2.4V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 [Note 2]		ns
Data hold time (transmission)	$t_{HD: DAT}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1.   The value must also be equal to or less than f_{MCK}/4.

Note 2.   Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   **Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

3.6   Analog Characteristics

3.6.1   A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (-) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (-) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (-)= AV$_{REFM}$
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI20	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ AV$_{REFP}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (-) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V		1.2	±3.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	2.125		39	μs
			2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	3.1875		39	μs
			2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	2.375		39	μs
			2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	3.5625		39	μs
			2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±0.25	%FSR
Full-scale error [Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±0.25	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V $\leq$ AV$_{REFP}$ $\leq$ 5.5 V			±1.5	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage output (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 4]		V
		Temperature sensor output voltage (2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 4]		V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3.   When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
       Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
       Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
       Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Note 4.   Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

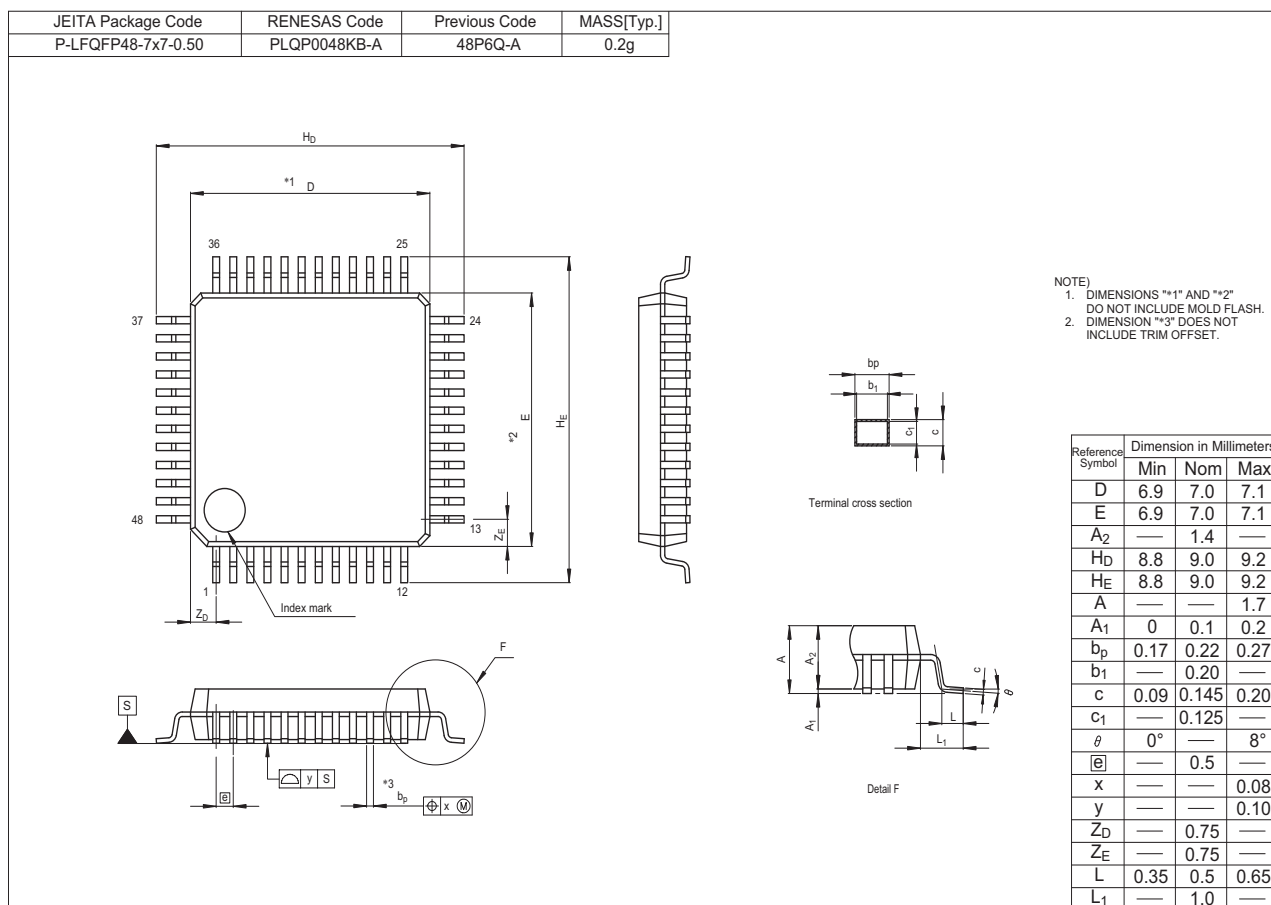| Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V $\leq$ V_{DD} $\leq$ 5.5 V	2.125		39	μs
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V	3.1875		39	μs
			2.4 V $\leq$ V_{DD} $\leq$ 5.5 V	17		39	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V $\leq$ V_{DD} $\leq$ 5.5 V	2.375		39	μs
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V	3.5625		39	μs
			2.4 V $\leq$ V_{DD} $\leq$ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E_{ZS}	10-bit resolution	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±0.60	%FSR
Full-scale error [Notes 1, 2]	E_{FS}	10-bit resolution	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±0.60	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±4.0	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
		Internal reference voltage (2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, HS (high-speed main) mode)			V_{BGR} [Note 3]		V
		Temperature sensor output voltage (2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, HS (high-speed main) mode)			V_{TMPS25} [Note 3]		V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

R5F104GKAFB, R5F104GLAFB
R5F104GKGFB, R5F104GLGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g

NOTE)
1. DIMENSIONS "*1" AND "*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT
   INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

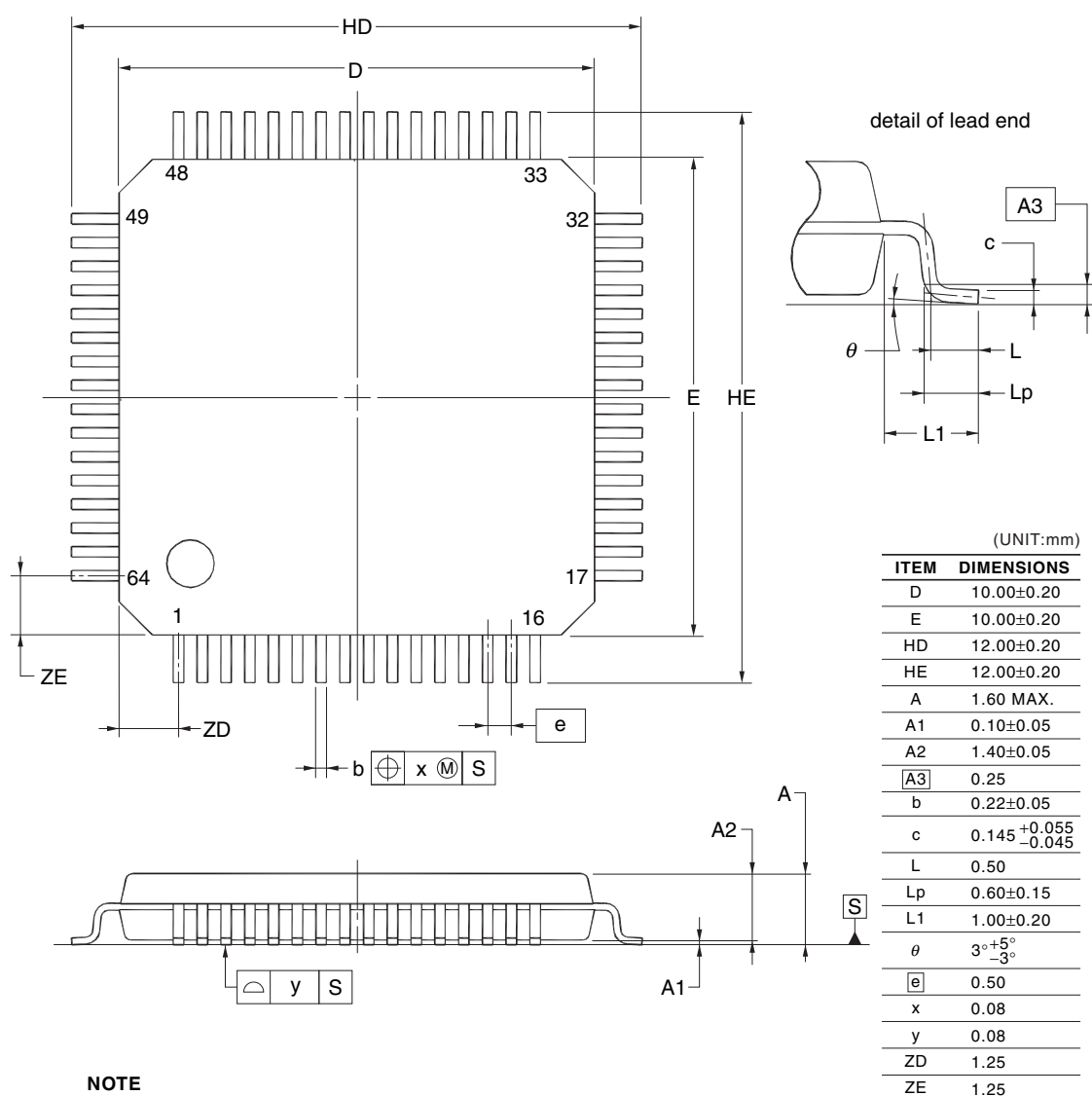| Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB, R5F104LJAFB

R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB, R5F104LJDFB

R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB, R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

detail of lead end

(UNIT:mm)	
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.