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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104feafp-x0

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

○ ROM, RAM capacities

Elash ROM	Data flach	PAM	RL78/G14					
T IdSIT KOW	Data liasii	rv/alvi	30 pins	32 pins	36 pins	40 pins		
192 KB	8 KB	20 KB	—	—	—	R5F104EH		
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG		
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF		
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE		
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED		
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC		
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA		

Elash ROM	Data flach	PAM		RL78/G14				
T Idolf TOW	Data liasii		44 pins	48 pins	52 pins	64 pins		
512 KB	8 KB	48 KB Note		R5F104GL	—	R5F104LL		
384 KB	8 KB	32 KB	_	R5F104GK	—	R5F104LK		
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ		
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH		
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG		
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF		
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE		
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD		
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC		
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	_			

Elach DOM	Data flach	DAM	RL78/G14			
T IdSIT KOW	Data hash		80 pins	100 pins		
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL		
384 KB	8 KB	32 KB	R5F104MK	R5F104PK		
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ		
192 KB	8 KB	20 KB	R5F104MH	R5F104PH		
128 KB	8 KB	16 KB	R5F104MG	R5F104PG		
96 KB	8 KB	12 KB	R5F104MF	R5F104PF		

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).



1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.



2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	IOH1 Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P111, P120, P130, P140 to Total of P00 to P04, P40 to P	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$1.6 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$			-10.0 Note 2	mA
		Total of P00 to P04, P40 to P47,	$4.0~V \leq EV_{DD0} \leq 5.5~V$			-55.0	mA
		P102, P120, P130, P140 to P145	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} < 4.0 \text{ V}$			-10.0	mA
		(when $auty \leq 70\%$ Note 5)	$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} < 2.7 \text{ V}$			-5.0	mA
			$1.6 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V}$			-2.5	mA
		Total of P05, P06, P10 to P17, 4	$4.0~V \leq EV_{DD0} \leq 5.5~V$			-80.0	mA
		P30, P31, P50 to P57,	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 4.0 \text{ V}$			-19.0	mA
		P64 to P67, P70 to P77, P80 to P87 P100 P101 P110	$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V}$			-10.0	mA
		P111, P146, P147 (When duty \leq 70% ^{Note 3})	$1.6 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V}$			-5.0	mA
		Total of all pins (When duty \leq 70% ^{Note 3})	$1.6 \text{ V} \le \text{EVDD0} \le 5.5 \text{ V}$			-135.0 Note 4	mA
	Іон2	Per pin for P20 to P27, P150 to P156	$1.6 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$			-0.1 Note 2	mA
		Total of all pins (When duty \leq 70% ^{Note 3})	$1.6 \text{ V} \le \text{VDD} \le 5.5 \text{ V}$			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%. The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = $(IOH \times 0.7)/(n \times 0.01)$ <Example> Where n = 80% and IOH = -10.0 mA Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Note 4. -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.



Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Parameter	Symbol	Conditions		HS (high-s main) mo	peed ode	LS (low-speed mode	d main)	LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkcy1 tkcy1 ≥ 4/fclk		$2.7~V \leq E_{VDD0} \leq 5.5~V$	125		500		1000		ns
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	250		500		1000		ns
			$1.8~V \leq EV_{DD0} \leq 5.5~V$	500		500		1000		ns
			$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	1000		1000		1000		ns
			$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	—		1000		1000		ns
SCKp high-/low-level	tĸнı,	$4.0 \text{ V} \leq \text{EV}_{\text{DDO}}$	0 ≤ 5.5 V	tксү1/2 - 12		tксү1/2 - 50		tксү1/2 - 50		ns
width	tKL1	$2.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	tксү1/2 - 18		tксү1/2 - 50		tксү1/2 - 50		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү1/2 - 38		tксү1/2 - 50		tксү1/2 - 50		ns
		$1.8~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$		tксү1/2 - 50		tксү1/2 - 50		tксү1/2 - 50		ns
	$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		tксү1/2 - 100		tксү1/2 - 100		tксү1/2 - 100		ns	
		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		—		tксү1/2 - 100		tксү1/2 - 100		ns
SIp setup time	tsik1	$4.0 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	44		110		110		ns
(to SCKp↑) ^{Note 1}		$2.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	44		110		110		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	75		110		110		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	110		110		110		ns
		$1.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	220		220		220		ns
		$1.6 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	—		220		220		ns
SIp hold time	tksi1	$1.7 \text{ V} \leq \text{EV}_{\text{DDC}}$	$\leq 5.5 V$	19		19		19		ns
(from SCKp↑) Note 2		$1.6 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	—		19		19		ns
Delay time from SCKp↓ to SOp output	tkso1	$1.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$ C = 30 pF Note 4			25		25		25	ns
		$1.6 V \le EV_{DDC}$ C = 30 pF Note	o ≤ 5.5 V e 4		_		25		25	ns

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) (TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

- **Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
 - h: POM number (h = 0, 1, 3 to 5, 7, 14)
- Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)



Parameter	Symbol	Conditions	HS (high- n	speed main) node	LS (low-s	speed main) 10de	LV (low-v m	oltage main) node	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	t
SCLr clock frequency	fscL	$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		1000 Note 1		300 Note 1		300 Note 1	kHz
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		1000 Note 1		300 Note 1		300 Note 1	kHz
		$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 100 \; pF, \; R_b = 2.8 \; k\Omega \end{array}$		400 Note 1		300 Note 1		300 Note 1	kHz
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		400 Note 1		300 Note 1		300 Note 1	kHz
		$\label{eq:VD} \begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V \ \text{Note 2}, \\ C_b = 100 \ \text{pF}, \ R_b = 5.5 \ \text{k}\Omega \end{array}$		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t∟ow		475		1550		1550		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	475		1550		1550		ns
			1150		1550		1550		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	1150		1550		1550		ns
		$\label{eq:linear} \begin{split} & 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ & 1.6 \ V \leq V_b \leq 2.0 \ V \ \text{Note 2}, \\ & C_b = 100 \ \text{pF}, \ R_b = 5.5 \ \text{k}\Omega \end{split}$	1550		1550		1550		ns
Hold time when SCLr = "H"	tніgн	$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	245		610		610		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	200		610		610		ns
			675		610		610		ns
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	600		610		610		ns
			610		610		610		ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified l²C mode) (TA = -40 to +85°C, 1.8 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)



(2) Interrupt & Reset Mode

(TA = -40 to +85°C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol		Condi	tions	MIN.	TYP.	MAX.	Unit
Voltage detection	VLVDA0	VPOC2,	VPOC1, VPOC0 = 0, 0, 0, fal	ling reset voltage	1.60	1.63	1.66	V
threshold	VLVDA1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC2,	VPOC1, VPOC0 = 0, 0, 1, fal	POC1, VPOC0 = 0, 0, 1, falling reset voltage		1.84	1.87	V
	VLVDB1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3		LVIS1, LVIS0 = 0, 0 F	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC2,	2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage			2.45	2.50	V
	VLVDC1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDC3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	VLVDD0	VPOC2,	VPOC1, VPOC0 = 0, 1, 1, fal	ling reset voltage	2.70	2.75	2.81	V
	VLVDD1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	VLVDD3	1	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.6.7 Power supply voltage rising slope characteristics

(TA = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.



ΙΑ = - 40 ι	0 +105	C , Z .4 V ≤ 1		$500 = 20001 \le 000 \le 5.5 0, 000 = 20001 = 0.0 0$					(2/2)
Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply cur-	IDD2	HALT mode	HS (high-speed main)	fносо = 64 MHz,	V _{DD} = 5.0 V		0.79	4.86	mA
rent Note 1	Note 2		mode Note 7	fiн = 32 MHz ^{Note 4}	V _{DD} = 3.0 V		0.79	4.86	
				fносо = 32 MHz,	VDD = 5.0 V		0.49	4.17	
				fiн = 32 MHz Note 4	V _{DD} = 3.0 V		0.49	4.17	
				fносо = 48 MHz,	VDD = 5.0 V		0.62	3.82	
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.62	3.82	
				fносо = 24 MHz,	V _{DD} = 5.0 V		0.4	3.25	
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.4	3.25	
			fносо = 16 MHz,	VDD = 5.0 V		0.38	2.28	1	
				fiн = 16 MHz Note 4	V _{DD} = 3.0 V		0.38	2.28	
			HS (high-speed main)	f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.30	2.65	mA
			mode Note 7	VDD = 5.0 V	Resonator connection		0.40	2.77	
				f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.30	2.65	
				VDD = 3.0 V	Resonator connection		0.40	2.77	7
				f _{MX} = 10 MHz Note 3,	Square wave input		0.20	1.36	
				VDD = 5.0 V	Resonator connection		0.25	1.46	
				f _{MX} = 10 MHz ^{Note 3} ,	Square wave input		0.20	1.36	
				VDD = 3.0 V	Resonator connection		0.25	1.46	
	Subsystem clock oper	fsub = 32.768 kHz ^{Note 5} ,	Square wave input		0.28	0.66	μA		
			ation	TA = -40°C	Resonator connection		0.47	0.85	
				fsu <mark>B = 32.768 kHz ^{Note 5},</mark> TA = +25°C	Square wave input		0.34	0.66	
					Resonator connection		0.53	0.85	1
				fsue = 32.768 kHz Note 5,	Square wave input		0.37	2.35	
				TA = +50°C	Resonator connection		0.56	2.54	
				fsue = 32.768 kHz Note 5,	Square wave input		0.61	4.08	
				TA = +70°C	Resonator connection		0.80	4.27	
				fsue = 32.768 kHz Note 5,	Square wave input		1.55	8.09	
				TA = +85°C	Resonator connection		1.74	8.28	1
				fsue = 32.768 kHz Note 5,	Square wave input		6.00	51.00	
				TA = +105°C	Resonator connection		6.00	51.00	
	IDD3	STOP mode	TA = -40°C	·			0.19	0.57	μΑ
	Note 6	Note 8	TA = +25°C				0.25	0.57	
			TA = +50°C				0.33	2.26	
			TA = +70°C				0.52	3.99	
	T _A = +8	TA = +85°C				1.46	8.00	1	
			TA = +105°C				5.50	50.00]

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(Notes and Remarks are listed on the next page.)

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)								
Parameter	Symbol		Conditions	HS (high-speed	l main) mode	Unit		
				MIN.	MAX.			
SSI00 setup time	tssik	DAPmn = 0	$2.7~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	240		ns		
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	400		ns		
		DAPmn = 1	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	1/fмск + 240		ns		
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	1/fмск + 400		ns		
SSI00 hold time	tĸssi	DAPmn = 0	$2.7~V \leq EV_{DD0} \leq 5.5~V$	1/fмск + 240		ns		
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	1/fмск + 400		ns		
		DAPmn = 1	$2.7~V \leq EV_{DD0} \leq 5.5~V$	240		ns		
			$2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	400		ns		

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential) (Slave Transmission of slave select input function (CSI00))

SCK00	 SCK
SI00 RL78 microcontroller SO00	SO User's device SI
<u>SSI00</u>	<u>SSO</u>

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31) Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)



The smaller maximum transfer rate derived by using fMck/12 or the following expression is the valid maximum transfer Note 5. rate.

Expression for calculating the transfer rate when 2.4 V \leq EVDD0 < 3.3 V and 1.6 V \leq Vb \leq 2.0 V

1

Maximum transfer rate =
$$\frac{1.5}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$

Baud rate e

$$\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}$$

$$(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Note 6. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.
- Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin Caution products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V) (3/3)				(3/3)	
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↓) ^{Note}	tsiк1		88		ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 30 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	88		ns
		$\begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 30 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$	220		ns
SIp hold time (from SCKp↓) ^{Note}	tksi1		38		ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 30 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	38		ns
		$\label{eq:2.4} \begin{array}{l} 2.4 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	tkso1			50	ns
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 30 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		50	ns
		$\begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 30 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Remarks are listed on the next page.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential



- **Remark 5.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
- **Remark 6.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 7. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
- Remark 8. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.





CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
 Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.



4.6 48-pin products

R5F104GAAFB, R5F104GCAFB, R5F104GDAFB, R5F104GEAFB, R5F104GFAFB, R5F104GGAFB, R5F104GHAFB, R5F104GJAFB

R5F104GADFB, R5F104GCDFB, R5F104GDDFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB, R5F104GHDFB, R5F104GJDFB

R5F104GAGFB, R5F104GCGFB, R5F104GDGFB, R5F104GEGFB, R5F104GFGFB, R5F104GGGFB, R5F104GHGFB, R5F104GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.



ZE

0.75

4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFA, R5F104LHAFA, R5F104LJAFA R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFA, R5F104LHDFA, R5F104LJDFA R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA R5F104LKAFA, R5F104LLAFA

R5F104LKGFA, R5F104LLGFA



Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LFDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7



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R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA R5F104MKAFA, R5F104MLAFA R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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REVISION HISTORY

RL78/G14 Datasheet

Boy	Data		Description	
Rev.	Rev. Dale		Summary	
0.01	Feb 10, 2011	—	First Edition issued	
0.02	May 01, 2011	1 to 2	1.1 Features revised	
		3	1.2 Ordering Information revised	
		4 to 13	1.3 Pin Configuration (Top View) revised	
		14	1.4 Pin Identification revised	
		15 to 17	1.5.1 30-pin products to 1.5.3 36-pin products revised	
		23 to 26	1.6 Outline of Functions revised	
0.03	Jul 28, 2011	1	1.1 Features revised	
1.00	Feb 21, 2012	1 to 40	1. OUTLINE revised	
		41 to 97	2. ELECTRICAL SPECIFICATIONS added	
2.00	Oct 25, 2013	1	Modification of 1.1 Features	
		3 to 8	Modification of 1.2 Ordering Information	
		9 to 22	Modification of package type in 1.3 Pin Configuration (Top View)	
		34 to 43	Modification of description of subsystem clock in 1.6 Outline of Functions	
		34 to 43	Modification of description of timer output in 1.6 Outline of Functions	
		34 to 43	Modification of error of data transfer controller in 1.6 Outline of Functions	
		34 to 43	Modification of error of event link controller in 1.6 Outline of Functions	
		45, 46	Modification of description of Tables in 2.1 Absolute Maximum Ratings	
		47	Modification of Tables, notes, cautions, and remarks in 2.2 Oscillator Characteristics	
		48	Modification of error of conditions of high level input voltage in 2.3.1 Pin characteristics	
		49	Modification of error of conditions of low level output voltage in 2.3.1 Pin characteristics	
		53 to 62	Modification of Notes and Remarks in 2.3.2 Supply current characteristics	
		65, 66	Addition of Minimum Instruction Execution Time during Main System Clock Operation	
		67 to 69	Addition of AC Timing Test Points	
		70 to 97	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit	
		98 to 101	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA	
		102 to 105	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics	
		107	Addition of characteristic in 2.6.4 Comparator	
		107	Deletion of detection delay in 2.6.5 POR circuit characteristics	
		109	Modification of 2.6.7 Power supply voltage rising slope characteristics	
		110	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	
		110	Addition of characteristic in 2.8 Flash Memory Programming Characteristics	
		111	Addition of description in 2.10 Timing for Switching Flash Memory Programming Modes	

REVISION HISTORY	RL78/G14 Datasheet
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Boy Data		Description		
Nev.	Page	Page	Summary	
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145	Modification of specifications in 3.3.2 Supply current characteristics	
		p.197	Modification of part number in 4.7 52-pin products	
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics	

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NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.