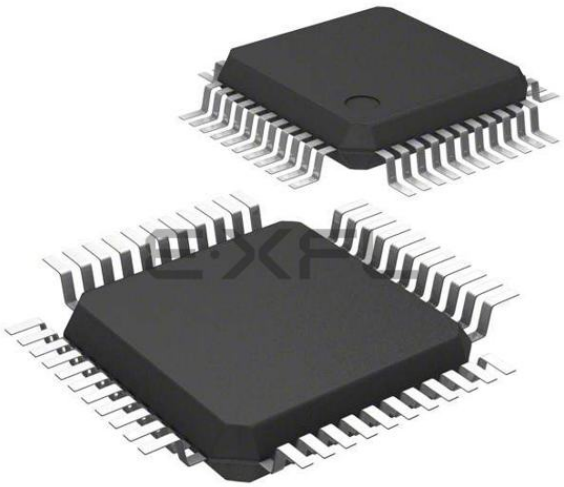
Renesas Electronics America Inc - R5F104FEDFP#50 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fedfp-50

(3/5)

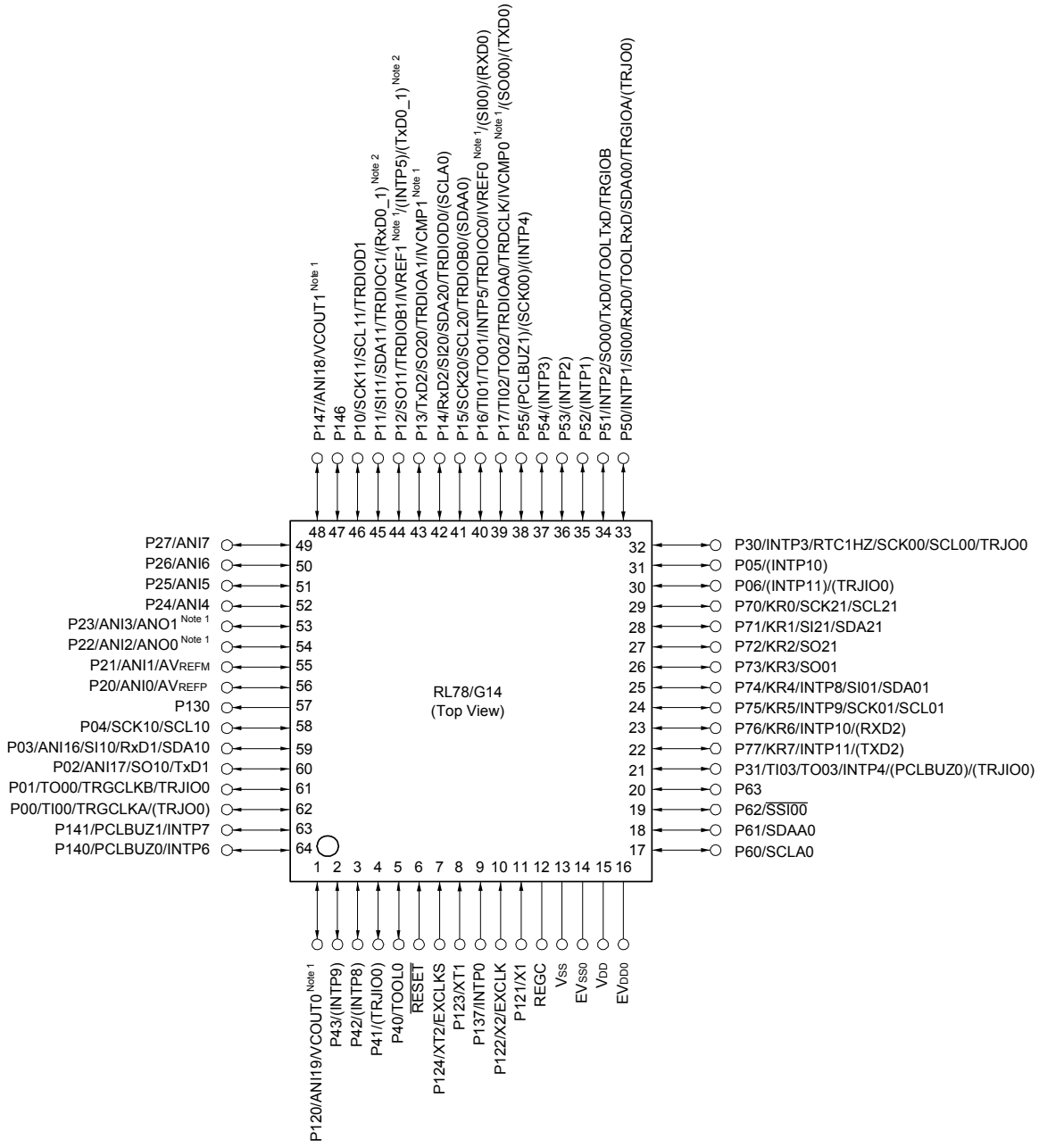
Pin count	Package	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0 R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 R5F104GKAFB#30, R5F104GLAFB#30 R5F104GKAFB#50, R5F104GLAFB#50
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GFDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0 R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GFDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0 R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0 R5F104GKGFB#30, R5F104GLGFB#30 R5F104GKGFB#50, R5F104GLGFB#50
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0 R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0 R5F104GKANA#U0, R5F104GLANA#U0 R5F104GKANA#W0, R5F104GLANA#W0
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0 R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0 R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0 R5F104GKGNA#U0, R5F104GLGNA#U0 R5F104GKGNA#W0, R5F104GLGNA#W0
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

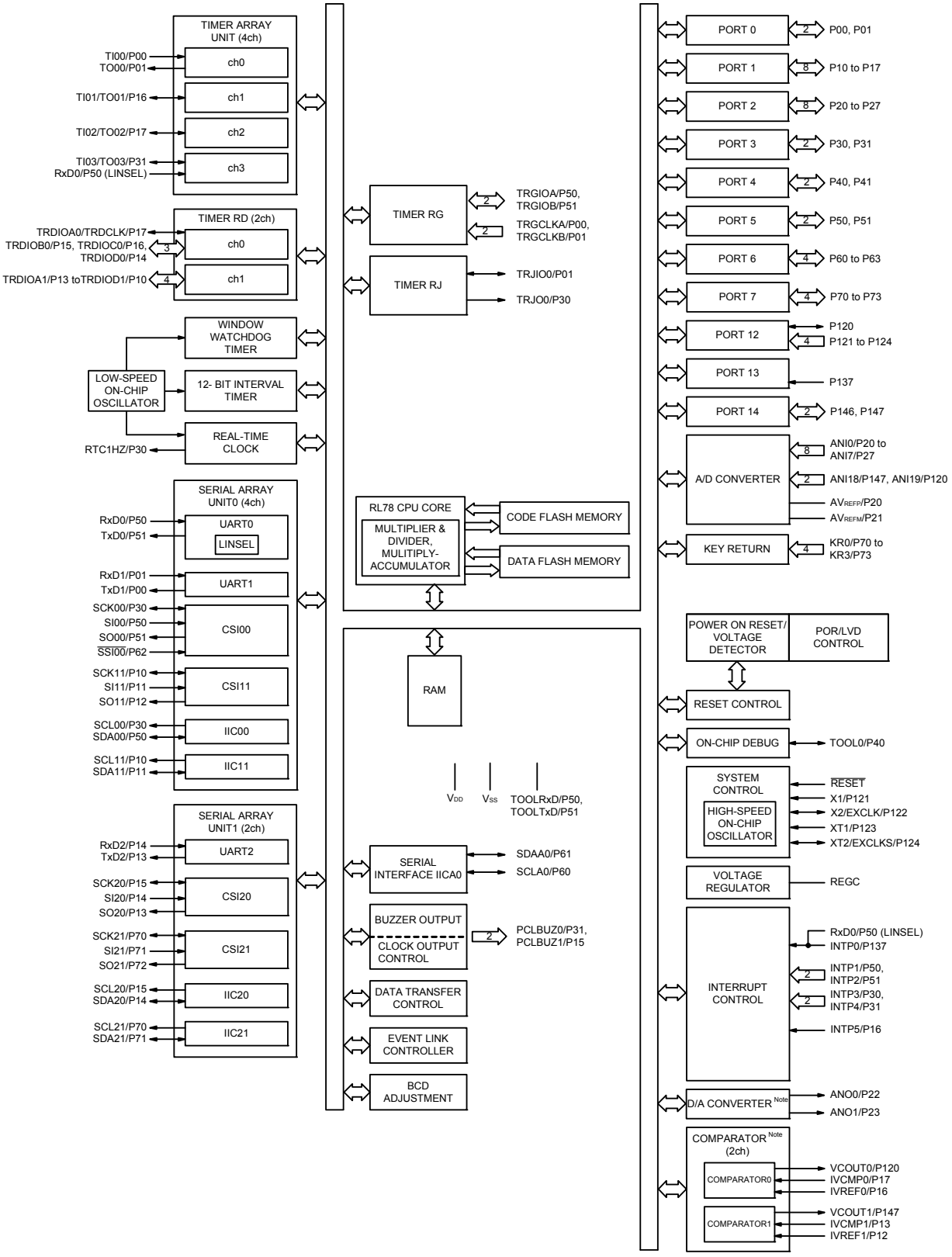
Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.5 44-pin products



Note Mounted on the 96 KB or more code flash memory products.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications T_A = -40 to +85°C
R5F104xxAxx
D: Industrial applications T_A = -40 to +85°C
R5F104xxDxx
G: Industrial applications when T_A = -40 to +105°C products is used in the range of T_A = -40 to +85°C
R5F104xxGxx

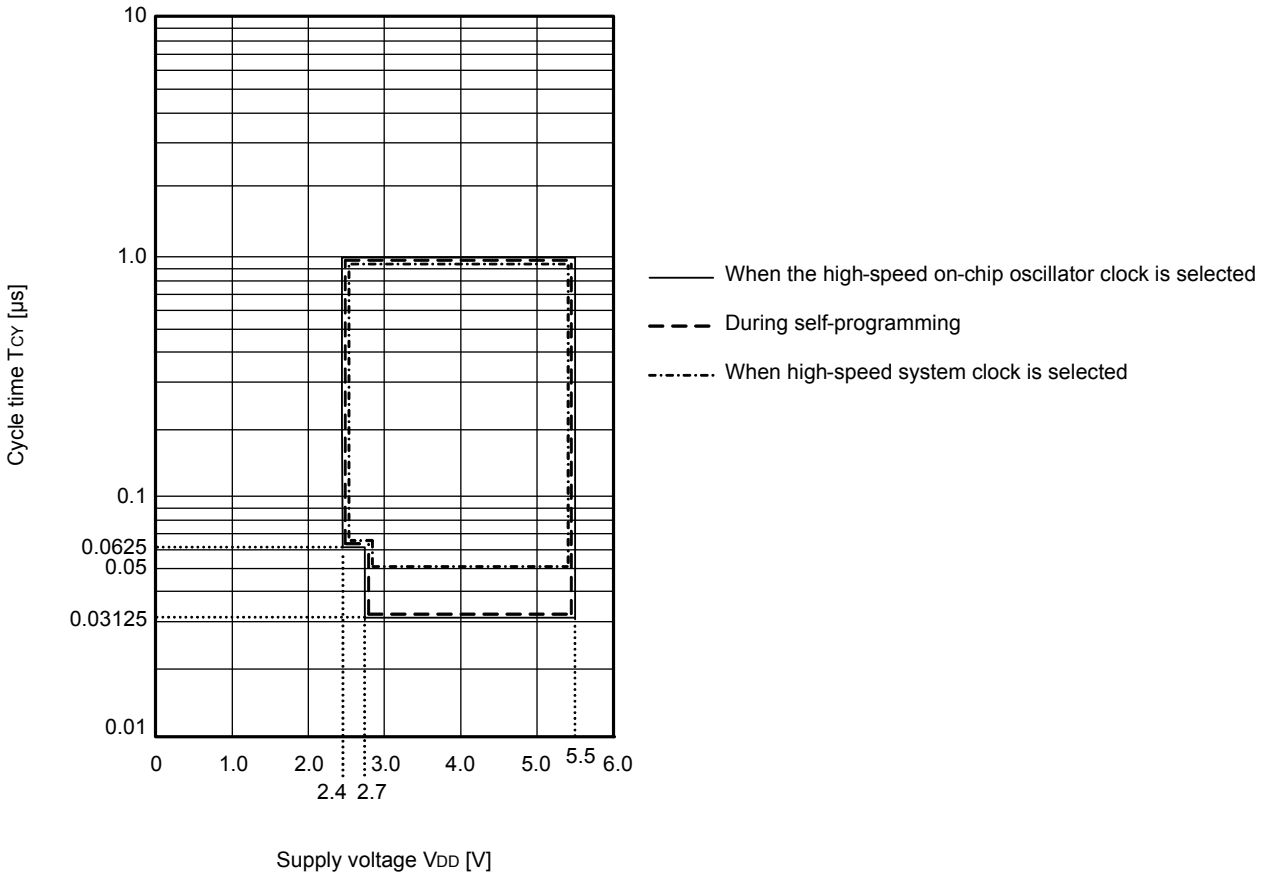
Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

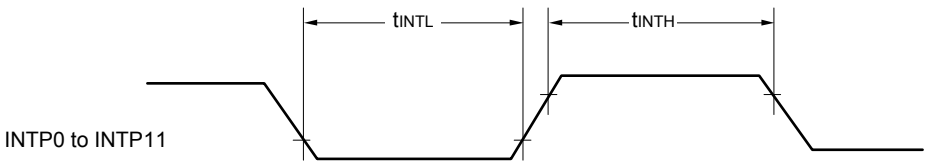
Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual**.**

Minimum Instruction Execution Time during Main System Clock Operation

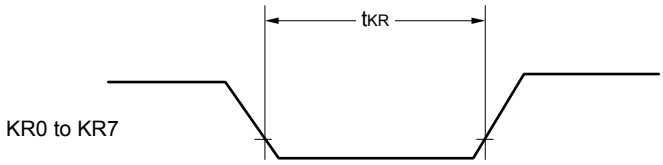
T_{CY} vs V_{DD} (HS (high-speed main) mode)



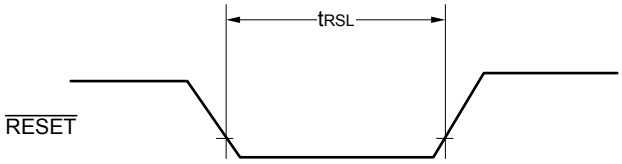
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 40		1/f_{MCK} + 40		1/f_{MCK} + 40		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		1/f_{MCK} + 40		1/f_{MCK} + 40		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 250		1/f_{MCK} + 250		1/f_{MCK} + 250		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		1/f_{MCK} + 250		1/f_{MCK} + 250		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 100		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 220		2/f_{MCK} + 220		2/f_{MCK} + 220	ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		2/f_{MCK} + 220		2/f_{MCK} + 220	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	1000	—		—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		—		—		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		—		—		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.5		—		—		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		—		—		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		50		—		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0	0.45	—		—		µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		—		—		µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.5		—		—		µs

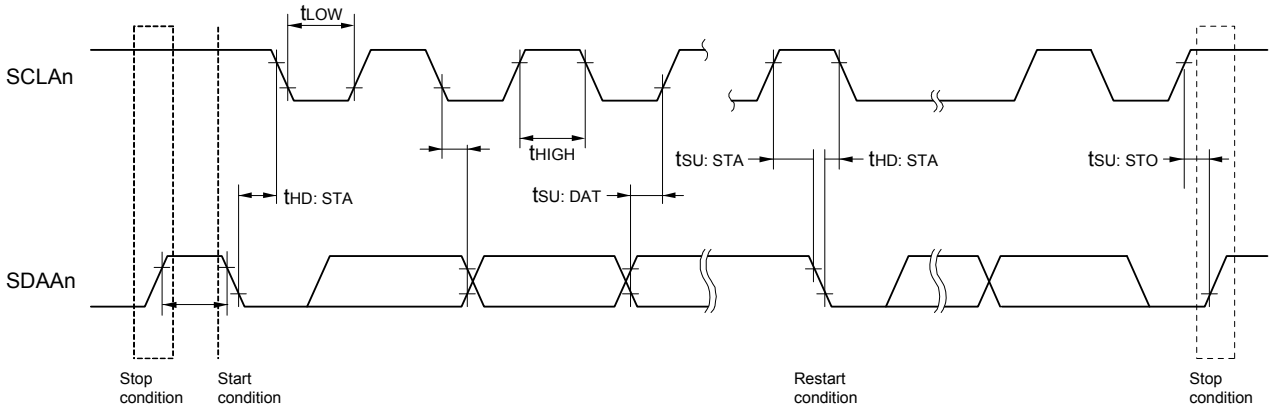
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Note 3. The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5		1.2	±8.5	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD0} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 5. When the conversion time is set to 57 µs (min.) and 95 µs (max.).

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} = EV_{DD1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.6		mA
						V_{DD} = 3.0 V		2.6		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.3		
						V_{DD} = 3.0 V		2.3		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.4	10.9	mA
						V_{DD} = 3.0 V		5.4	10.9	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.0	10.3	
						V_{DD} = 3.0 V		5.0	10.3	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.2	8.2	
						V_{DD} = 3.0 V		4.2	8.2	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	7.8	
						V_{DD} = 3.0 V		4.0	7.8	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.0	5.6	
						V_{DD} = 3.0 V		3.0	5.6	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	6.6	mA
						Resonator connection		3.6	6.7	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	6.6	
						Resonator connection		3.6	6.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.9	
						Resonator connection		2.2	4.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.9	
						Resonator connection		2.2	4.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.9	7.1	µA
						Resonator connection		4.9	7.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	7.1	
						Resonator connection		4.9	7.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.1	8.8	
						Resonator connection		5.1	8.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	10.5	
						Resonator connection		5.5	10.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.5	14.5	
						Resonator connection		6.5	14.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		13.0	58.0	
						Resonator connection		13.0	58.0	

(**Notes** and **Remarks** are listed on the next page.)

(4) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		µA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		µA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		µA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		µA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		µA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		µA
D/A converter operating current	I_{DAC} Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	I_{CMP} Notes 1, 12, 13	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		µA
			Comparator high-speed mode		6.5		µA
			Comparator low-speed mode		1.7		µA
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		µA
			Comparator high-speed mode		4.0		µA
			Comparator low-speed mode		1.3		µA
LVD operating current	I_{LVD} Notes 1, 7				0.08		µA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

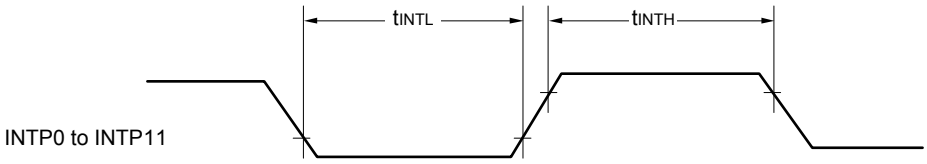
Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

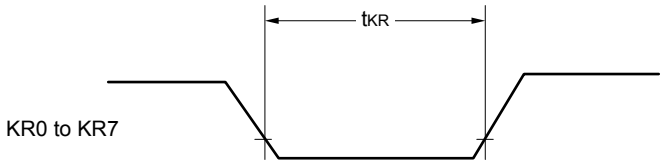
Note 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

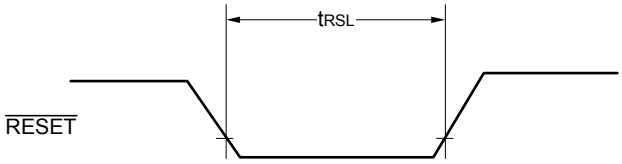
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 66	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

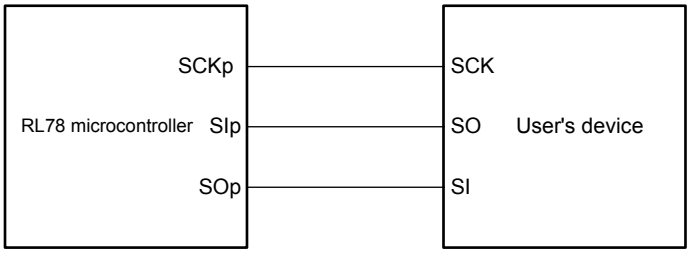
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	400		ns

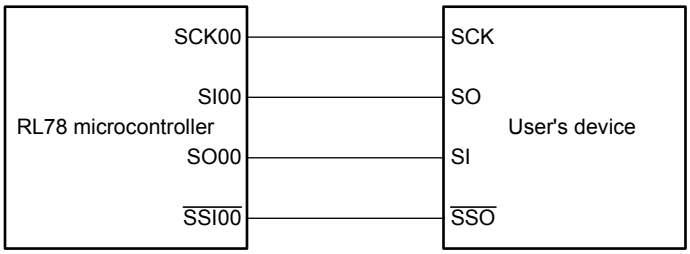
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)

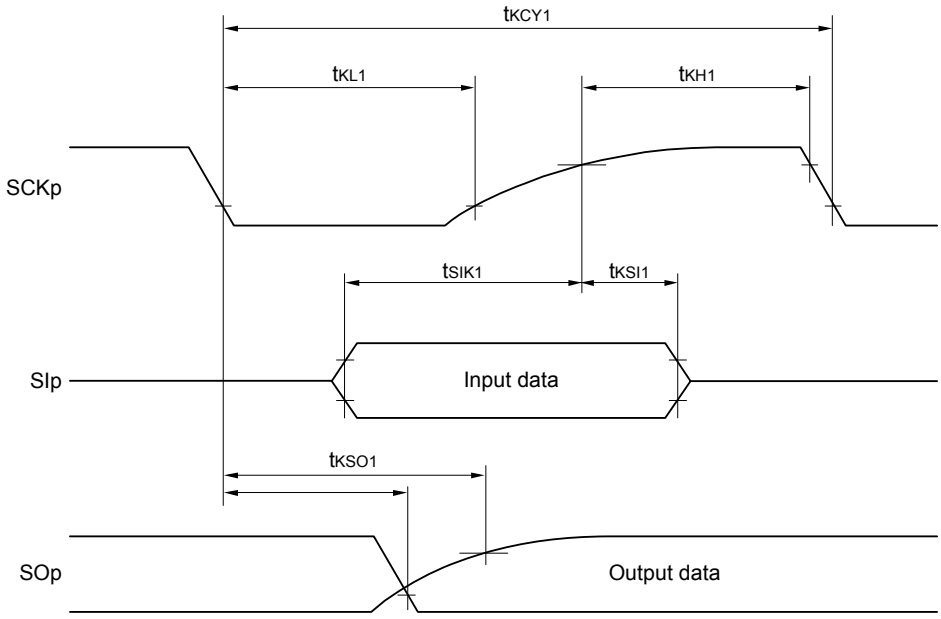


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

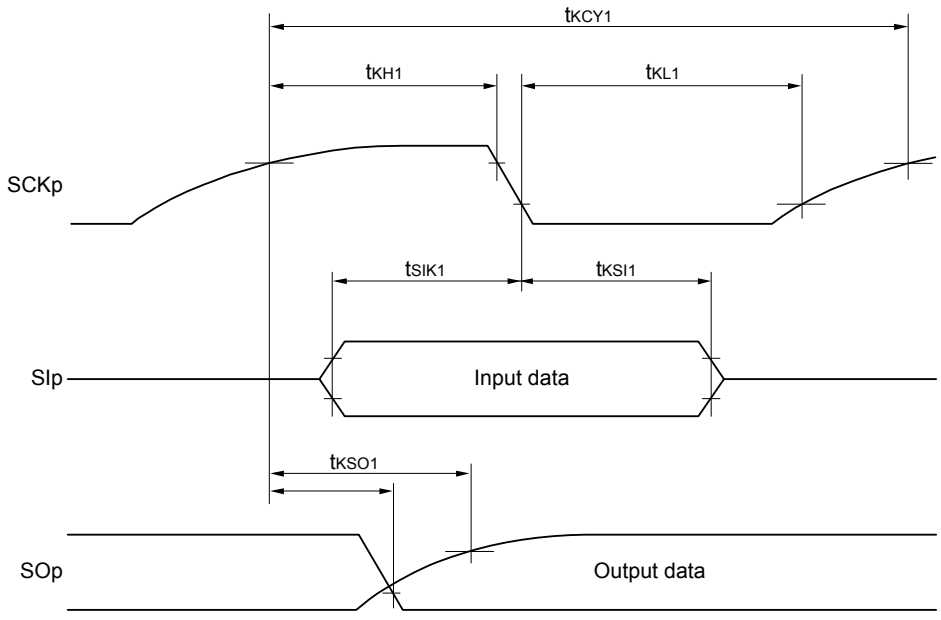


Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

3.6.4 Comparator

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref			0		EV_{DD0} - 1.4	V
	Ivcmp			-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V Input slew rate > 50 mV/µs	Comparator high-speed mode, standard mode			1.2	µs
			Comparator high-speed mode, window mode			2.0	µs
			Comparator low-speed mode, standard mode		3.0	5.0	µs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode			0.76 V_{DD}		V
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode			0.24 V_{DD}		V
Operation stabilization wait time	t_{CMP}			100			µs
Internal reference voltage Note	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.50	V

Note Not usable in sub-clock operation or STOP mode.

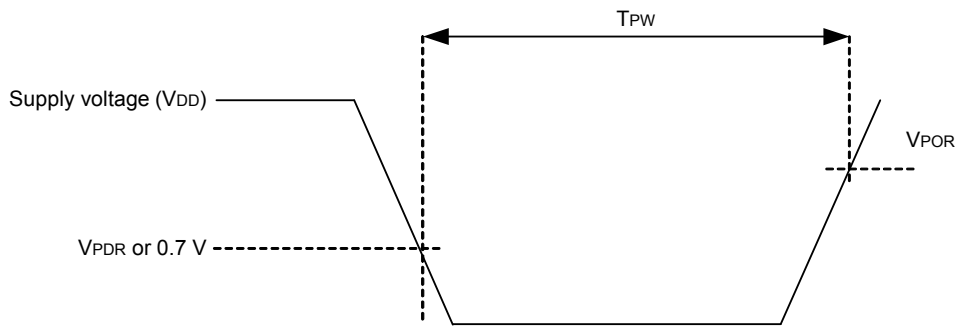
3.6.5 POR circuit characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on V_{DD} rising	1.45	1.51	1.57	V
	V_{PDR}	Voltage threshold on V_{DD} falling Note 1	1.44	1.50	1.56	V
Minimum pulse width Note 2	T_{PW}		300			µs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

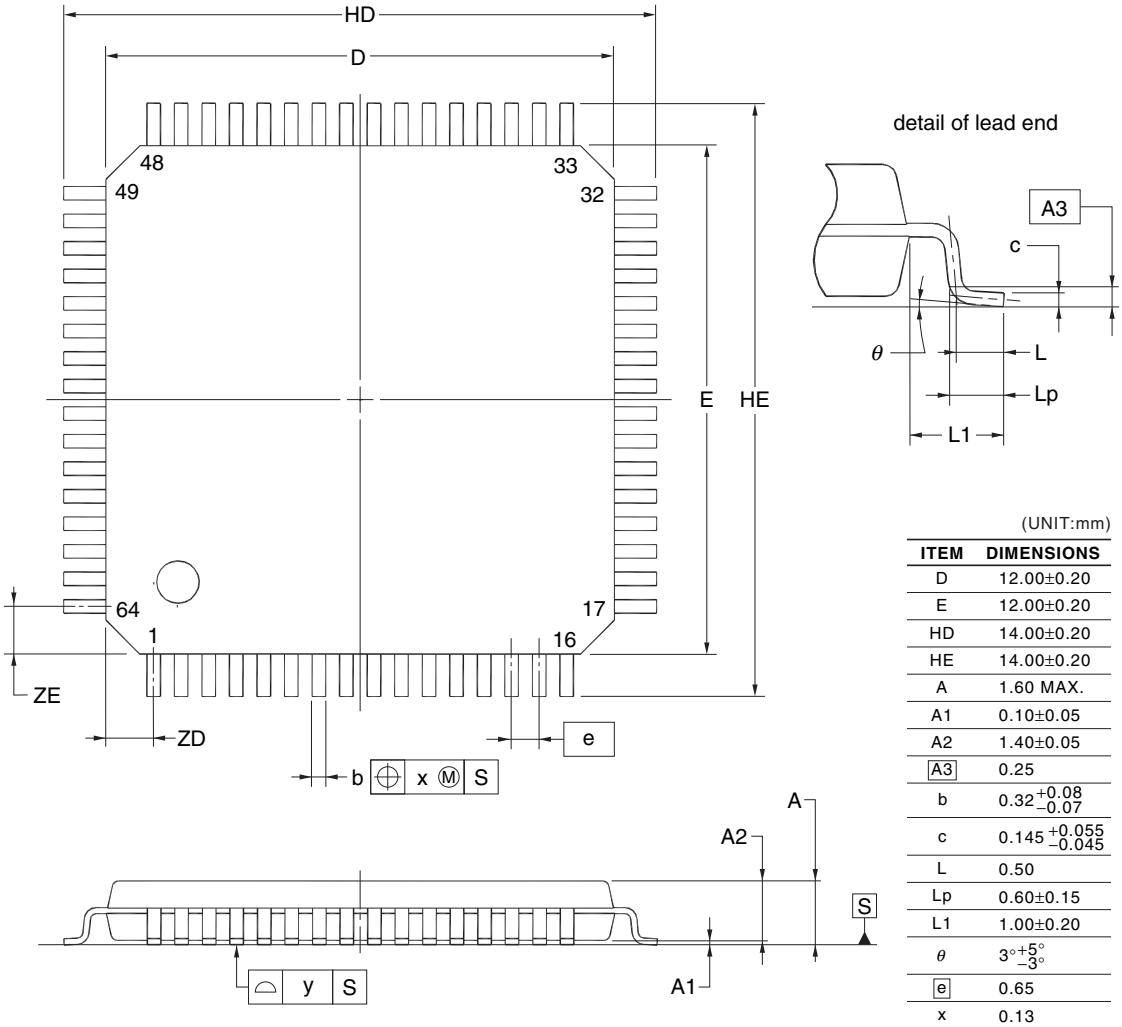
Note 2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFA, R5F104LHAFA, R5F104LJAFA
R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFA, R5F104LHDFA, R5F104LJDFA
R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
R5F104LKAFA, R5F104LLAFA
R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.