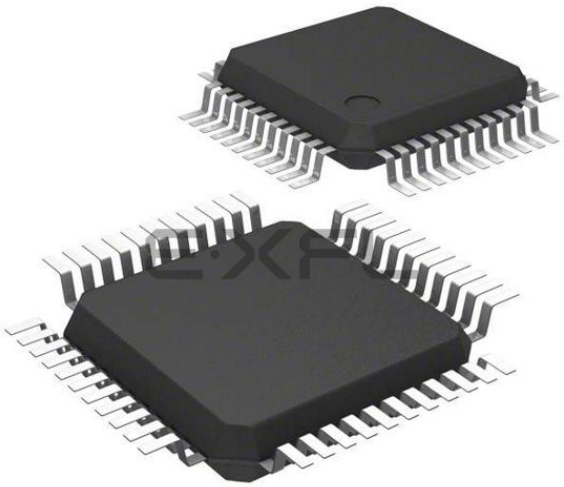
Renesas Electronics America Inc - R5F104FHAFP#X0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fhafp-x0

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Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAFA#V0, R5F104LHAFA#V0, R5F104LJAFA#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAFA#X0, R5F104LHAFA#X0, R5F104LJAFA#X0 R5F104LKAFA#30, R5F104LLAFA#30 R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFA#V0, R5F104LHDFA#V0, R5F104LJDFA#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFA#X0, R5F104LHDFA#X0, R5F104LJDFA#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LFDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LFDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0 R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0 R5F104LKALA#U0, R5F104LLALA#U0 R5F104LKALA#W0, R5F104LLALA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LFDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LFDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

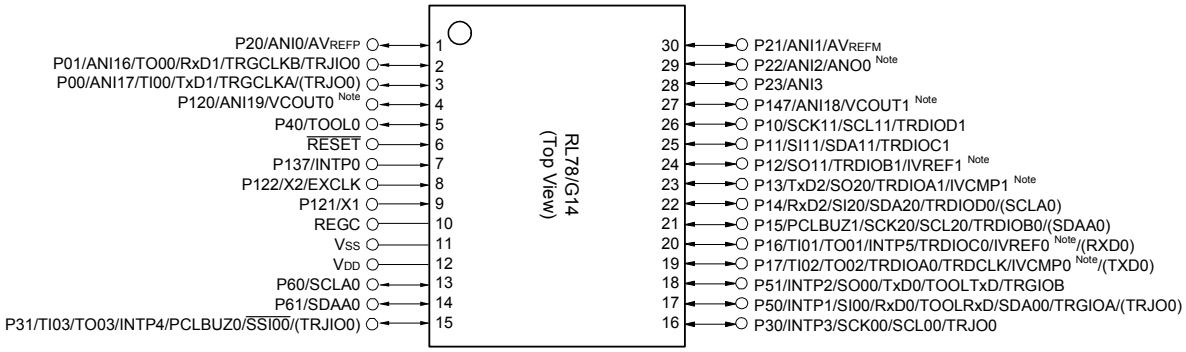
Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

• 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

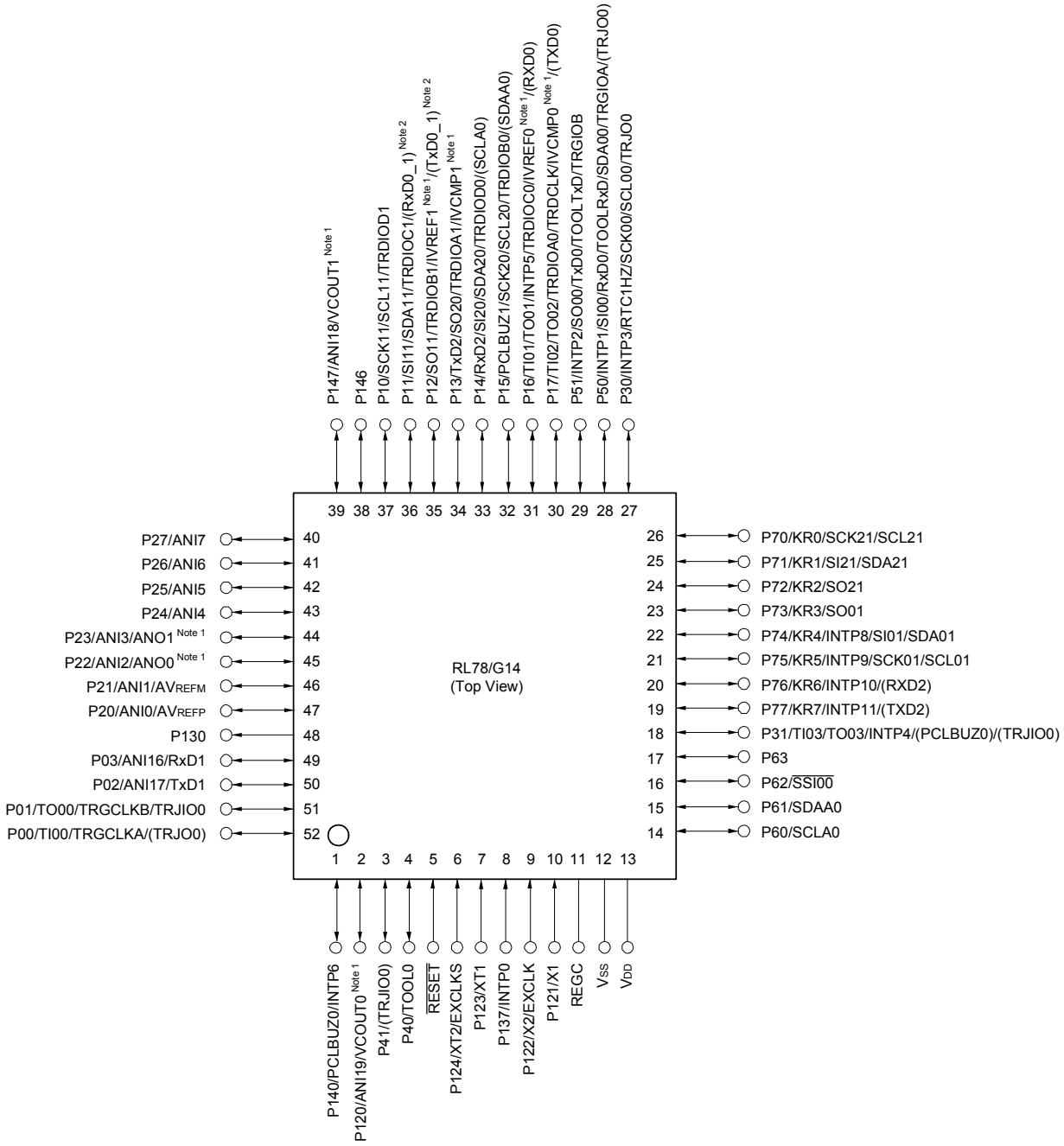
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.7 52-pin products

• 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



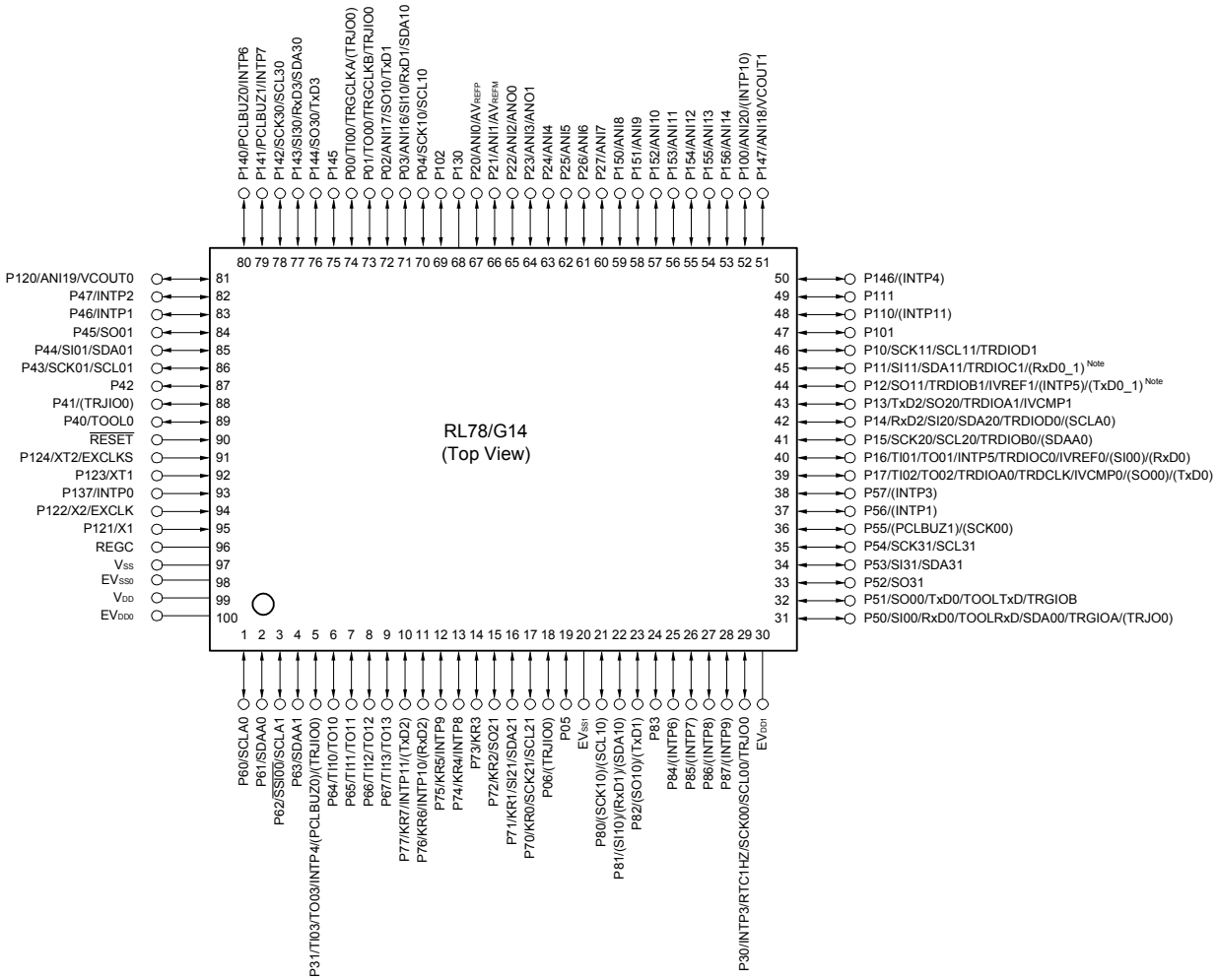
Note 1. Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

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Item		30-pin R5F104Ax (x = F, G)	32-pin R5F104Bx (x = F, G)	36-pin R5F104Cx (x = F, G)	40-pin R5F104Ex (x = F to H)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
D/A converter		1 channel	2 channels		
Comparator		2 channels			
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels			
	I^2C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources			31 sources
Event link controller (ELC)		Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = –40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = –40 to +105°C)			
Operating ambient temperature		T_A = –40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

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Item		44-pin R5F104Fx (x = F to H, J)	48-pin R5F104Gx (x = F to H, J)	52-pin R5F104Jx (x = F to H, J)	64-pin R5F104Lx (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256	96 to 256	96 to 256
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 24 Note	12 to 24 Note	12 to 24 Note	12 to 24 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)			

(**Note** is listed on the next page.)

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

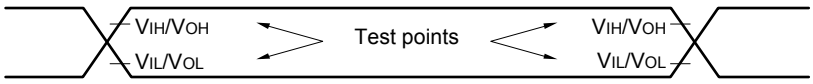
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.9		mA
						V_{DD} = 3.0 V		2.9		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.5		
						V_{DD} = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		6.0	11.2	mA
						V_{DD} = 3.0 V		6.0	11.2	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.5	10.6	
						V_{DD} = 3.0 V		5.5	10.6	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.7	8.6	
						V_{DD} = 3.0 V		4.7	8.6	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.4	8.2	
						V_{DD} = 3.0 V		4.4	8.2	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.3	5.9	
						V_{DD} = 3.0 V		3.3	5.9	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.5	mA
						V_{DD} = 2.0 V		1.5	2.5	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.1	mA
						V_{DD} = 2.0 V		1.5	2.1	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8	
						Resonator connection		3.9	7.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.2		µA
						Resonator connection		5.2		
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(**Notes** and **Remarks** are listed on the next page.)

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EV_{DD0} ≤ 5.5 V		f_{MCK}/6 Note 2		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		5.3		1.3		0.6	Mbps
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		f_{MCK}/6 Note 2		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		5.3		1.3		0.6	Mbps
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		f_{MCK}/6 Note 2		f_{MCK}/6 Note 2		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		5.3		1.3		0.6	Mbps
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—			f_{MCK}/6 Note 2		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	—			1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ EV_{DD0} < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ EV_{DD0} < 1.8 V: MAX. 0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns

Note Use it with $EV_{DD0} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

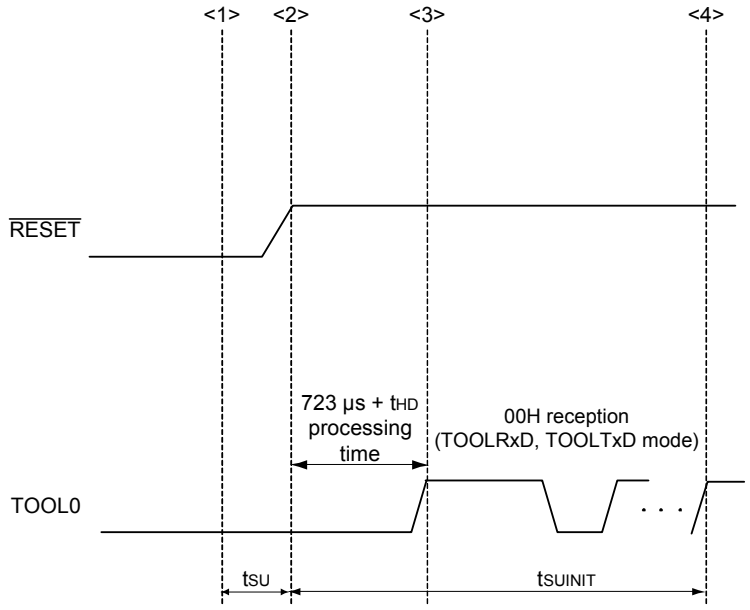
Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		4.7		4.7		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		4.0		4.0		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		4.7		4.7		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		4.0		4.0		µs

(**Notes**, **Caution**, and **Remark** are listed on the next page.)

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note 2		ns
		2.4V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

Note 5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		µs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

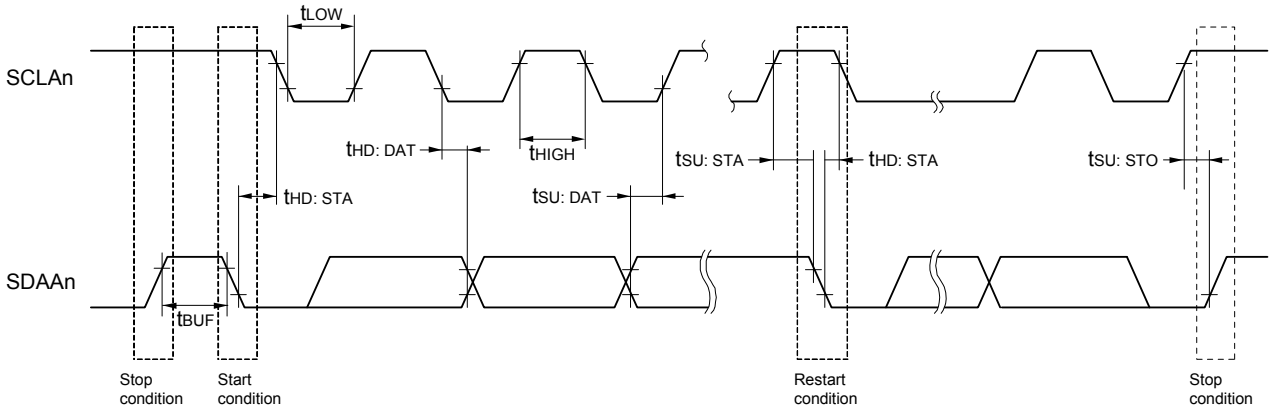
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD0} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

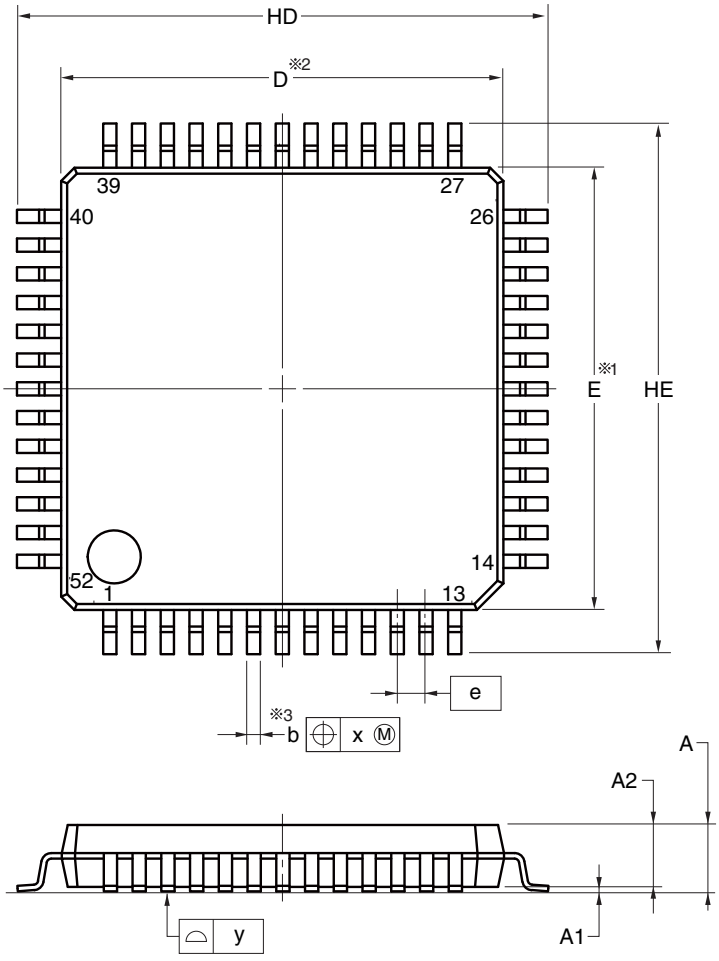
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

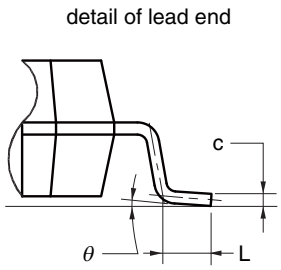
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

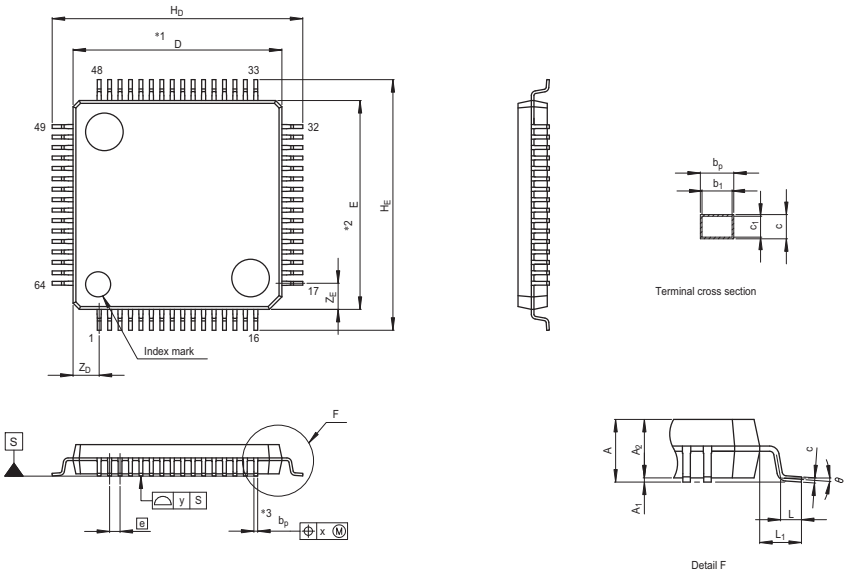
NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

R5F104LKAFB, R5F104LLAFB
R5F104LKGFB, R5F104LLGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Oct 25, 2013	112 to 169	Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS
		171 to 187	Modification of 4.1 30-pin products to 4.10 100-pin products
3.00	Feb 07, 2014	All	Addition of products with maximum 512 KB flash ROM and 48 KB RAM
		1	Modification of 1.1 Features
		2	Modification of ROM, RAM capacities and addition of note 3
		3	Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14
		6 to 8	Addition of part number
		15, 16	Modification of 1.3.6 48-pin products
		17	Modification of 1.3.7 52-pin products
		18, 19	Modification of 1.3.8 64-pin products
		20	Modification of 1.3.9 80-pin products
		21, 22	Modification of 1.3.10 100-pin products
		35, 37, 39, 41, 43, 45, 47	Modification of operating ambient temperature in 1.6 Outline of Functions
		42, 43	Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB)
		46, 47	Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB)
		65 to 68	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products
		118	Modification of 2.7 Data Memory Retention Characteristics
		137 to 140	Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products
		180	Modification of 3.7 Data Memory Retention Characteristics
		189, 190	Addition and modification of 4.6 48-pin products
		191	Modification of 4.7 52-pin products
		193 to 195	Addition and modification of 4.8 64-pin products
		198, 199	Addition and modification of 4.9 80-pin products
		201, 202	Addition and modification of 4.10 100-pin products
3.20	Jan 05, 2015	p.2	Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note
		p.6	Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information
		p.6 to 8	Deletion of note 2 in 1.2 Ordering Information
		p.17	Deletion of note 2 in 1.3.7 52-pin products
		p.36, 39, 42, 45, 48, 50, 52	Modification of description in 1.6 Outline of Functions
		p.46, 48	Deletion of description of 52-pin in 1.6 Outline of Functions
		p.47	Modification of note of 1.6 Outline of Functions
		p.62, 64, 66, 68, 70, 72	Modification of specifications in 2.3.2 Supply current characteristics