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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24К х 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fjafp-50

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.2 Ordering Information



Part No. R5F104LEAxxxFB#V0 Packaging specification #30: Tray (LFQFP, LQFP) #U0: Tray (HWQFN, WFLGA, FLGA) #V0: Tray (LFQFP, LQFP, LSSOP) #50: Embossed Tape (LFQFP, LQFP) #W0:Embossed Tape (HWQFN, WFLGA, FLGA) #X0: Embossed Tape (LFQFP, LQFP, LSSOP) Package type: SP: LSSOP, 0.65 mm pitch FP: LQFP, 0.80 mm pitch FA: LQFP, 0.65 mm pitch FB: LFQFP, 0.50 mm pitch NA: HWQFN, 0.50 mm pitch LA: WFLGA, 0.50 mm pitch FLGA, 0.50 mm pitch ROM number (Omitted with blank products) Fields of application: A: Consumer applications, TA = -40 to +85 °C D: Industrial applications, TA = -40 to +85 $^{\circ}$ C G: Industrial applications, TA = -40 to +105 °C ROM capacity: A: 16 KB C: 32 KB D: 48 KB E: 64 KB F: 96 KB G: 128 KB H: 192 KB J: 256 KB K: 384 KB L: 512 KB Pin count: A: 30-pin B: 32-pin C: 36-pin E: 40-pin F: 44-pin G: 48-pin J: 52-pin L: 64-pin M: 80-pin P: 100-pin RL78/G14 Memory type: F: Flash memory Renesas MCU Renesas semiconductor product



• 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

- Caution 1. Make EVsso, EVss1 pins the same potential as Vss pin.
- Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).
- Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).
- Remark 1. For pin identification, see 1.4 Pin Identification.
- Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.
- **Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).



1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		SCK00, SCK01, SCK10,:	Serial clock input/output
ANO0, ANO1:	Analog output	SCK11, SCK20, SCK21,	
AVREFM:	A/D converter reference	SCK30, SCK31	
	potential (– side) input	SCLA0, SCLA1,:	Serial clock input/output
AVREFP:	A/D converter reference	SCL00, SCL01, SCL10, SCL11,:	Serial clock output
	potential (+ side) input	SCL20, SCL21, SCL30,	
EVDD0, EVDD1:	Power supply for port	SCL31	
EVsso, EVss1:	Ground for port	SDAA0, SDAA1, SDA00,:	Serial data input/output
EXCLK:	External clock input	SDA01, SDA10, SDA11,	
	(main system clock)	SDA20, SDA21, SDA30,	
EXCLKS:	External clock input	SDA31	
	(subsystem clock)	SI00, SI01, SI10, SI11,:	Serial data input
INTP0 to INTP11:	External interrupt input	SI20, SI21, SI30, SI31	
IVCMP0, IVCMP1:	Comparator input	SO00, SO01, SO10,:	Serial data output
IVREF0, IVREF1:	Comparator reference input	SO11, SO20, SO21,	
KR0 to KR7:	Key return	SO30, SO31	
P00 to P06:	Port 0	SSI00:	Serial interface chip select input
P10 to P17:	Port 1	TI00 to TI03,:	Timer input
P20 to P27:	Port 2	TI10 to TI13	
P30, P31:	Port 3	TO00 to TO03,:	Timer output
P40 to P47:	Port 4	TO10 to TO13, TRJO0	
P50 to P57:	Port 5	TOOL0:	Data input/output for tool
P60 to P67:	Port 6	TOOLRxD, TOOLTxD:	Data input/output for external device
P70 to P77:	Port 7	TRDCLK, TRGCLKA,:	Timer external input clock
P80 to P87:	Port 8	TRGCLKB	
P100 to P102:	Port 10	TRDIOA0, TRDIOB0,:	Timer input/output
P110, P111:	Port 11	TRDIOC0, TRDIOD0,	
P120 to P124:	Port 12	TRDIOA1, TRDIOB1,	
P130, P137:	Port 13	TRDIOC1, TRDIOD1,	
P140 to P147:	Port 14	TRGIOA, TRGIOB, TRJIO0	
P150 to P156:	Port 15	TxD0 to TxD3:	Transmit data
PCLBUZ0, PCLBUZ1:	Programmable clock	VCOUT0, VCOUT1:	Comparator output
	output/buzzer output	Vdd:	Power supply
REGC:	Regulator capacitance	Vss:	Ground
RESET:	Reset	X1, X2:	Crystal oscillator (main system clock)
RTC1HZ:	Real-time clock correction	XT1, XT2:	Crystal oscillator (subsystem clock)
	clock		
	(1 Hz) output		



(2)	2)
(2/	<u>~</u>)

		44-pin	48-pin 52-pin 64-pin					
l	tem	R5F104Fx	R5F104Gx	R5F104Jx	R5F104Lx			
		(x = F to H, J)	(x = F to H, J)	(x = F to H, J)	(x = F to H, J)			
Clock output/buzz	zer output	2	2	2	2			
		• 2.44 kHz, 4.88 kHz,	9.76 kHz, 1.25 MHz, 2.	5 MHz, 5 MHz, 10 MHz				
		(Main system clock:	fMAIN = 20 MHz operation	on)				
		• 256 Hz, 512 Hz, 1.0	24 KHZ, 2.048 KHZ, 4.09	96 kHz, 8.192 kHz, 16.3 tion)	384 kHz, 32.768 kHz			
9/10 bit recolution					12 obonnolo			
8/10-bit resolution	TA/D converter		To channels	12 channels	12 channels			
D/A converter		2 channels						
Comparator		2 channels						
Serial interface		[44-pin products]			:6 - d 120 - 4 - d - a - a - a - a			
		CSI: 1 channel/UAR		N-DUS): 1 channel/simpi	Iffed I2C: 1 channel			
		CSI: 2 channels/LIAI	RT: 1 channel/simplified	I ² C: 2 channels				
		[48-pin, 52-pin produc	ts]					
		CSI: 2 channels/UAI	RT (UART supporting L	IN-bus): 1 channel/simp	olified I ² C: 2 channels			
		CSI: 1 channel/UAR	T: 1 channel/simplified I	² C: 1 channel				
		CSI: 2 channels/UAF	RT: 1 channel/simplified	I ² C: 2 channels				
		[64-pin products]						
		• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 2 channels						
		CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels						
		• CSI: 2 channels/UAI	RI: 1 channel/simplified		1			
	I ² C bus		1 channel	1 channel	1 channel			
Data transfer con	troller (DTC)	31 sources 32 sources 33 sources						
Event link control	ler (ELC)	Event input: 22						
	1	Event trigger output: 9						
Vectored inter-	Internal	24	24	24	24			
Tupi sources	External	7	10	12	13			
Key interrupt		4	6	8	8			
Reset		Reset by RESET pin						
		 Internal reset by wat 	chdog timer					
		Internal reset by pov	ver-on-reset					
		Internal reset by volu	age delector	Note				
		Internal reset by RA	Internal reset by Illegal Instruction execution Note Internal reset by RAM parity error					
		Internal reset by illeg	gal-memory access					
Power-on-reset c	ircuit	Power-on-reset:	1.51 ±0.04 V (TA = -40	to +85°C)				
			1.51 ±0.06 V (TA = -40	to +105°C)				
		• Power-down-reset: 1.50 ±0.04 V (Ta = -40 to +85°C)						
		1.50 ±0.06 V (TA = -40 to +105°C)						
Voltage detector		1.63 V to 4.06 V (14 s	tages)					
On-chip debug fu	nction	Provided						
Power supply vol	tage	VDD = 1.6 to 5.5 V (TA	$= -40 \text{ to } +85^{\circ}\text{C}$					
Operating and in	at tomporet	VUU = 2.4 to 5.5 V (1A)	$\frac{1}{2} - \frac{1}{2} + \frac{1}$	Du Industrial application				
Operating ambier	it temperature	$IA = -40$ to $+85^{\circ}C$ (A: $T_{A} = -40$ to $+105^{\circ}C$ (C	Consumer applications	, ט: industrial applicatio	ns),			
		IA+0 10 + 105 C (G		/				

Note

The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

1	0	in	1
(2	12	

		48-pin	64-pin			
Item		R5F104Gx	R5F104Lx			
		(x = K, L)	(x = K, L)			
Clock output/buzzer outp	ut	2	2			
		 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 (Main system clock: fMAIN = 20 MHz operation 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.09 (Subsystem clock: fsuB = 32.768 kHz operation) 	5 MHz, 5 MHz, 10 MHz on) 6 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz tion)			
8/10-bit resolution A/D co	nverter	10 channels	12 channels			
D/A converter		2 channels				
Comparator		2 channels				
Serial interface		 [48-pin products] CSI: 2 channels/UART (UART supporting LI CSI: 1 channel/UART: 1 channel/simplified I CSI: 2 channels/UART: 1 channel/simplified [64-pin products] CSI: 2 channels/UART (UART supporting LI CSI: 2 channels/UART: 1 channel/simplified CSI: 2 channels/UART: 1 channel/simplified CSI: 2 channels/UART: 1 channel/simplified 	 [48-pin products] CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [64-pin products] CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
	I ² C bus	1 channel	1 channel			
Data transfer controller (I	DTC)	32 sources	33 sources			
Event link controller (ELC	;)	Event input: 22 Event trigger output: 9				
Vectored interrupt	Internal	24	24			
sources	External	10	13			
Key interrupt		6	8			
Reset		 Reset by RESET pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access 				
Power-on-reset circuit		• Power-on-reset: $1.51 \pm 0.04 \text{ V} (\text{TA} = -40 \text{ to } +85^{\circ}\text{C})$ $1.51 \pm 0.06 \text{ V} (\text{TA} = -40 \text{ to } +105^{\circ}\text{C})$ • Power-down-reset: $1.50 \pm 0.04 \text{ V} (\text{TA} = -40 \text{ to } +85^{\circ}\text{C})$ $1.50 \pm 0.06 \text{ V} (\text{TA} = -40 \text{ to } +105^{\circ}\text{C})$				
Voltage detector		1.63 V to 4.06 V (14 stages)				
On-chip debug function		Provided				
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)				
Operating ambient tempe	erature	TA = -40 to +85°C (A: Consumer applications, TA = -40 to +105°C (G: Industrial applications)	D: Industrial applications),			

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

RENESAS

2. ELECTRICAL SPECIFICATIONS (TA = -40 to $+85^{\circ}$ C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^{\circ}C$

R5F104xxAxx

- D: Industrial applications TA = -40 to +85°C R5F104xxDxx
- G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C R5F104xxGxx
- Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.
- Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.



- Note 1. Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 Note 2. During HALT instruction execution by flash memory.
- **Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 4.** When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 32 MHz
 - 2.4 V \leq VDD \leq 5.5 V@1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 4 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remark 3.** file: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsuB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



Parameter	Symbol		Conditions	HS (high-s main) mo	peed ode	LS (low-speed mode	d main)	LV (low-vo main) mo	ltage ode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tксү1 ≥ 4/fcLк	$2.7~V \leq E_{VDD0} \leq 5.5~V$	125		500		1000		ns
			$2.4~\text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5~\text{V}$	250		500		1000		ns
			$1.8~V \leq EV_{DD0} \leq 5.5~V$	500		500		1000		ns
			$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	1000		1000		1000		ns
			$1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	—		1000		1000		ns
SCKp high-/low-level	tĸнı,	$4.0 \text{ V} \leq \text{EV}_{\text{DDO}}$	0 ≤ 5.5 V	tксү1/2 - 12		tксү1/2 - 50		tксү1/2 - 50		ns
width	tKL1	$2.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	tксү1/2 - 18		tксү1/2 - 50		tксү1/2 - 50		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DDO}}$	$0 \leq 5.5 \text{ V}$	tксү1/2 - 38		tксү1/2 - 50		tксү1/2 - 50		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	tксү1/2 - 50		tксү1/2 - 50		tксү1/2 - 50		ns
		$1.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	tксү1/2 - 100		tксү1/2 - 100		tксү1/2 - 100		ns
		$1.6 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	—		tксү1/2 - 100		tксү1/2 - 100		ns
SIp setup time	tsik1	$4.0 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	44		110		110		ns
(to SCKp↑) ^{Note 1}		$2.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	44		110		110		ns
		$2.4 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	75		110		110		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	110		110		110		ns
		$1.7 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	220		220		220		ns
		$1.6 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	—		220		220		ns
SIp hold time	tksi1	$1.7 \text{ V} \leq \text{EV}_{\text{DDC}}$	$\leq 5.5 V$	19		19		19		ns
(from SCKp↑) Note 2		$1.6 \text{ V} \leq \text{EV}_{\text{DDO}}$	$\leq 5.5 V$	—		19		19		ns
Delay time from SCKp↓ to SOp output	tkso1	$1.7 V \le EV_{DDC}$ C = 30 pF Note	o ≤ 5.5 V e 4		25		25		25	ns
		$1.6 V \le EV_{DDC}$ C = 30 pF Note	o ≤ 5.5 V e 4		_		25		25	ns

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) (TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))



RL78/G14

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

Parameter	Symbol	Cor	nditions	HS (hig main)	h-speed mode	LS (low main)	LS (low-speed main) mode		-voltage mode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tксү2	$4.0~V \leq EV_{DD0} \leq 5.5~V,$	24 MHz < fмск	14/fмск		—		_		ns
Note 1		$2.7~V \leq V_b \leq 4.0~V$	$20 \text{ MHz} < f_{MCK} \leq 24 \text{ MHz}$	12/fмск		—				ns
			$8 \text{ MHz} < \text{fmck} \le 20 \text{ MHz}$	10/fмск		_				ns
			$4 \text{ MHz} < f_{MCK} \le 8 \text{ MHz}$	8/fмск		16/fмск		_		ns
			fмск ≤ 4 MHz	6/fмск		10/fмск		10/fмск		ns
		$2.7~V \leq EV_{DD0} < 4.0~V,$	24 MHz < fмск	20/fмск		—		_		ns
		$2.3 \text{ V} \leq \text{V}_b \leq 2.7 \text{ V}$	20 MHz < fмск ≤ 24 MHz	16/fмск		—		_		ns
			16 MHz < fмск ≤ 20 MHz	14/fмск		—		_		ns
			$8 \text{ MHz} < \text{fmck} \le 16 \text{ MHz}$	12/fмск		_		_		ns
			$4 \text{ MHz} < \text{fmck} \le 8 \text{ MHz}$	8/fмск		16/fмск		_		ns
			fмск ≤ 4 MHz	6/fмск		10/fмск		10/fмск		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} < 3.3 \text{ V},$	24 MHz < fмск	48/fмск		_		_		ns
		1.6 V ≤ Vb ≤ 2.0 V Note 2	20 MHz < fмск ≤ 24 MHz	36/fмск		_		_		ns
			16 MHz < fmck \leq 20 MHz	32/fмск		—		_		ns
			$8 \text{ MHz} < \text{fmck} \le 16 \text{ MHz}$	26/fмск		_		_		ns
		$4 \text{ MHz} < \text{fmck} \le 8 \text{ MHz}$	16/fмск		16/fмск		_		ns	
			fмск ≤ 4 MHz	10/fмск		10/fмск		10/fмск		ns
SCKp high-/ low-level width	tкн2, tкL2	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}, 2$	$2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$	tксү2/2 - 12		tксү2/2 - 50		tксү2/2 - 50		ns
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}, 2$	$2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}$	tксү2/2 - 18		tксү2/2 - 50		tксү2/2 - 50		ns
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 3.3 \text{ V}, ^{2}$	$1.6 \text{ V} \leq V_b \leq 2.0 \text{ V} \text{ Note } 2$	tксү2/2 - 50		tксү2/2 - 50		tксү2/2 - 50		ns
SIp setup time (to SCKp↑) ^{Note 3}	tsık2	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}, 2$	$2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}, 2$	$2.3 \text{ V} \leq \text{V}_b \leq 2.7 \text{ V}$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 3.3 \text{ V}, ^{2}$	$1.6 \text{ V} \leq V_b \leq 2.0 \text{ V} \text{ Note 2}$	1/fмск + 30		1/fмск + 30		1/fмск + 30		ns
SIp hold time (from SCKp↑) Note 4	tksi2			1/fмск + 31		1/fмск + 31		1/fмск + 31		ns
Delay time from SCKp↓ to SOp	tkso2	4.0 V \leq EVDD0 \leq 5.5 V, 2 Cb = 30 pF, Rb = 1.4 kΩ	$2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V},$		2/fмск + 120		2/fмск + 573		2/fмск + 573	ns
output ^{Note 5}		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, 2 \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	$2.3 \text{ V} \le \text{V}_{\text{b}} \le 2.7 \text{ V},$		2/fмск + 214		2/fмск + 573		2/fмск + 573	ns
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ C_b = 30 \ pF, \ R_V = 5.5 \ k\Omega \end{array}$	$1.6 \text{ V} \le \text{V}_b \le 2.0 \text{ V} \text{ Note 2},$		2/fмск + 573		2/fмск + 573		2/fмск + 573	ns

($(T_A = -40 \text{ to } +85^{\circ}\text{C})$	18V<	< Vnn < 5 5 V	Vss = EVsso	= FVSS1 = 0	٧١
	1A = -40 10 + 00 0	1.0 V -		, v 33 – L v 330		• /

(Notes, Caution, and Remarks are listed on the next page.)



(2) When reference voltage (+) = AVREFP/ANIO (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

 $(TA = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{EVDD0} = \text{EVDD1} \le \text{VDD} \le 5.5 \text{ V}, 1.6 \text{ V} \le \text{AVREFP} \le \text{VDD} \le 5.5 \text{ V}, \text{Vss} = \text{EVss0} = \text{EVss1} = 0 \text{ V}, \text{Reference voltage (+)} = \text{AVREFP}, \text{Reference voltage (-)} = \text{AVREFM} = 0 \text{ V})$

Parameter	Symbol	Condi	itions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	$1.8~V \le AV_{REFP} \le 5.5~V$		1.2	±5.0	LSB
		$EV_{DD0} \le AV_{REFP} = V_{DD}$ Notes 3, 4	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}^{\text{Note 5}}$		1.2	±8.5	LSB
Conversion time	tconv	10-bit resolution	$3.6~V \leq V_{DD} \leq 5.5~V$	2.125		39	μs
		Target ANI pin: ANI16 to ANI20	$2.7~V \leq V_{DD} \leq 5.5~V$	3.1875		39	μs
			$1.8~V \le V_{DD} \le 5.5~V$	17		39	μs
			$1.6~V \leq V_{DD} \leq 5.5~V$	57		95	μs
Zero-scale error Notes 1, 2	Ezs	10-bit resolution	$1.8 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±0.35	%FSR
		$EV_{DD0} \le AV_{REFP} = V_{DD}$ Notes 3, 4	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}^{\text{Note 5}}$			±0.60	%FSR
Full-scale error Notes 1, 2	Efs	10-bit resolution	$1.8 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±0.35	%FSR
		$EV_{DD0} \le AV_{REFP} = V_{DD}$ Notes 3, 4	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}^{\text{Note 5}}$			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	$1.8 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±3.5	LSB
		$EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.6~V \leq AV_{REFP} \leq 5.5~V$ Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$1.8 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±2.0	LSB
		$EV_{DD0} \le AV_{REFP} = V_{DD}$ Notes 3, 4	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}^{\text{Note 5}}$			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AVREFP and EVDD0	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EVDD0 \le AVREFP \le VDD$, the MAX. values are as follows.

 Overall error:
 Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

 Zero-scale error/Full-scale error:
 Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

 Integral linearity error/ Differential linearity error:
 Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

 Note 4.
 When AVREFP < EVDD0 ≤ VDD, the MAX. values are as follows.</td>

 Overall error:
 Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

 Zero-scale error/Full-scale error:
 Add ±0.20%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.

Note 5. When the conversion time is set to 57 μ s (min.) and 95 μ s (max.).



3.2 Oscillator Characteristics

3.2.1 X1, XT1 characteristics

$(TA = -40 \text{ to } +105^{\circ}C, 2.4 \text{ V} \le \text{VDD} \le 5.5 \text{ V}, \text{Vss} = 0 \text{ V})$

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/	$2.7~V \leq V \text{DD} \leq 5.5~V$	1.0		20.0	MHz
	crystal resonator	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	1.0		16.0	
XT1 clock oscillation frequency (fxT) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G14 User's Manual.

3.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V \leq VDD \leq 5.5 V, Vss = 0 V)

Oscillators	Parameters	Conditions			TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fін					32	MHz
High-speed on-chip oscillator clock frequency		-20 to +85°C	$2.4~V \leq V \text{DD} \leq 5.5~V$	-1.0		+1.0	%
accuracy		-40 to -20°C	$2.4~V \leq V \text{DD} \leq 5.5~V$	-1.5		+1.5	%
		+85 to +105°C	$2.4~V \leq V \text{DD} \leq 5.5~V$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.



Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	Vih1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0.8 EVDD0		EVddo	V
	VIH2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	2.2		EVDD0	V
			TTL input buffer $3.3 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}$	2.0		EVDD0	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	Vінз	P20 to P27, P150 to P156	0.7 Vdd		Vdd	V	
	VIH4	P60 to P63	0.7 EVDD0		6.0	V	
	Vih5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 Vdd		Vdd	V
Input voltage, low	VIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
	VIL2 P01, P0 P30, P4 P80, P8	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55,	TTL input buffer $4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$	0		0.8	V
		P80, P81, P142, P143	TTL input buffer $3.3 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}$	0		0.5	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	0		0.32	V
	VIL3	P20 to P27, P150 to P156		0		0.3 VDD	V
	VIL4	P60 to P63		0		0.3 EVDD0	V
	VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

(3/5)

The maximum value of VIH of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins. Remark

Caution



- Note 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or Vss, EVss0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2. During HALT instruction execution by flash memory.
- **Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4. When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7 \text{ V} \le \text{Vdd} \le 5.5 \text{ V}$ @1 MHz to 32 MHz
 - 2.4 V \leq VDD \leq 5.5 V@1 MHz to 16 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3. fill: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



- Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
- **Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
- Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- **Note 8.** Current flowing during programming of the data flash.
- Note 9. Current flowing during self-programming.
- Note 10. For shift time to the SNOOZE mode, see 23.3.3 SNOOZE mode in the RL78/G14 User's Manual.
- **Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the HALT mode.
- **Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Note 13. A comparator and D/A converter are provided in products with 96 KB or more code flash memory.
- Remark 1. fil: Low-speed on-chip oscillator clock frequency
- Remark 2. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3. fcLK: CPU/peripheral hardware clock frequency
- Remark 4. Temperature condition of the TYP. value is TA = 25°C



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

- **Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
 - h: POM number (h = 0, 1, 3 to 5, 7, 14)
- Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)



(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
Transfer rate	transmission		$\begin{array}{l} 4.0 \ V \leq E V_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V \end{array} \end{array} \label{eq:VD0}$		Note 1	bps
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 k\Omega, V_b = 2.7 V		2.6 Note 2	Mbps	
		2 2	$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 k\Omega, V_b = 2.3 V		1.2 Note 4	Mbps
			$\begin{array}{l} 2.4 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V \end{array}$		Note 5	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 k Ω , V_b = 1.6 V		0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using fMCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V \leq EVDD0 \leq 5.5 V and 2.7 V \leq Vb \leq 4.0 V

Maximum transfer rate =
$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3}$$
Baud rate error (theoretical value) =
$$\frac{\frac{1}{Transfer rate \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\}}{(\frac{1}{Transfer rate}) \times Number of transferred bits}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

- Note 2.This value as an example is calculated when the conditions described in the "Conditions" column are met.Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- **Note 3.** The smaller maximum transfer rate derived by using fMck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V \leq EVDD0 < 4.0 V and 2.3 V \leq Vb \leq 2.7 V

Maximum transfer rate = -

$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\} \times 3}$$

1

al value) =
$$\frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times 100 [\%]}$$

Baud rate error (theoretical value) =

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4.This value as an example is calculated when the conditions described in the "Conditions" column are met.Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

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CSI mode connection diagram (during communication at different potential



- **Remark 5.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
- **Remark 6.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 7. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
- Remark 8. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.



(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +105°C, 2.4 V \leq VDD \leq 5.5 V, 1.6 V \leq EVDD = EVDD1 \leq VDD, Vss = EVsso = EVss1 = 0 V,

Reference voltage (+) = VBGR Note 3, Reference voltage (-) = AVREFM = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$	17		39	μs
Zero-scale error Notes 1, 2	Ezs	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±1.0	LSB
Analog input voltage	Vain			0		VBGR Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = Vss, the MAX. values are as follows.

Zero-scale error:Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.Integral linearity error:Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.Differential linearity error:Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.



4.10 100-pin products

R5F104PFAFB, R5F104PGAFB, R5F104PHAFB, R5F104PJAFB R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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