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What is "[Embedded - Microcontrollers](#)"?

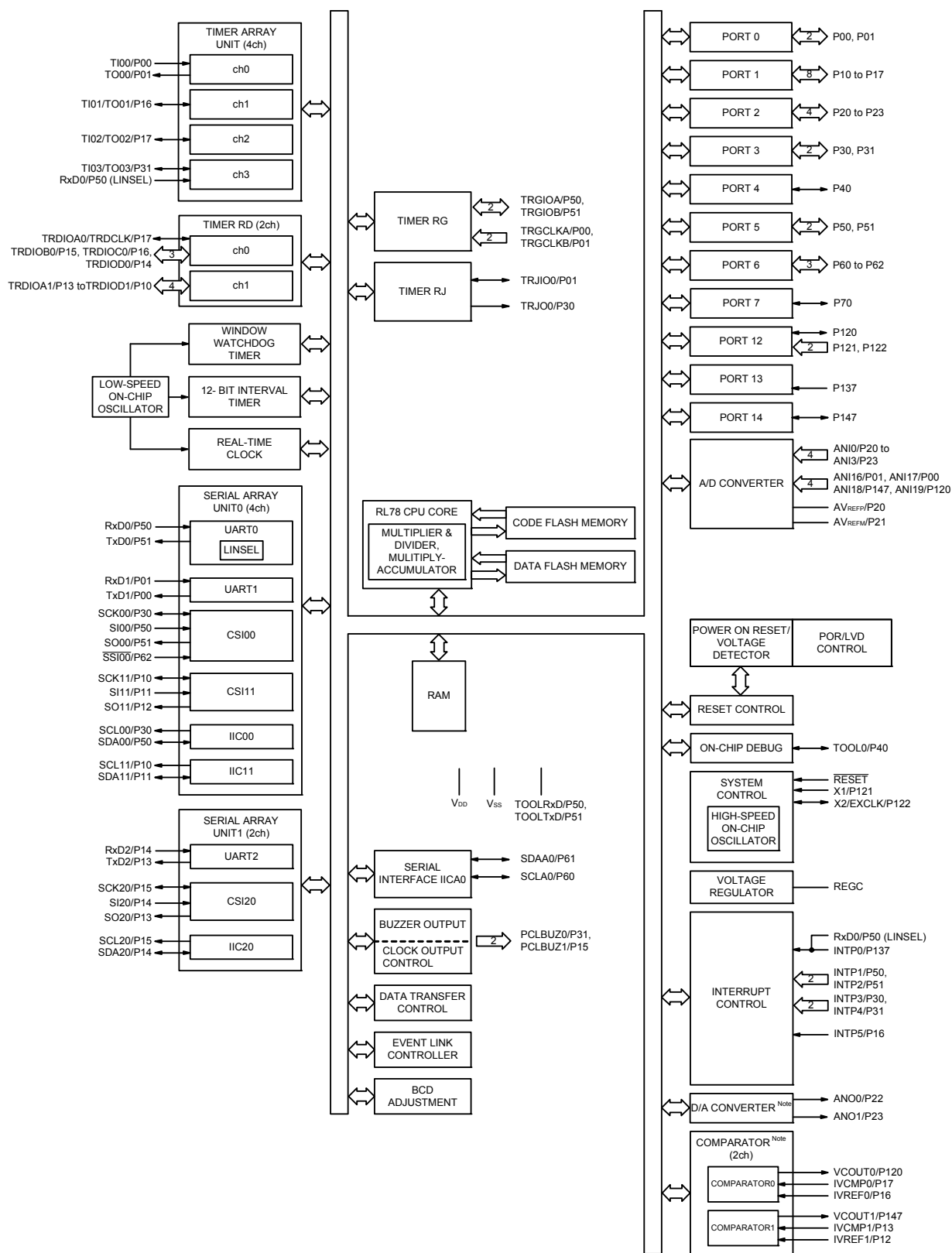
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fjafp-v0

1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.

(2/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Clock output/buzzer output		2	2	2	2
		<ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 			
8/10-bit resolution A/D converter		10 channels	10 channels	12 channels	12 channels
Serial interface		<p>[44-pin products]</p> <ul style="list-style-type: none"> CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[48-pin, 52-pin products]</p> <ul style="list-style-type: none"> CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[64-pin products]</p> <ul style="list-style-type: none"> CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		29 sources	30 sources		31 sources
Event link controller (ELC)		Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt		4	6	8	8
Reset		<ul style="list-style-type: none"> Reset by $\overline{\text{RESET}}$ pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access 			
Power-on-reset circuit		<ul style="list-style-type: none"> Power-on-reset: 1.51 ±0.04 V (T_A = -40 to +85°C) 1.51 ±0.06 V (T_A = -40 to +105°C) Power-down-reset: 1.50 ±0.04 V (T_A = -40 to +85°C) 1.50 ±0.06 V (T_A = -40 to +105°C) 			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)			
Operating ambient temperature		T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7		mA
						VDD = 3.0 V		5.1	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9		
						VDD = 3.0 V		4.0	6.9		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3		
						VDD = 3.0 V		3.8	6.3		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0		mA
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8		mA
						VDD = 2.0 V		1.3	1.8		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3		mA
						Resonator connection		3.4	5.5		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3		
						Resonator connection		3.4	5.5		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
			LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9		mA
						Resonator connection		1.2	2.0		
				fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9		
						Resonator connection		1.2	2.0		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IIH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.9		mA
						V _{DD} = 3.0 V		2.9		
				f _{HOCO} = 32 MHz, f _{IIH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.5		
						V _{DD} = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IIH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		6.0	11.2	mA
						V _{DD} = 3.0 V		6.0	11.2	
				f _{HOCO} = 32 MHz, f _{IIH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.5	10.6	
						V _{DD} = 3.0 V		5.5	10.6	
				f _{HOCO} = 48 MHz, f _{IIH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.7	8.6	
						V _{DD} = 3.0 V		4.7	8.6	
				f _{HOCO} = 24 MHz, f _{IIH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.4	8.2	
						V _{DD} = 3.0 V		4.4	8.2	
				f _{HOCO} = 16 MHz, f _{IIH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.3	5.9	
						V _{DD} = 3.0 V		3.3	5.9	
			LS (low-speed main) mode Note 5	f _{HOCO} = 8 MHz, f _{IIH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.5	mA
						V _{DD} = 2.0 V		1.5	2.5	
			LV (low-voltage main) mode Note 5	f _{HOCO} = 4 MHz, f _{IIH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.1	mA
						V _{DD} = 2.0 V		1.5	2.1	
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8	
						Resonator connection		3.9	7.0	
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
			LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		5.2		μA
						Resonator connection		5.2		
				f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz |
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
- Note 8.** Current flowing during programming of the data flash.
- Note 9.** Current flowing during self-programming.
- Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.
- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{CMP} when the comparator circuit is in operation.
- Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

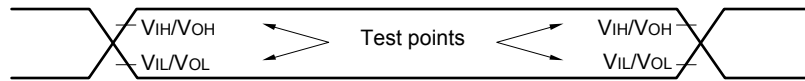
Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.8 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.7 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.6 V ≤ EVDD0 ≤ 5.5 V	—			fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3	—			1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 < 2.4 V: MAX. 1.3 Mbps

1.6 V ≤ EVDD0 < 1.8 V: MAX. 0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

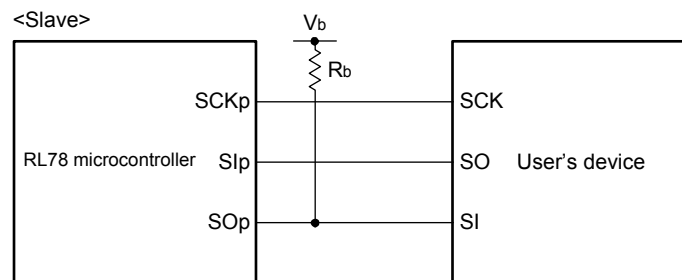
(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with EV_{DD0} ≥ V_b.
- Note 3.** When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
- Note 4.** When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
- Note 5.** When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
- Caution** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remark 1.** R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode Note 7	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	4.36	mA	
				VDD = 3.0 V		0.80	4.36			
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	3.67		
				VDD = 3.0 V		0.49	3.67			
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.42		
				VDD = 3.0 V		0.62	3.42			
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.85		
				VDD = 3.0 V		0.4	2.85			
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	2.08		
				VDD = 3.0 V		0.37	2.08			
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	2.45	mA	
				Resonator connection		0.40	2.57			
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28	2.45		
				Resonator connection		0.40	2.57			
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19	1.28		
				Resonator connection		0.25	1.36			
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.19	1.28		
				Resonator connection		0.25	1.36			
		Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA		
			Resonator connection		0.44	0.76				
			fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57			
			Resonator connection		0.49	0.76				
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17			
			Resonator connection		0.59	1.36				
			fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97			
			Resonator connection		0.72	2.16				
			fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37			
			Resonator connection		1.16	3.56				
			fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		3.20	17.10			
			Resonator connection		3.40	17.50				
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
			TA = +25°C					0.24	0.51	
			TA = +50°C					0.29	1.10	
			TA = +70°C					0.41	1.90	
			TA = +85°C					0.90	3.30	
			TA = +105°C					3.10	17.00	

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

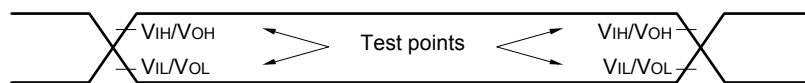
<R>

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

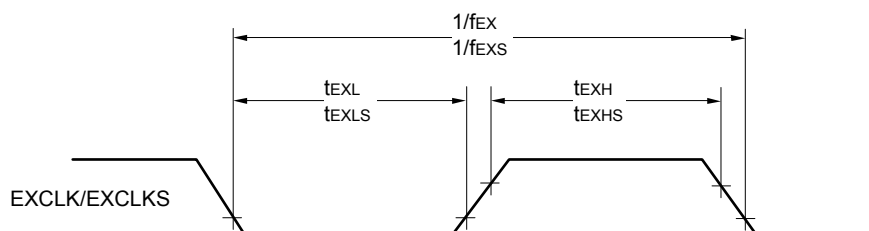
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode Note 7	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	5.16	mA	
					VDD = 3.0 V		0.93	5.16		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	4.47		
					VDD = 3.0 V		0.5	4.47		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	4.08		
					VDD = 3.0 V		0.72	4.08		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	3.51		
					VDD = 3.0 V		0.42	3.51		
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	2.38		
					VDD = 3.0 V		0.39	2.38		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	2.83	mA	
					Resonator connection		0.41	2.92		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	2.83		
					Resonator connection		0.41	2.92		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21	1.46		
					Resonator connection		0.26	1.57		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	1.46		
					Resonator connection		0.26	1.57		
		Subsystem clock operation	fsUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31	0.76	μA		
				Resonator connection		0.50	0.95			
				fsUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.38		0.76	
					Resonator connection		0.57		0.95	
				fsUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47		3.59	
					Resonator connection		0.70		3.78	
				fsUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80		6.20	
					Resonator connection		1.00		6.39	
				fsUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65		10.56	
					Resonator connection		1.84		10.75	
				fsUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		8.00		65.7	
					Resonator connection		8.00		65.7	
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19	0.63	μA
			TA = +25°C					0.30	0.63	
			TA = +50°C					0.41	3.47	
			TA = +70°C					0.80	6.08	
			TA = +85°C					1.53	10.44	
			TA = +105°C					6.50	67.14	

(Notes and Remarks are listed on the next page.)

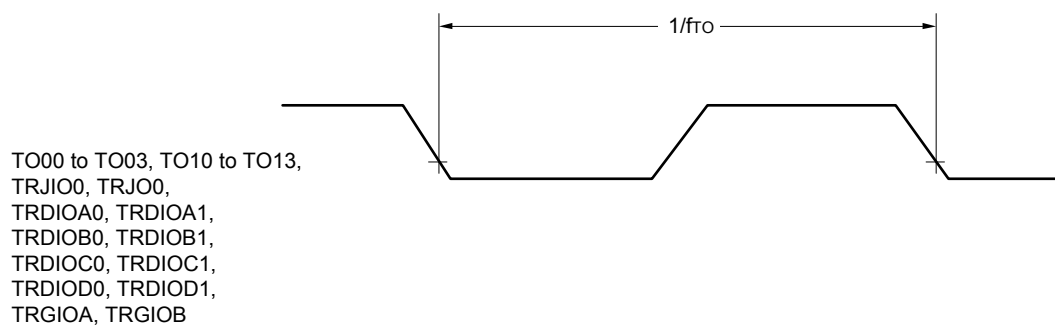
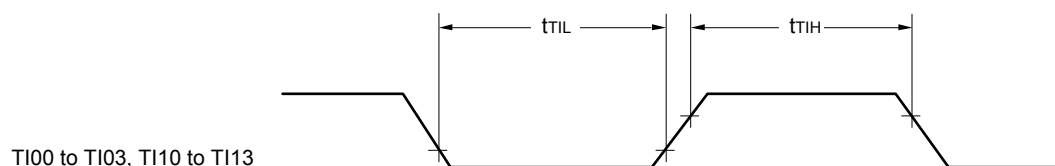
AC Timing Test Points



External System Clock Timing



TI/TO Timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
Input channel			
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI20	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} ,
Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14	0		AV_{REFP}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{BGR} Note 4			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{TMPS25} Note 4			V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) Interrupt & Reset Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.7 Power supply voltage rising slope characteristics**($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

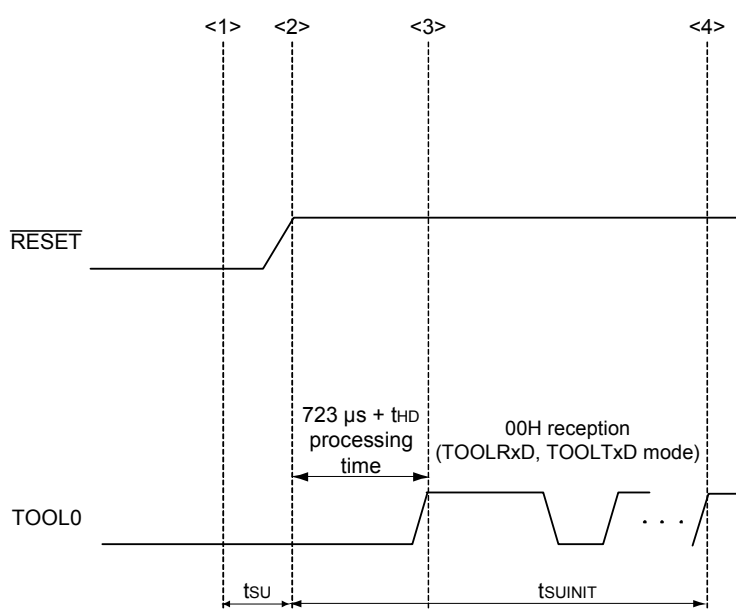
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

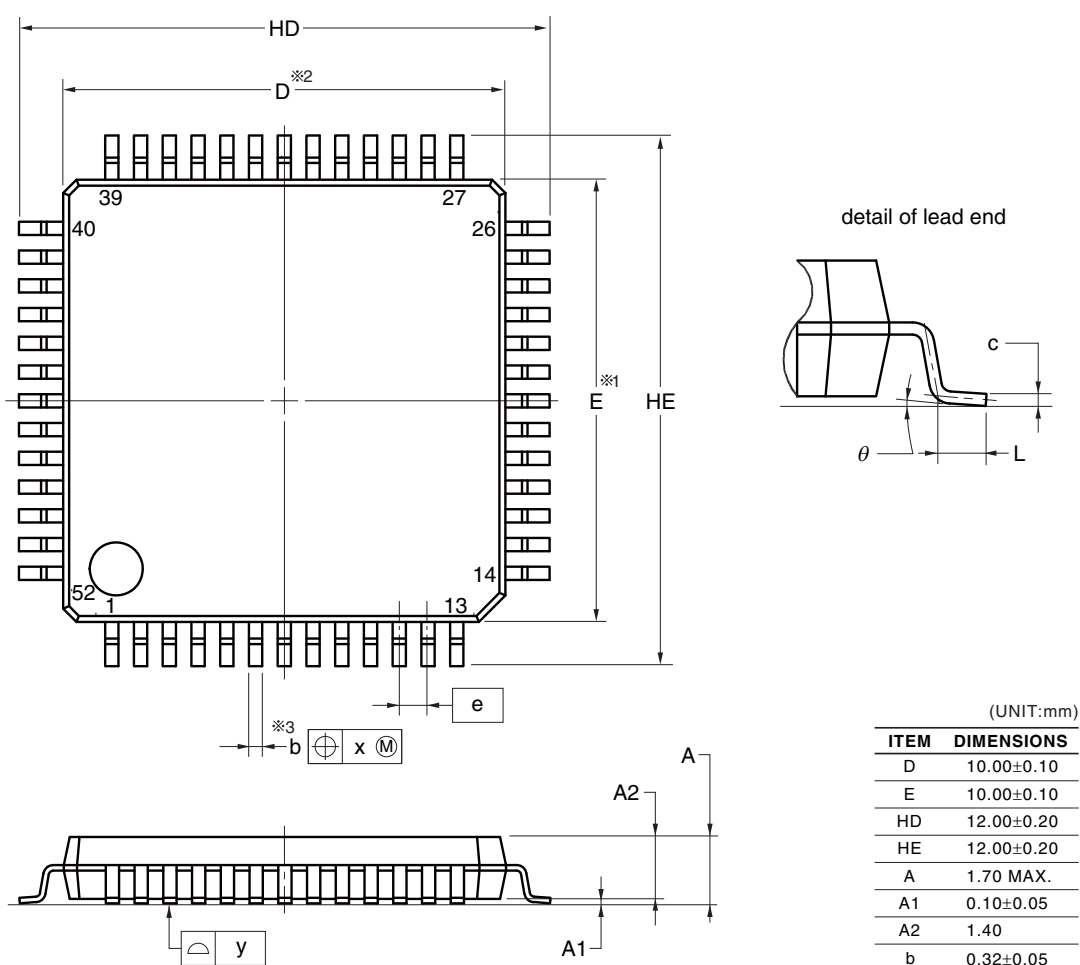
t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t_{HD} : How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
 R5F104JCDAFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
 R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

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