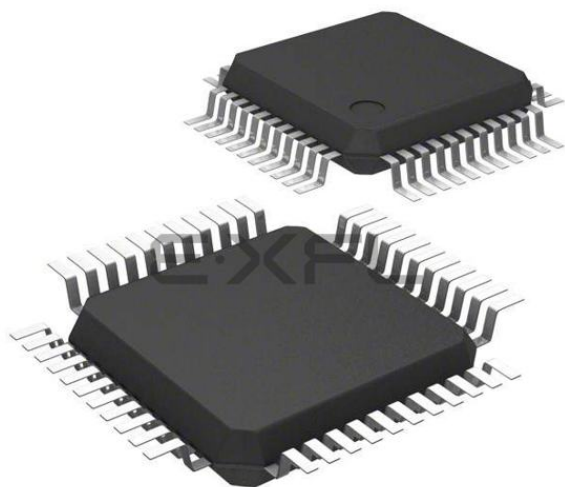




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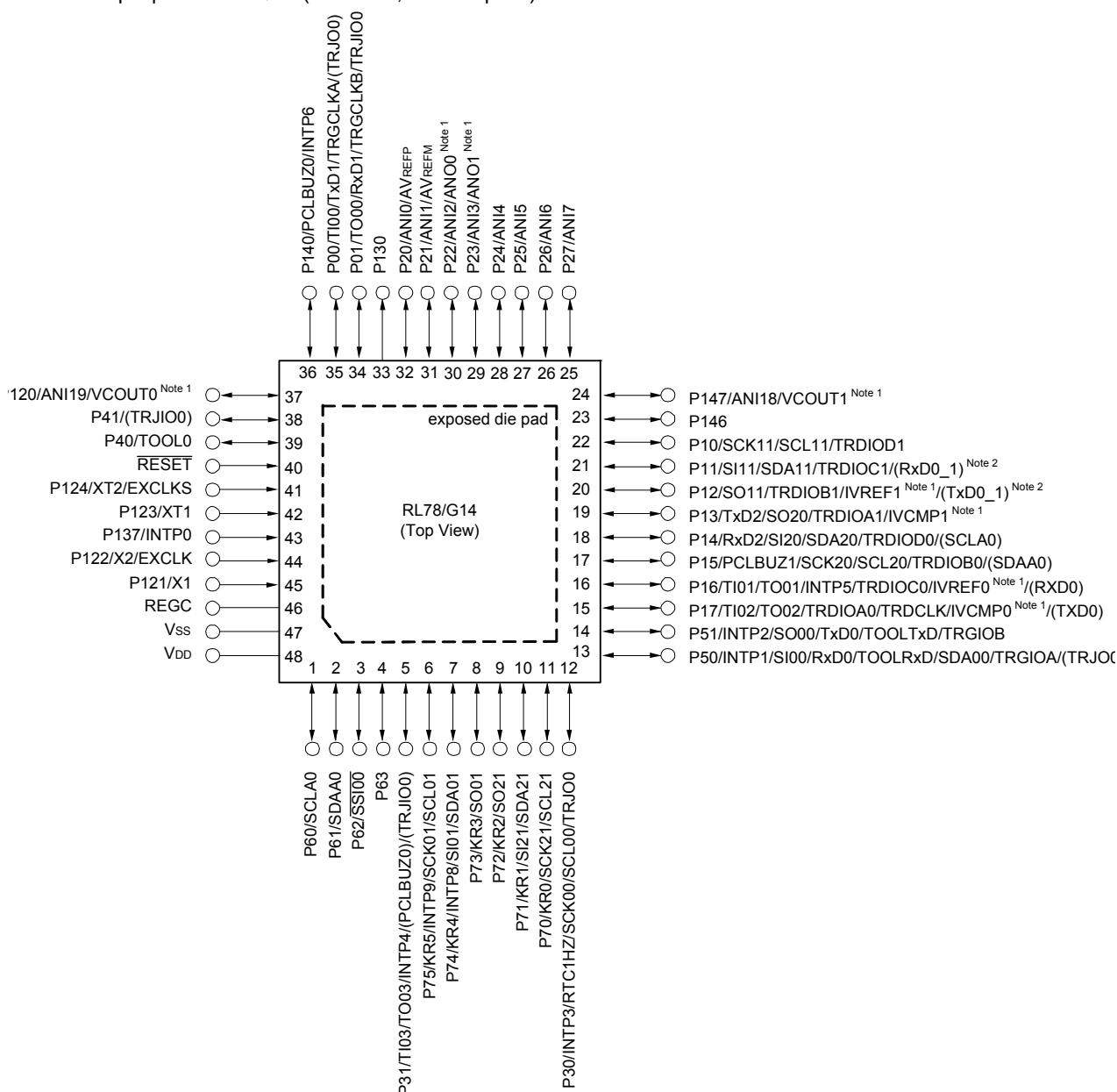
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fjafp-x0

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

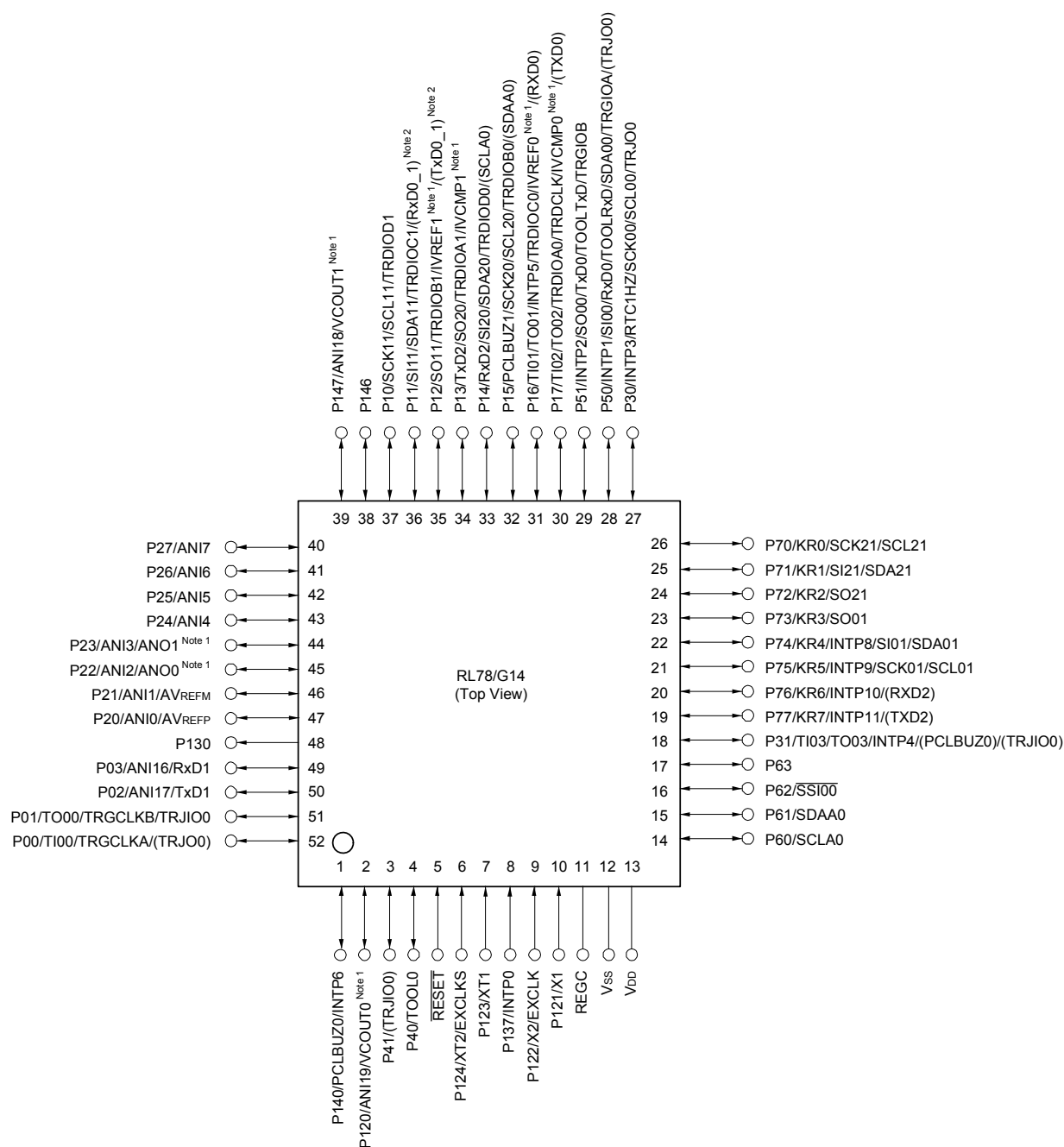
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

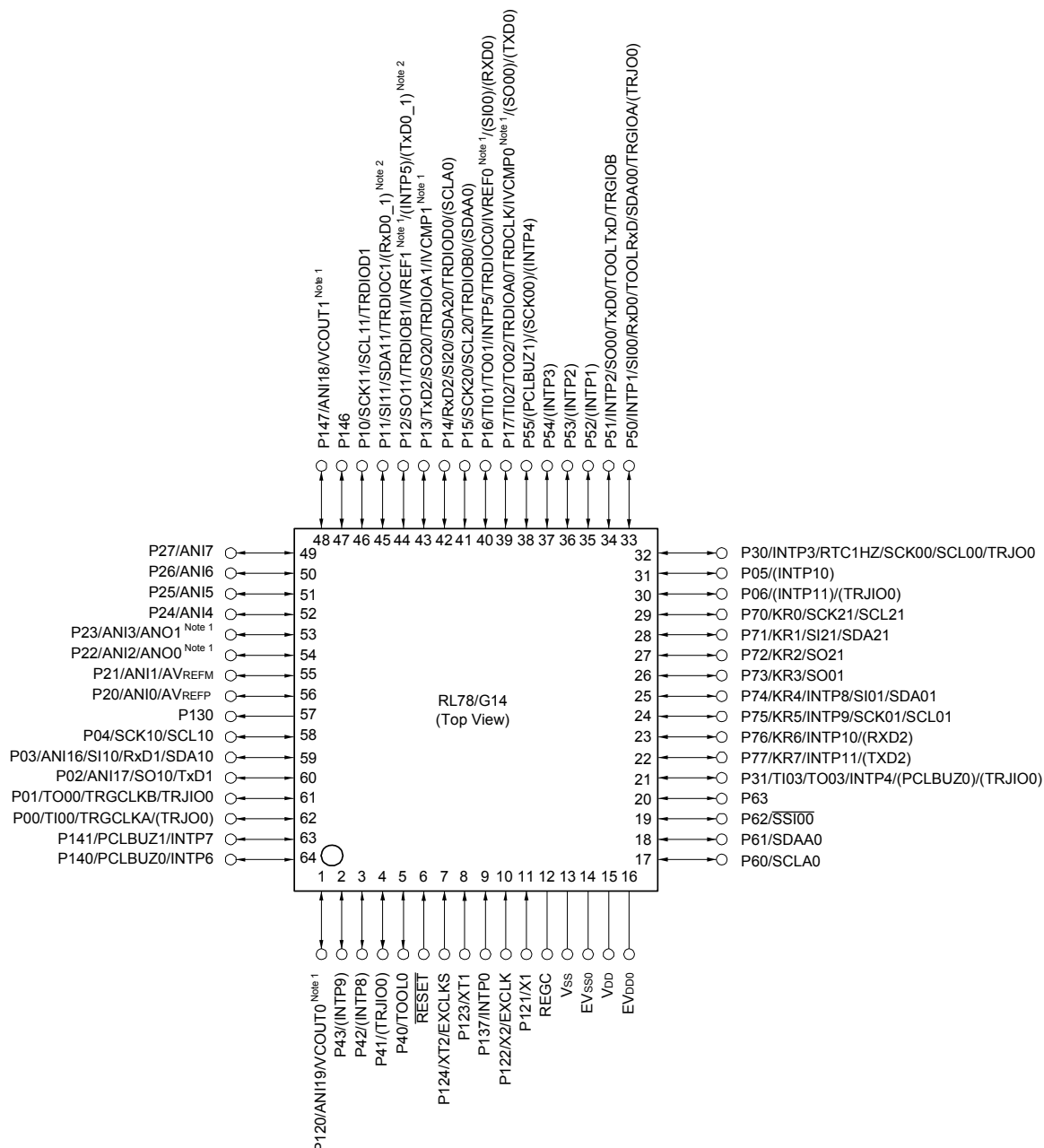
1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

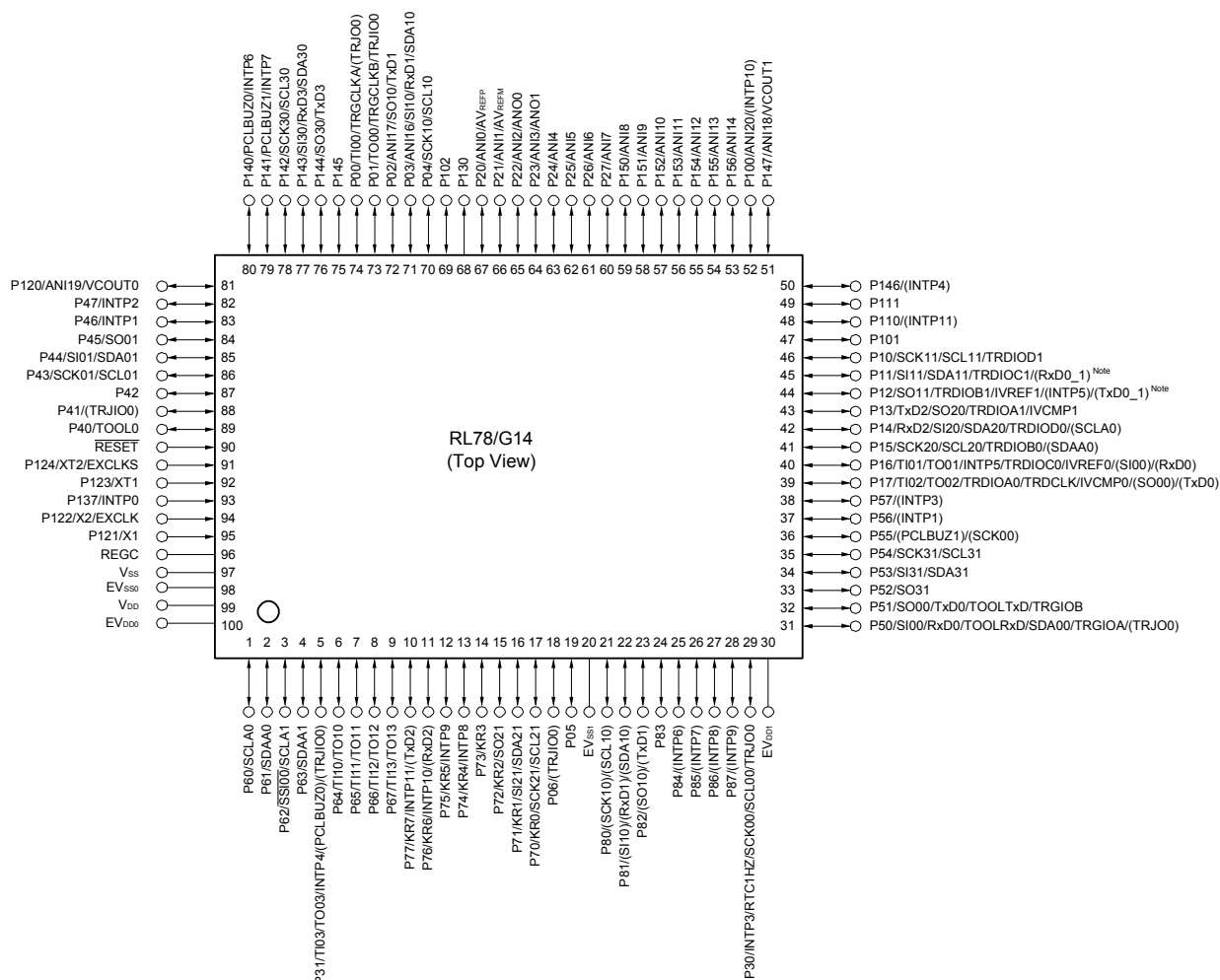
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0, EVSS1 pins the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVSS0 and EVSS1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		SCK00, SCK01, SCK10,:	Serial clock input/output
ANO0, ANO1:	Analog output	SCK11, SCK20, SCK21,	
AVREFM:	A/D converter reference potential (– side) input	SCK30, SCK31	
AVREFP:	A/D converter reference potential (+ side) input	SCLA0, SCLA1,:	Serial clock input/output
EVDD0, EVDD1:	Power supply for port	SCL00, SCL01, SCL10, SCL11,:	Serial clock output
EVSS0, EVSS1:	Ground for port	SCL20, SCL21, SCL30,	
EXCLK:	External clock input (main system clock)	SCL31	
EXCLKS:	External clock input (subsystem clock)	SDAA0, SDAA1, SDA00,:	Serial data input/output
INTP0 to INTP11:	External interrupt input	SDA01, SDA10, SDA11,	
IVCMP0, IVCMP1:	Comparator input	SDA20, SDA21, SDA30,	
IVREF0, IVREF1:	Comparator reference input	SDA31	
KR0 to KR7:	Key return	SI00, SI01, SI10, SI11,:	Serial data input
P00 to P06:	Port 0	SI20, SI21, SI30, SI31	
P10 to P17:	Port 1	SO00, SO01, SO10,:	Serial data output
P20 to P27:	Port 2	SO11, SO20, SO21,	
P30, P31:	Port 3	SO30, SO31	
P40 to P47:	Port 4	$\overline{\text{SSI00}}$:	Serial interface chip select input
P50 to P57:	Port 5	TI00 to TI03,:	Timer input
P60 to P67:	Port 6	TI10 to TI13	
P70 to P77:	Port 7	TO00 to TO03,:	Timer output
P80 to P87:	Port 8	TO10 to TO13, TRJ00	
P100 to P102:	Port 10	TOOL0:	Data input/output for tool
P110, P111:	Port 11	TOOLRxD, TOOLTxD:	Data input/output for external device
P120 to P124:	Port 12	TRDCLK, TRGCLKA,:	Timer external input clock
P130, P137:	Port 13	TRGCLKB	
P140 to P147:	Port 14	TRDIOA0, TRDIOB0,:	Timer input/output
P150 to P156:	Port 15	TRDIOC0, TRDIOD0,	
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	TRDIOA1, TRDIOB1,	
REGC:	Regulator capacitance	TRDIOC1, TRDIOD1,	
$\overline{\text{RESET}}$:	Reset	TRGIOA, TRGIOB, TRJIO0	
RTC1HZ:	Real-time clock correction clock (1 Hz) output	TxD0 to TxD3:	Transmit data
		VCOUT0, VCOUT1:	Comparator output
		VDD:	Power supply
		VSS:	Ground
		X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

Note In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

Absolute Maximum Ratings

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		VLVD1	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		VLVD2	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		VLVD3	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		VLVD4	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		VLVD5	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		VLVD6	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		VLVD7	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		VLVD8	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		VLVD9	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		VLVD10	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		VLVD11	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		VLVD12	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		VLVD13	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _I REGC	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3 Note 2	V
Analog input voltage	V _{AI1}	ANI16 to ANI20	-0.3 to EV _{DD0} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

3.2 Oscillator Characteristics

3.2.1 X1, XT1 characteristics

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	
XT1 clock oscillation frequency (f_{XT1}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to $+85^{\circ}\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		+1.0	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
		$+85$ to $+105^{\circ}\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	4.36	mA	
					VDD = 3.0 V		0.80	4.36		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	3.67		
					VDD = 3.0 V		0.49	3.67		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.42		
					VDD = 3.0 V		0.62	3.42		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.85		
					VDD = 3.0 V		0.4	2.85		
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	2.08			
				VDD = 3.0 V		0.37	2.08			
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	2.45	mA	
					Resonator connection		0.40	2.57		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28	2.45		
					Resonator connection		0.40	2.57		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19	1.28		
					Resonator connection		0.25	1.36		
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input		0.19	1.28			
				Resonator connection		0.25	1.36			
		Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA		
				Resonator connection		0.44	0.76			
			fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57			
				Resonator connection		0.49	0.76			
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17			
				Resonator connection		0.59	1.36			
			fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97			
				Resonator connection		0.72	2.16			
			fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37			
				Resonator connection		1.16	3.56			
			fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		3.20	17.10			
				Resonator connection		3.40	17.50			
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
			TA = +25°C					0.24	0.51	
			TA = +50°C					0.29	1.10	
			TA = +70°C					0.41	1.90	
			TA = +85°C					0.90	3.30	
			TA = +105°C					3.10	17.00	

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	4.86	mA
					VDD = 3.0 V		0.79	4.86	
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	4.17	
					VDD = 3.0 V		0.49	4.17	
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.82	
					VDD = 3.0 V		0.62	3.82	
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	3.25	
					VDD = 3.0 V		0.4	3.25	
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	2.28	
					VDD = 3.0 V		0.38	2.28	
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	2.65	mA
					Resonator connection		0.40	2.77	
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30	2.65	
					Resonator connection		0.40	2.77	
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
	IDD3 Note 6	STOP mode Note 8	Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA
					Resonator connection		0.47	0.85	
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66	
					Resonator connection		0.53	0.85	
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35	
					Resonator connection		0.56	2.54	
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08	
					Resonator connection		0.80	4.27	
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09	
					Resonator connection		1.74	8.28	
				fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		6.00	51.00	
					Resonator connection		6.00	51.00	
				TA = -40°C			0.19	0.57	μA
				TA = +25°C			0.25	0.57	
				TA = +50°C			0.33	2.26	
				TA = +70°C			0.52	3.99	
				TA = +85°C			1.46	8.00	
				TA = +105°C			5.50	50.00	

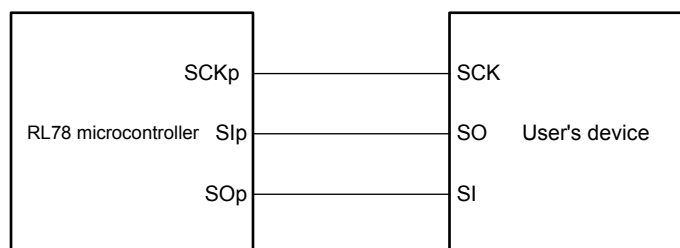
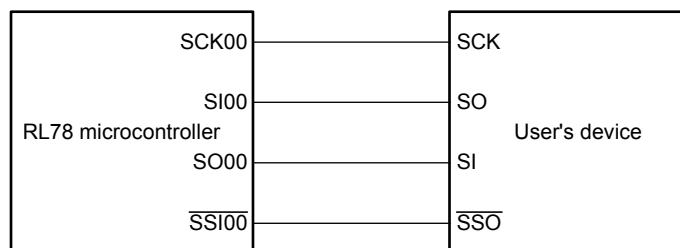
(Notes and Remarks are listed on the next page.)

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{\text{SSI00}}$ setup time	t_{SSIK}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
$\overline{\text{SSI00}}$ hold time	t_{kSSI}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

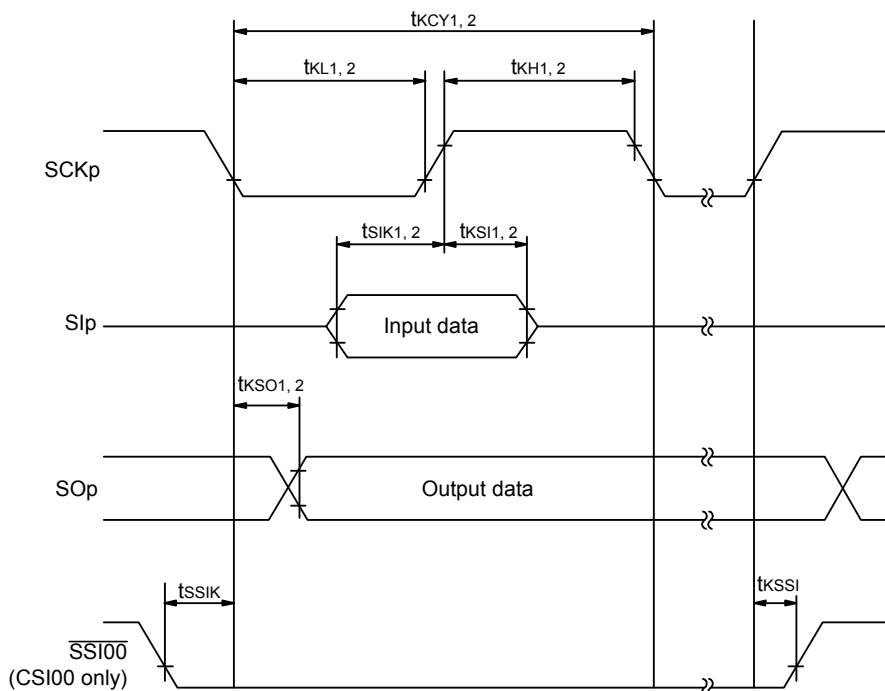
Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)
CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))


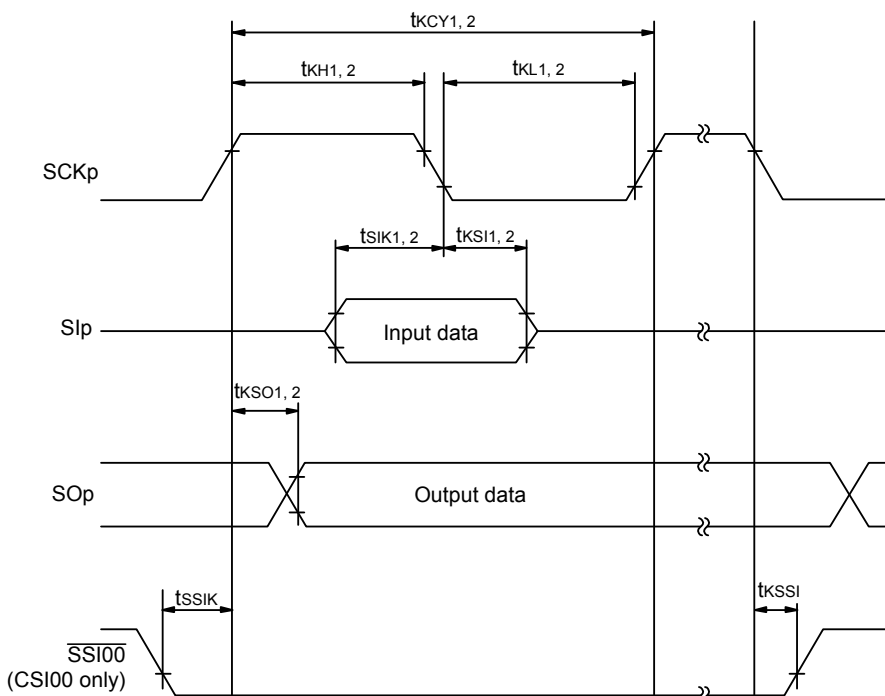
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	tsik1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	tkS11	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/ EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

3.5.2 Serial interface IICA

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: fCLK ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	tSU: STA		4.7		0.6		μs
Hold time ^{Note 1}	tHD: STA		4.0		0.6		μs
Hold time when SCLA0 = “L”	tLOW		4.7		1.3		μs
Hold time when SCLA0 = “H”	tHIGH		4.0		0.6		μs
Data setup time (reception)	tSU: DAT		250		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT		0	3.45	0	0.9	μs
Setup time of stop condition	tSU: STO		4.0		0.6		μs
Bus-free time	tBUF		4.7		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of t_{HD: DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

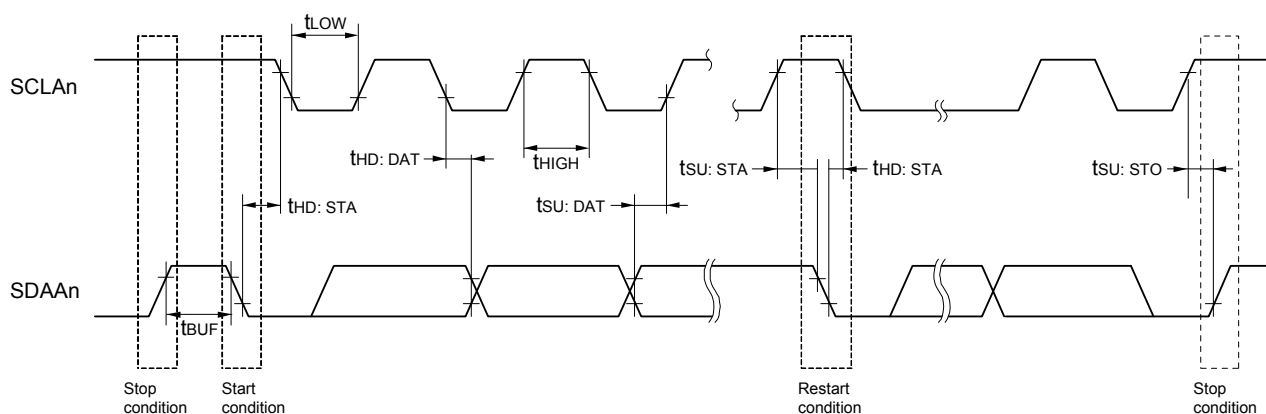
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

(2) Interrupt & Reset Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.7 Power supply voltage rising slope characteristics**($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

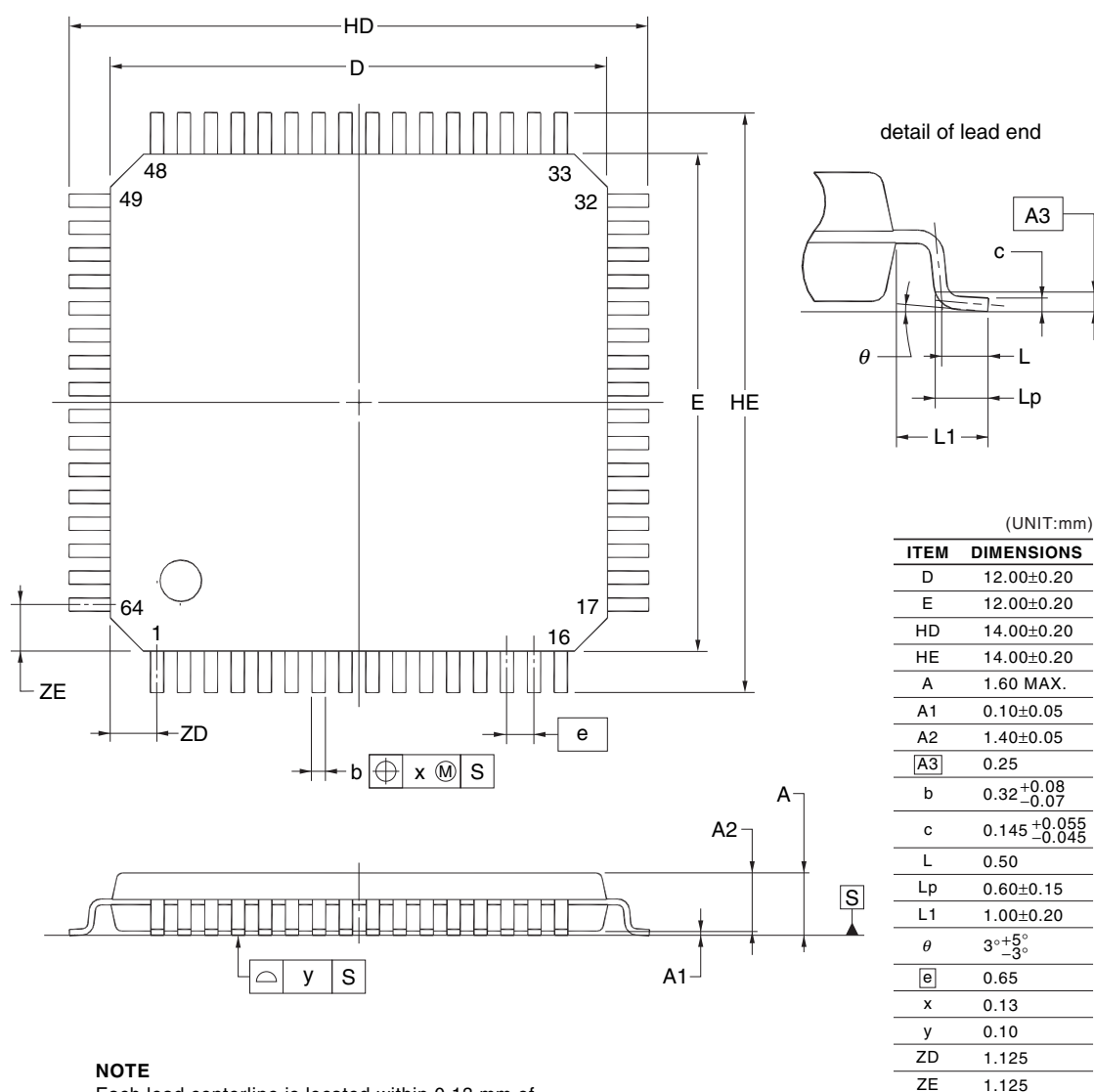
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFa, R5F104LHAFA, R5F104LJAFA
 R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFa, R5F104LHDFa, R5F104LJDFA
 R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
 R5F104LKAFA, R5F104LLAFA
 R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

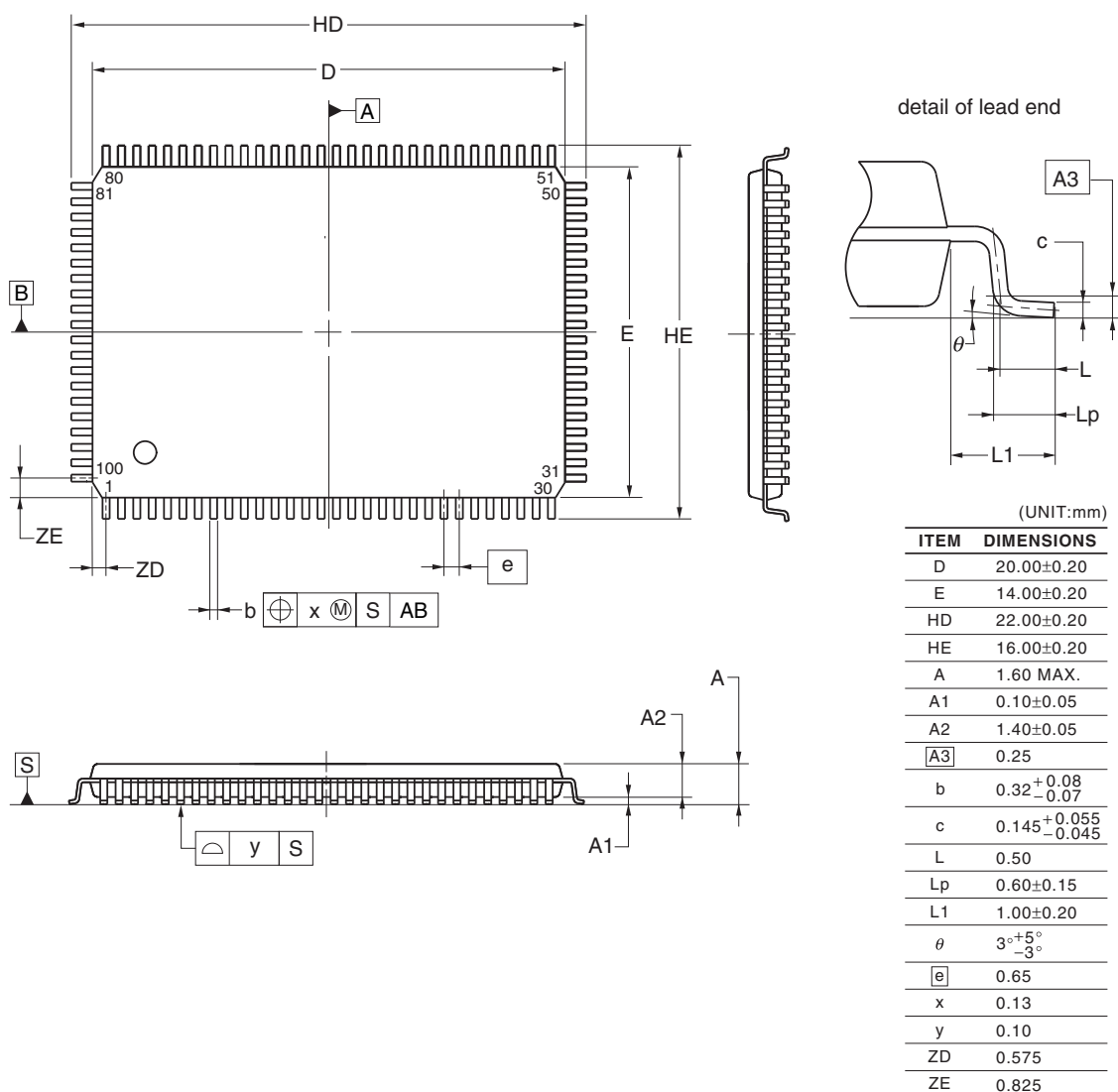


NOTE

Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJFAFA
 R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFA
 R5F104PFGFA, R5F104PGGFA, R5F104PHGFA, R5F104PJGFA
 R5F104PKAFA, R5F104PLAFA
 R5F104PKGFA, R5F104PLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



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