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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104fjdfp-v0

(1/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0
			R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0
			R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0
			R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0
			R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0
			R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0
			R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0
			R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BFDFP#V0, R5F104BGDFP#V0
			R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BFDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0
			R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0
			R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0
			R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**
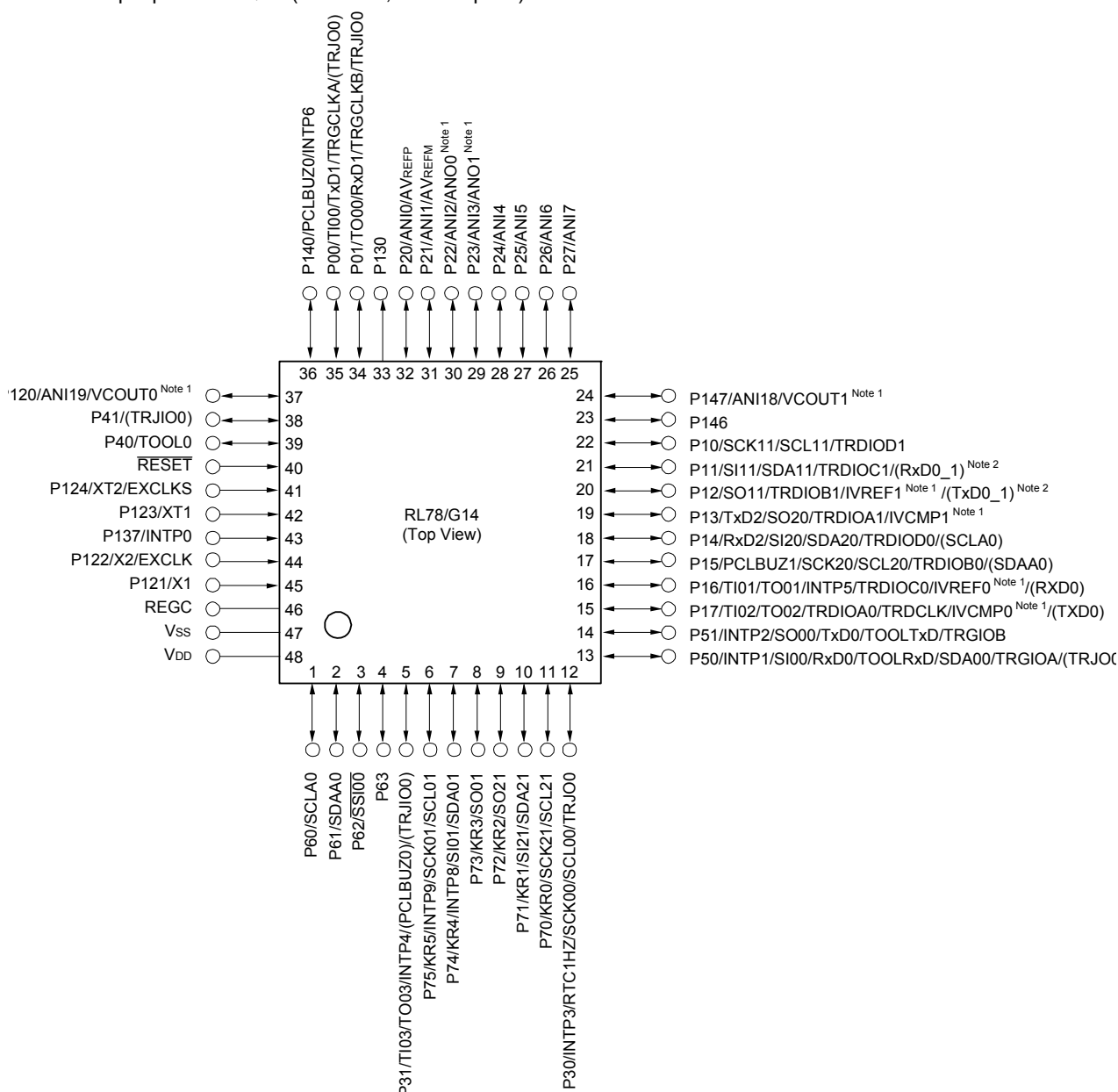
(2/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	A	R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0
			R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0
		D	R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0
			R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0
		G	R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0
			R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0
44 pins	44-pin plastic LQFP (10 × 10, 0.8 mm pitch)	A	R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0
			R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0
		D	R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0
			R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0
		G	R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0
			R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0

Note   For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution   **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

1.3.6 48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

RL78/G14
(Top View)

Top pins (36 to 25):
- 36 P140/PCLBUZ0/INTP6
- 35 P00/TI00/TxD1/TRGCLKA/(TRJO0)
- 34 P01/TO00/RxD1/TRGCLKB/TRJIO0
- 33 P130
- 32 P20/ANI0/AV$_{REFP}$
- 31 P21/ANI1/AV$_{REFM}$
- 30 P22/ANI2/ANO0 [Note 1]
- 29 P23/ANI3/ANO1 [Note 1]
- 28 P24/ANI4
- 27 P25/ANI5
- 26 P26/ANI6
- 25 P27/ANI7

Left pins (37 to 48):
- 37 P120/ANI19/VCOUT0 [Note 1]
- 38 P41/(TRJIO0)
- 39 P40/TOOL0
- 40 $\overline{\text{RESET}}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 Vss
- 48 VDD

Right pins (24 to 13):
- 24 P147/ANI18/VCOUT1 [Note 1]
- 23 P146
- 22 P10/SCK11/SCL11/TRDIOD1
- 21 P11/SI11/SDA11/TRDIOC1/(RxD0_1) [Note 2]
- 20 P12/SO11/TRDIOB1/IVREF1 [Note 1]/(TxD0_1) [Note 2]
- 19 P13/TxD2/SO20/TRDIOA1/IVCMP1 [Note 1]
- 18 P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
- 17 P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
- 16 P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 [Note 1]/(RXD0)
- 15 P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 [Note 1]/(TXD0)
- 14 P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
- 13 P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)

Bottom pins (1 to 12):
- 1 P60/SCLA0
- 2 P61/SDAA0
- 3 P62/$\overline{\text{SSI00}}$
- 4 P63
- 5 P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)
- 6 P75/KR5/INTP9/SCK01/SCL01
- 7 P74/KR4/INTP8/SI01/SDA01
- 8 P73/KR3/SO01
- 9 P72/KR2/SO21
- 10 P71/KR1/SI21/SDA21
- 11 P70/KR0/SCK21/SCL21
- 12 P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0

Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.9 80-pin products

TIMER ARRAY UNIT0 (4ch)
- TI00/P00, TO00/P01 → ch0
- TI01/TO01/P16 → ch1
- TI02/TO02/P17 → ch2
- TI03/TO03/P31, RxD0/P50 (LINSEL) → ch3

TIMER RD (2ch)
- TRDIOA0/TRDCLK/P17, TRDIOB0/P15, TRDIOC0/P16, TRDIOD0/P14 (3) → ch0
- TRDIOA1/P13 toTRDIOD1/P10 (4) → ch1

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12- BIT INTERVAL TIMER

REAL-TIME CLOCK
- RTC1HZ/P30

SERIAL ARRAY UNIT0 (4ch)
- RxD0/P50, TxD0/P51 → UART0 [LINSEL]
- RxD1/P03, TxD1/P02 → UART1
- SCK00/P30, SI00/P50, SO00/P51, SSI00/P62 → CSI00
- SCK01/P43, SI01/P44, SO01/P45 → CSI01
- SCK10/P04, SI10/P03, SO10/P02 → CSI10
- SCK11/P10, SI11/P11, SO11/P12 → CSI11
- SCL00/P30, SDA00/P50 → IIC00
- SCL01/P43, SDA01/P44 → IIC01
- SCL10/P04, SDA10/P03 → IIC10
- SCL11/P10, SDA11/P11 → IIC11

SERIAL ARRAY UNIT1 (4ch)
- RxD2/P14, TxD2/P13 → UART2
- RxD3/P143, TxD3/P144 → UART3
- SCK20/P15, SI20/P14, SO20/P13 → CSI20
- SCK21/P70, SI21/P71, SO21/P72 → CSI21
- SCK30/P142, SI30/P143, SO30/P144 → CSI30
- SCK31/P54, SI31/P53, SO31/P52 → CSI31
- SCL20/P15, SDA20/P14 → IIC20
- SCL21/P70, SDA21/P71 → IIC21
- SCL30/P142, SDA30/P143 → IIC30
- SCL31/P54, SDA31/P53 → IIC31

TIMER ARRAY UNIT1 (4ch)
- ch0 → TI10/TO10/P64
- ch1 → TI11/TO11/P65
- ch2 → TI12/TO12/P66
- ch3 → TI13/TO13/P67

TIMER RG
- (2) TRGIOA/P50, TRGIOB/P51
- (2) TRGCLKA/P00, TRGCLKB/P01

TIMER RJ
- TRJIO0/P01
- TRJO0/P30

A/D CONVERTER
- (8) ANI0/P20 to ANI7/P27
- (4) ANI8/P150 to ANI11/P153
- (5) ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120, ANI20/P100
- AVREFP/P20
- AVREFM/P21

RL78 CPU CORE
- MULTIPLIER & DIVIDER, MULITIPLY-ACCUMULATOR
- CODE FLASH MEMORY
- DATA FLASH MEMORY

RAM

VDD, EVDD0
VSS, EVSS0
TOOLRxD/P50, TOOLTxD/P51

SERIAL INTERFACE IICA0
- SDAA0/P61
- SCLA0/P60

SERIAL INTERFACE IICA1
- SDAA1/P63
- SCLA1/P62

BUZZER OUTPUT / CLOCK OUTPUT CONTROL
- (2) PCLBUZ0/P140, PCLBUZ1/P141

DATA TRANSFER CONTROL

EVENT LINK CONTROLLER

BCD ADJUSTMENT

PORT 0 → (7) P00 to P06
PORT 1 → (8) P10 to P17
PORT 2 → (8) P20 to P27
PORT 3 → (2) P30, P31
PORT 4 → (6) P40 to P45
PORT 5 → (6) P50 to P55
PORT 6 → (8) P60 to P67
PORT 7 → (8) P70 to P77
PORT 10 → P100
PORT 11 → (2) P110, P111
PORT 12 → P120, (4) P121 to P124
PORT 13 → P130, P137
PORT 14 → (7) P140 to P144, P146, P147
PORT 15 → (4) P150 to P153
KEY RETURN → (8) KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR | POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG → TOOL0/P40

SYSTEM CONTROL / HIGH-SPEED ON-CHIP OSCILLATOR
- RESET
- X1/P121
- X2/EXCLK/P122
- XT1/P123
- XT2/EXCLKS/P124

VOLTAGE REGULATOR → REGC

INTERRUPT CONTROL
- RxD0/P50 (LINSEL)
- INTP0/P137
- (2) INTP1/P50, INTP2/P51
- (2) INTP3/P30, INTP4/P31
- INTP5/P16
- (2) INTP6/P140, INTP7/P141
- (4) INTP8/P74 to INTP11/P77

D/A CONVERTER
- ANO0/P22
- ANO1/P23

COMPARATOR (2ch)
- COMPARATOR0 → VCOUT0/P120, IVCMP0/P17, IVREF0/P16
- COMPARATOR1 → VCOUT1/P147, IVCMP1/P13, IVREF1/P12

(2/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		17 channels	20 channels
D/A converter		2 channels	2 channels
Comparator		2 channels	2 channels
Serial interface		[80-pin, 100-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^{2}C: 2 channels	
	I^{2}C bus	2 channels	2 channels
Data transfer controller (DTC)		39 sources	39 sources
Event link controller (ELC)		Event input: 26 Event trigger output: 9	
Vectored interrupt sources	Internal	32	32
	External	13	13
Key interrupt		8	8
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access	

Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = −40 to +85°C)
		                   1.51 ±0.06 V (T_A = −40 to +105°C)
		• Power-down-reset: 1.50 ±0.04 V (T_A = −40 to +85°C)
		                   1.50 ±0.06 V (T_A = −40 to +105°C)	

Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

Note   The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Note   In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications TA = -40 to +85°C

          R5F104xxAxx

      D: Industrial applications TA = -40 to +85°C

        R5F104xxDxx

     G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C

        R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

(T_A = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -10.0 mA	EV$_{DD0}$ - 1.5			V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -3.0 mA	EV$_{DD0}$ - 0.7			V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = -1.5 mA	EV$_{DD0}$ - 0.5			V
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V, I$_{OH1}$ = -1.0 mA	EV$_{DD0}$ - 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OH2}$ = -100 µA	V$_{DD}$ - 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 20.0 mA			1.3	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
			1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 0.3 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OL2}$ = 400 µA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V
			1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 1.0 mA			0.4	V

Caution   **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3)　Flash ROM: 384 to 512 KB of 48- to 100-pin products

(T$_A$ = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)　　　　　　**(2/2)**

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD2}$ Note 2	HALT mode	HS (high-speed main) mode Note 7	f$_{HOCO}$ = 64 MHz, f$_{IH}$ = 32 MHz Note 4		V$_{DD}$ = 5.0 V		0.93	3.32	mA
						V$_{DD}$ = 3.0 V		0.93	3.32	
				f$_{HOCO}$ = 32 MHz, f$_{IH}$ = 32 MHz Note 4		V$_{DD}$ = 5.0 V		0.5	2.63	
						V$_{DD}$ = 3.0 V		0.5	2.63	
				f$_{HOCO}$ = 48 MHz, f$_{IH}$ = 24 MHz Note 4		V$_{DD}$ = 5.0 V		0.72	2.60	
						V$_{DD}$ = 3.0 V		0.72	2.60	
				f$_{HOCO}$ = 24 MHz, f$_{IH}$ = 24 MHz Note 4		V$_{DD}$ = 5.0 V		0.42	2.03	
						V$_{DD}$ = 3.0 V		0.42	2.03	
				f$_{HOCO}$ = 16 MHz, f$_{IH}$ = 16 MHz Note 4		V$_{DD}$ = 5.0 V		0.39	1.50	
						V$_{DD}$ = 3.0 V		0.39	1.50	
			LS (low-speed main) mode Note 7	f$_{HOCO}$ = 8 MHz, f$_{IH}$ = 8 MHz Note 4		V$_{DD}$ = 3.0 V		270	800	µA
						V$_{DD}$ = 2.0 V		270	800	
			LV (low-voltage main) mode Note 7	f$_{HOCO}$ = 4 MHz, f$_{IH}$ = 4 MHz Note 4		V$_{DD}$ = 3.0 V		450	755	µA
						V$_{DD}$ = 2.0 V		450	755	
			HS (high-speed main) mode Note 7	f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input			0.31	1.69	mA
					Resonator connection			0.41	1.91	
				f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input			0.31	1.69	
					Resonator connection			0.41	1.91	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input			0.21	0.94	
					Resonator connection			0.26	1.02	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input			0.21	0.94	
					Resonator connection			0.26	1.02	
			LS (low-speed main) mode Note 7	f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input			110	610	µA
					Resonator connection			150	660	
				f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 2.0 V	Square wave input			110	610	
					Resonator connection			150	660	
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = -40°C	Square wave input			0.31		µA
					Resonator connection			0.50		
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = +25°C	Square wave input			0.38	0.76	
					Resonator connection			0.57	0.95	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = +50°C	Square wave input			0.47	3.59	
					Resonator connection			0.70	3.78	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = +70°C	Square wave input			0.80	6.20	
					Resonator connection			1.00	6.39	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = +85°C	Square wave input			1.65	10.56	
					Resonator connection			1.84	10.75	
	I$_{DD3}$ Note 6	STOP mode Note 8	T$_A$ = -40°C					0.19		µA
			T$_A$ = +25°C					0.30	0.59	
			T$_A$ = +50°C					0.41	3.42	
			T$_A$ = +70°C					0.80	6.03	
			T$_A$ = +85°C					1.53	10.39	

(**Notes** and **Remarks** are listed on the next page.)

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq EV_{DD0}$ < 3.3 V and 1.6 V $\leq V_b \leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3} \ [bps]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T$_A$ = -40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   (2/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) Note 1	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		483		483		483	ns

Note 1.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2.   Use it with EV$_{DD0}$ ≥ V$_b$.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

2.6   Analog Characteristics

2.6.1   A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (-) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (-) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (-)= AV$_{REFM}$
ANI0 to ANI14	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI20	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		—

(1)   When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = -40 to +85°C, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (-) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Full-scale error [Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±5.0	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 5]		V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3.   When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
  Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
  Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
  Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Note 4.   Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).
Note 5.   Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 1.6 V $\leq$ EV$_{DD}$ = EV$_{DD1}$ $\leq$ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V,
Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (-) = AV$_{REFM}$ = 0 V [Note 4], HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±0.60	% FSR
Integral linearity error [Note 1]	ILE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3.   Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.
Note 4.   When reference voltage (-) = V$_{SS}$, the MAX. values are as follows.
　　　　　　Zero-scale error:　　　　　　　　Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV$_{REFM}$.
　　　　　　Integral linearity error:　　　　　Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.
　　　　　　Differential linearity error:　　　Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.

3.10   Timing of Entry to Flash Memory Programming Modes

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t$_{SUINIT}$	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t$_{SU}$	POR and LVD reset must end before the external reset ends.	10			µs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must end before the external reset ends.	1			ms
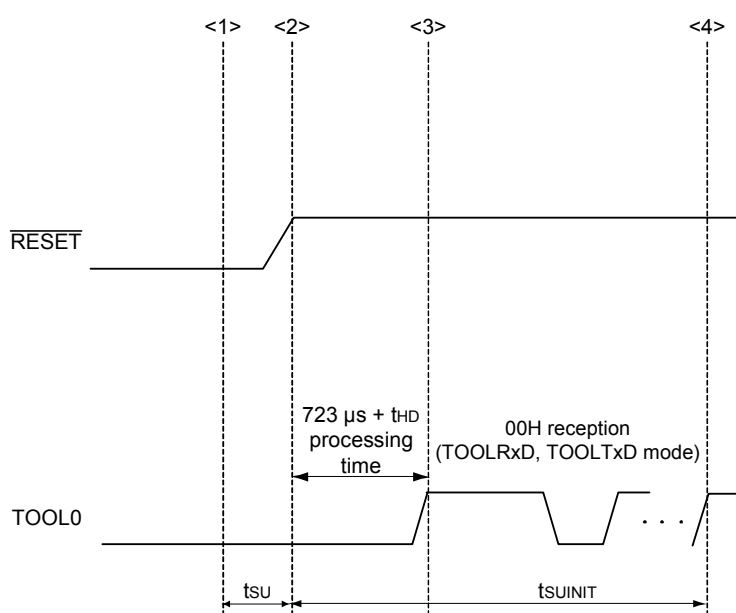
<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark   t$_{SUINIT}$:   The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

                t$_{SU}$:   How long from when the TOOL0 pin is placed at the low level until a pin reset ends

                t$_{HD}$:   How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4.7   52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3
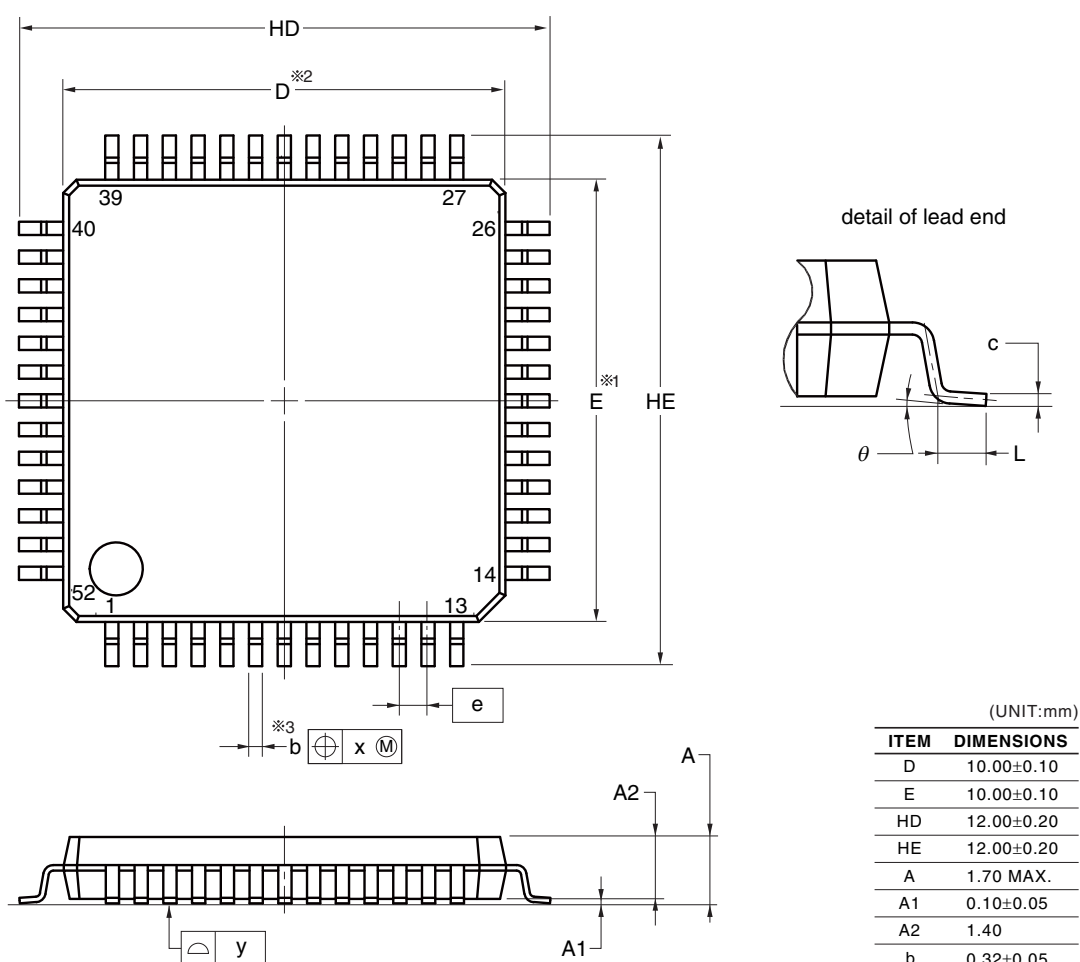
detail of lead end

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

(UNIT:mm)

NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

4.8   64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFA, R5F104LHAFA, R5F104LJAFA
R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFA, R5F104LHDFA, R5F104LJDFA
R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
R5F104LKAFA, R5F104LLAFA
R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of
its true position at maximum material condition.
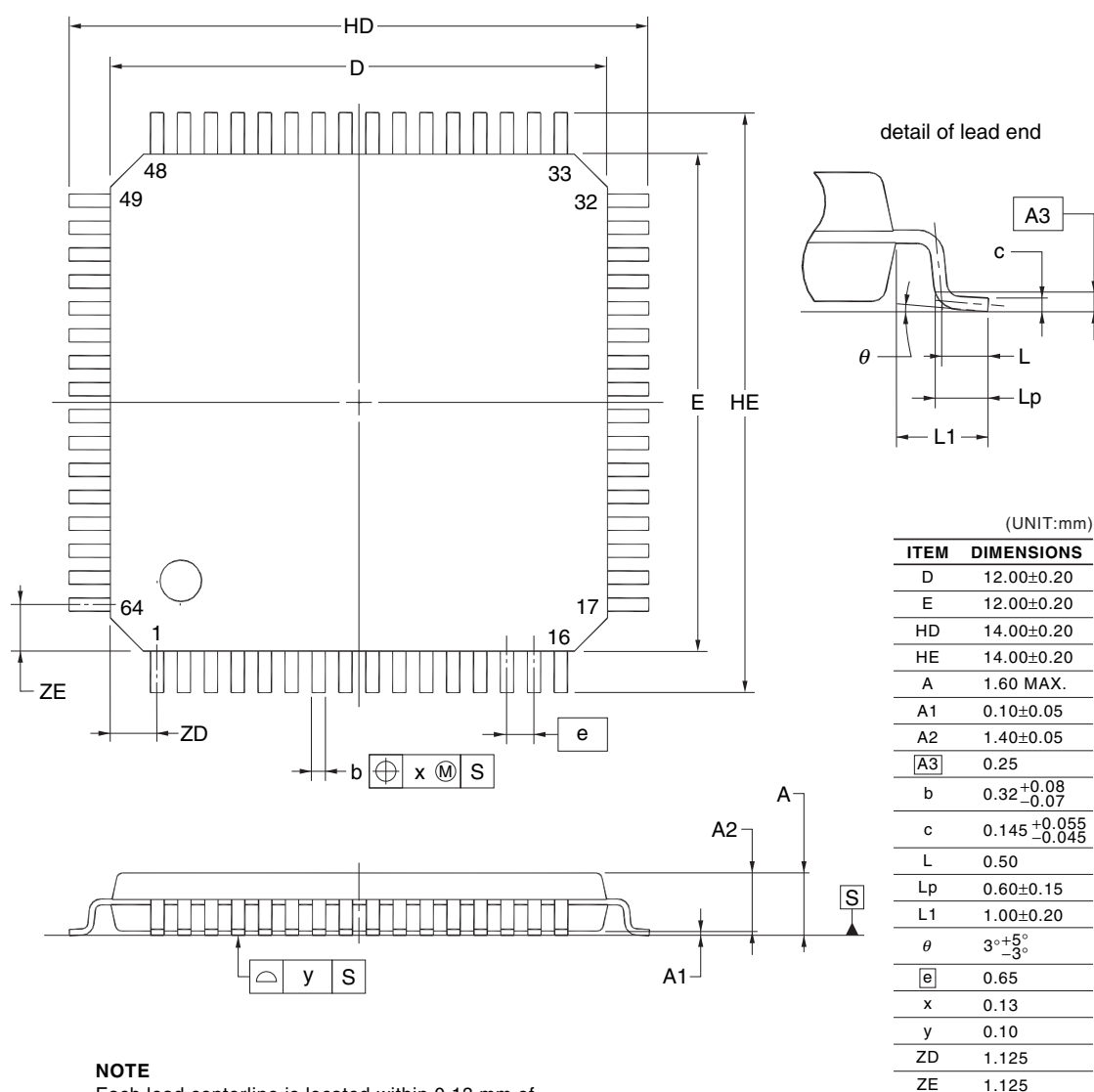
R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
R5F104LKALA, R5F104LLALA

R5F104LCGLA,R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
R5F104LKGLA, R5F104LLGLA

64-PIN PLASTIC FLGA (5x5)

DETAIL C

DETAIL D

DETAIL E

φ b
(LAND PAD)

φ0.34±0.03
(APERTURE OF
SOLDER RESIST)

0.70±0.03
0.55±0.04
0.75
0.55

R0.17±0.015
R0.125±0.02

0.55
0.75
0.55±0.04
0.70±0.03

R0.17±0.015
R0.125±0.02

0.70±0.03
0.55±0.04
0.75
0.55

0.55
0.75
0.55±0.04
0.70±0.03

R0.275±0.02

R0.35±0.015

(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5
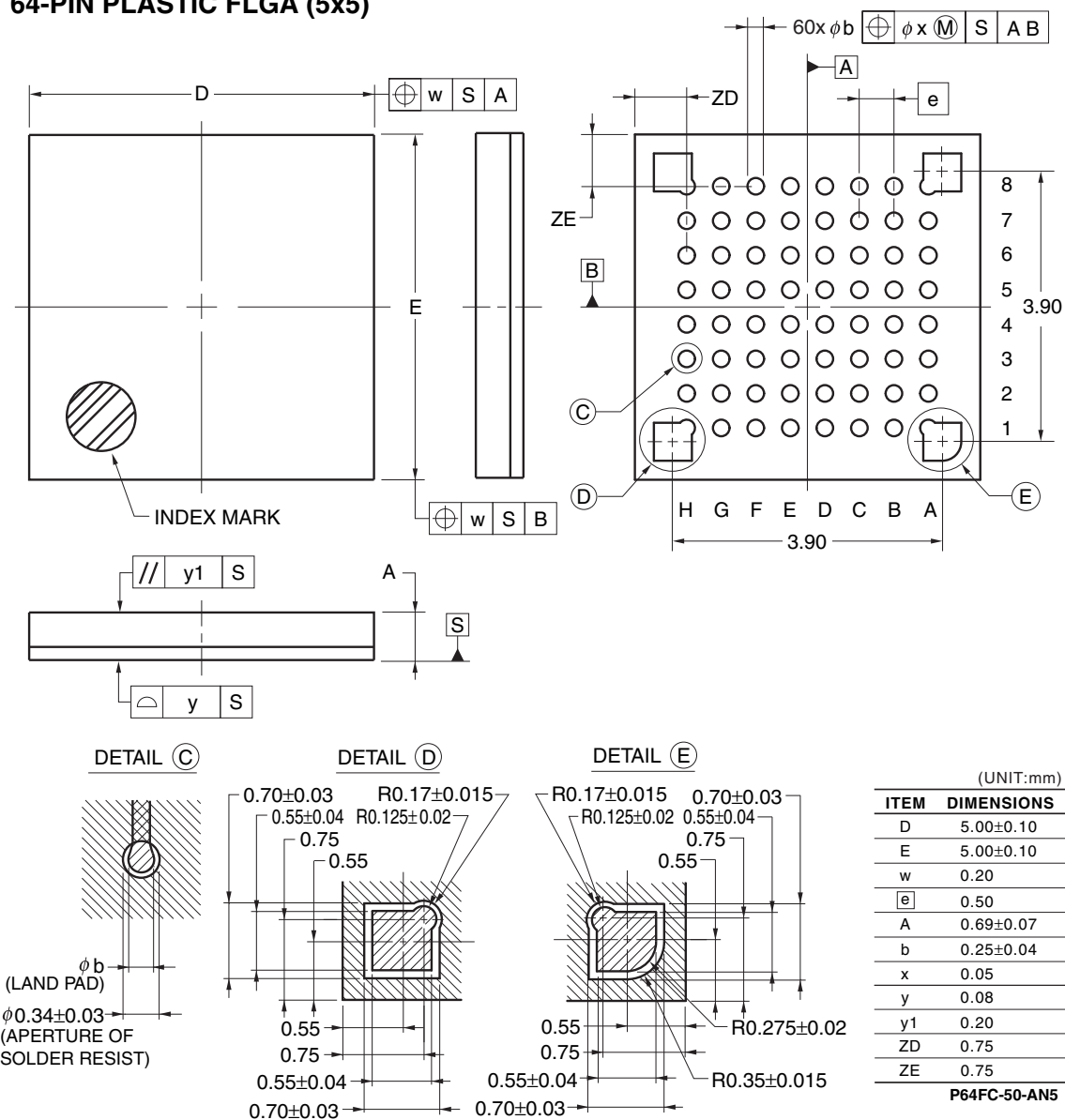
R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LFDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7
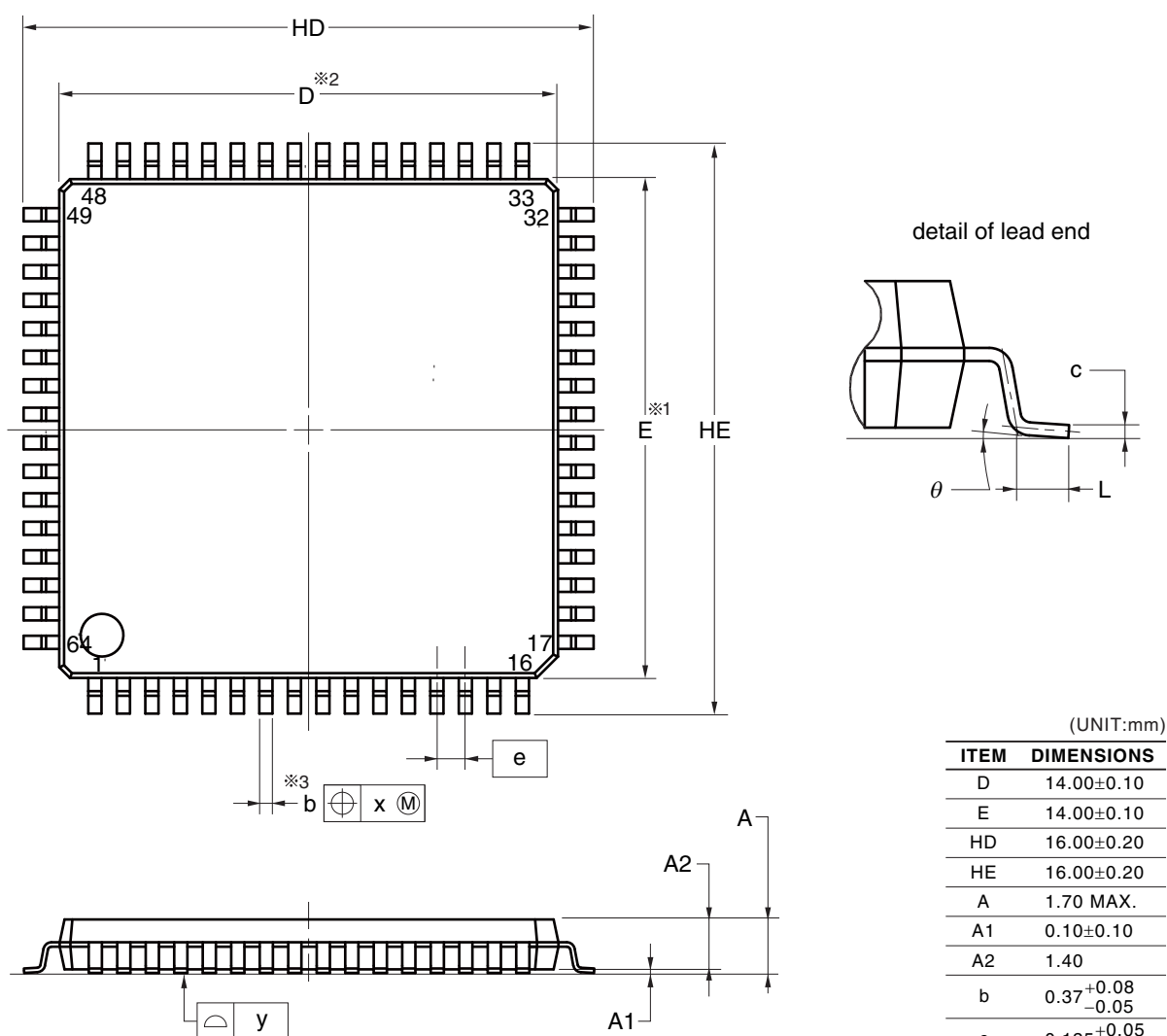
detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.10
E	14.00±0.10
HD	16.00±0.20
HE	16.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	$0.37^{+0.08}_{-0.05}$
c	$0.125^{+0.05}_{-0.02}$
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

REVISION HISTORY	RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Feb 10, 2011	—	First Edition issued
0.02	May 01, 2011	1 to 2	1.1 Features revised
		3	1.2 Ordering Information revised
		4 to 13	1.3 Pin Configuration (Top View) revised
		14	1.4 Pin Identification revised
		15 to 17	1.5.1 30-pin products to 1.5.3 36-pin products revised
		23 to 26	1.6 Outline of Functions revised
0.03	Jul 28, 2011	1	1.1 Features revised
1.00	Feb 21, 2012	1 to 40	1. OUTLINE revised
		41 to 97	2. ELECTRICAL SPECIFICATIONS added
2.00	Oct 25, 2013	1	Modification of 1.1 Features
		3 to 8	Modification of 1.2 Ordering Information
		9 to 22	Modification of package type in 1.3 Pin Configuration (Top View)
		34 to 43	Modification of description of subsystem clock in 1.6 Outline of Functions
		34 to 43	Modification of description of timer output in 1.6 Outline of Functions
		34 to 43	Modification of error of data transfer controller in 1.6 Outline of Functions
		34 to 43	Modification of error of event link controller in 1.6 Outline of Functions
		45, 46	Modification of description of Tables in 2.1 Absolute Maximum Ratings
		47	Modification of Tables, notes, cautions, and remarks in 2.2 Oscillator Characteristics
		48	Modification of error of conditions of high level input voltage in 2.3.1 Pin characteristics
		49	Modification of error of conditions of low level output voltage in 2.3.1 Pin characteristics
		53 to 62	Modification of Notes and Remarks in 2.3.2 Supply current characteristics
		65, 66	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		67 to 69	Addition of AC Timing Test Points
		70 to 97	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit
		98 to 101	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA
		102 to 105	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics
		107	Addition of characteristic in 2.6.4 Comparator
		107	Deletion of detection delay in 2.6.5 POR circuit characteristics
		109	Modification of 2.6.7 Power supply voltage rising slope characteristics
		110	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		110	Addition of characteristic in 2.8 Flash Memory Programming Characteristics
		111	Addition of description in 2.10 Timing for Switching Flash Memory Programming Modes

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