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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

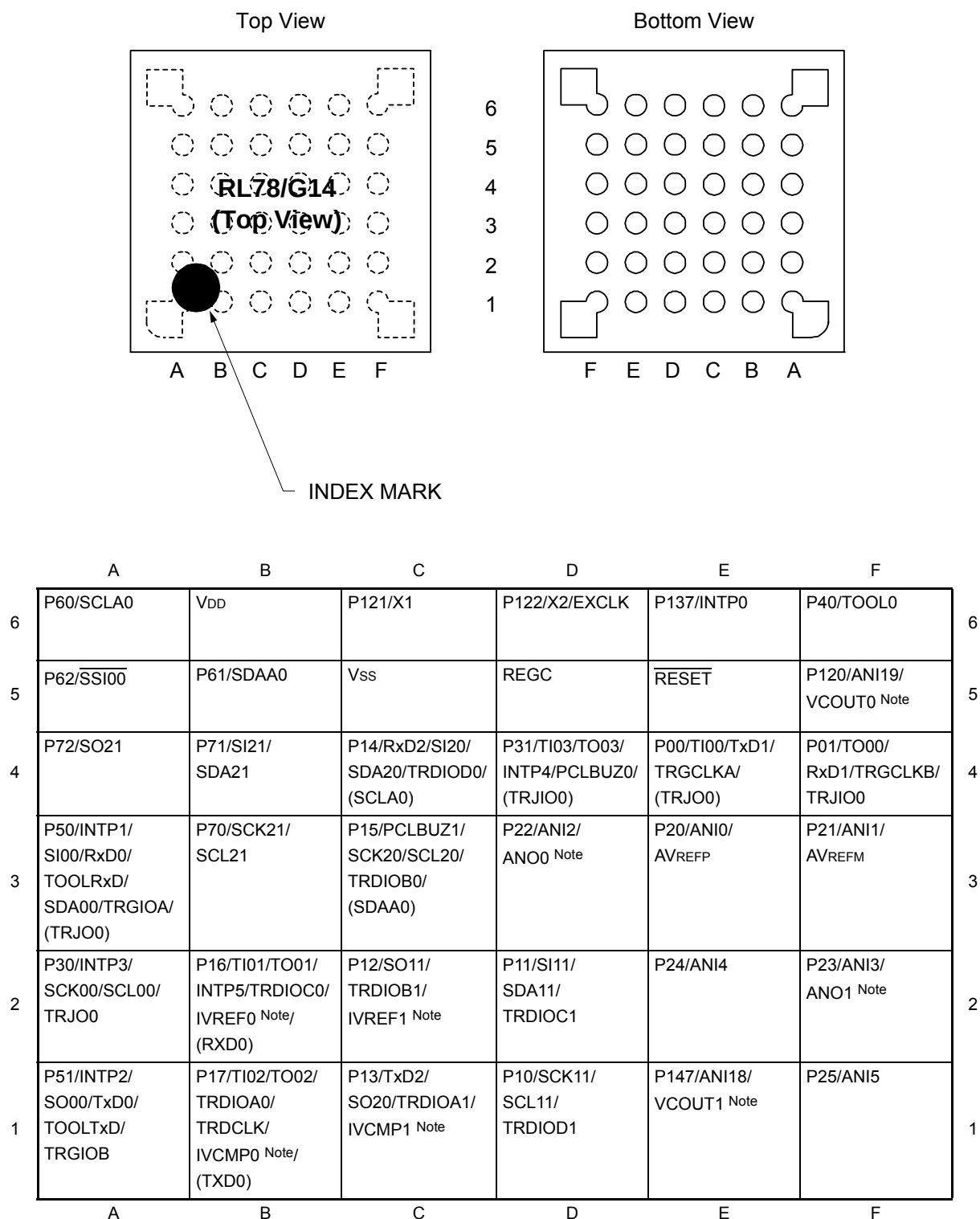
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104gadfb-x0

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

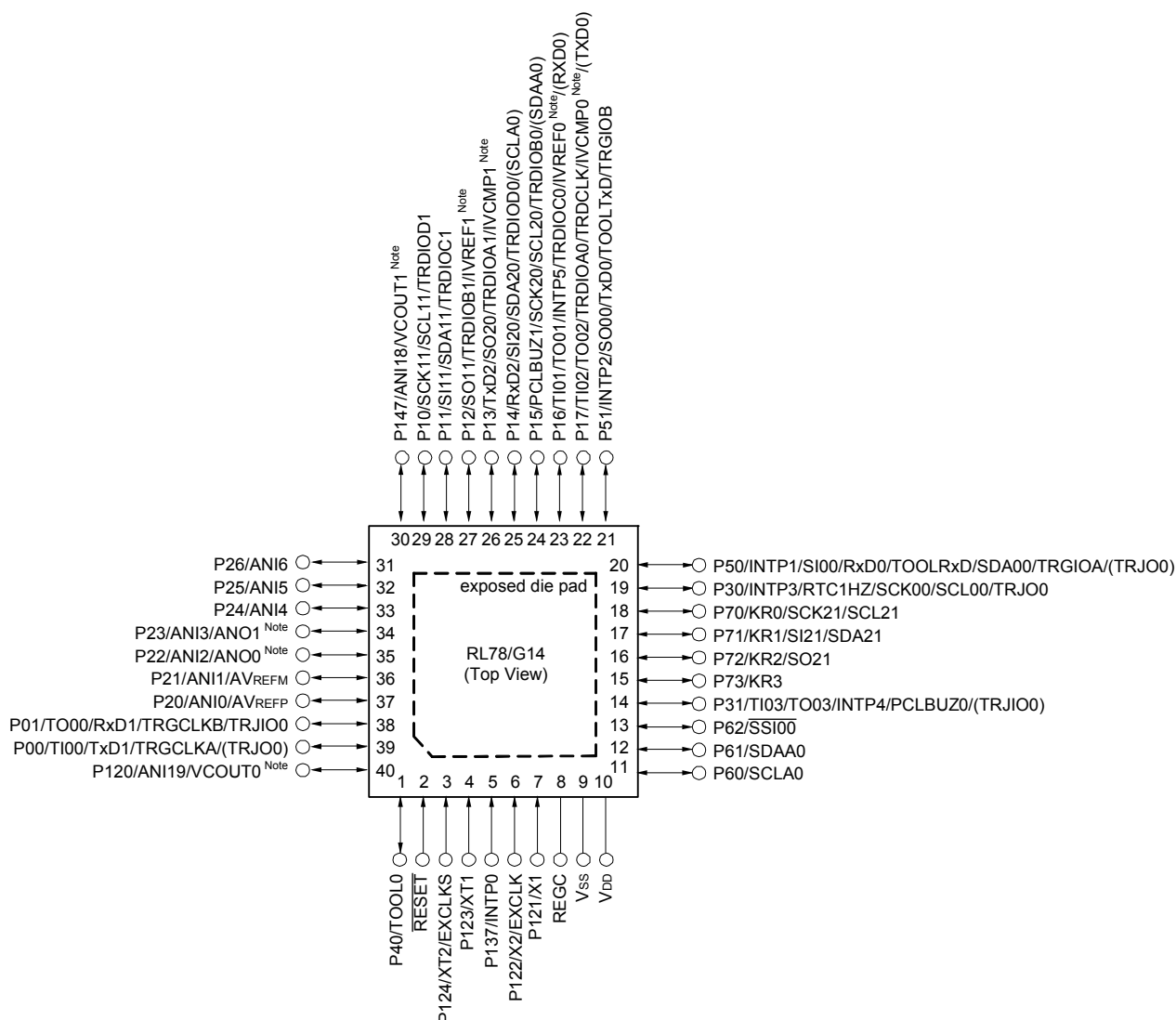
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

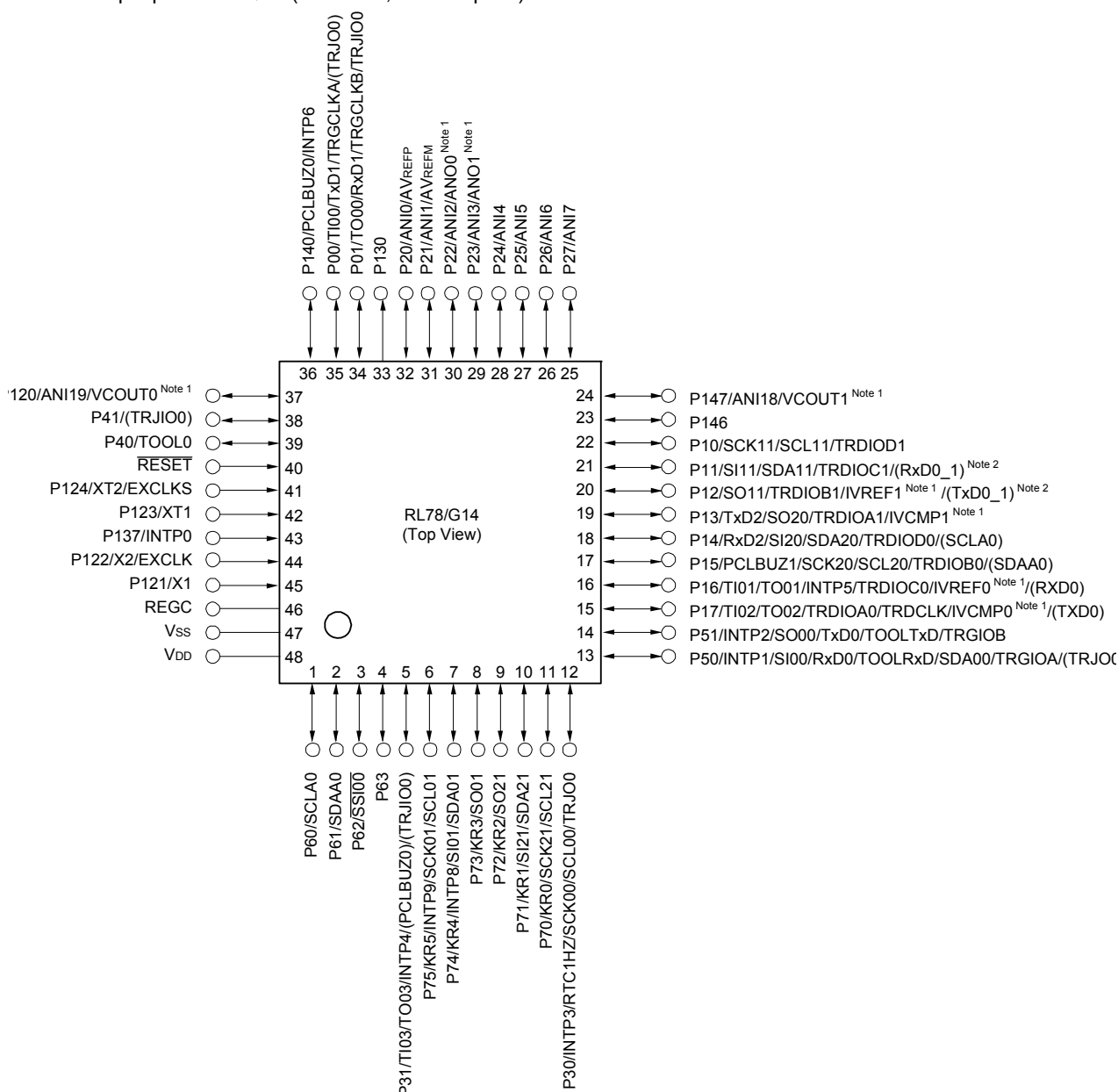
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to V_{SS}.

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

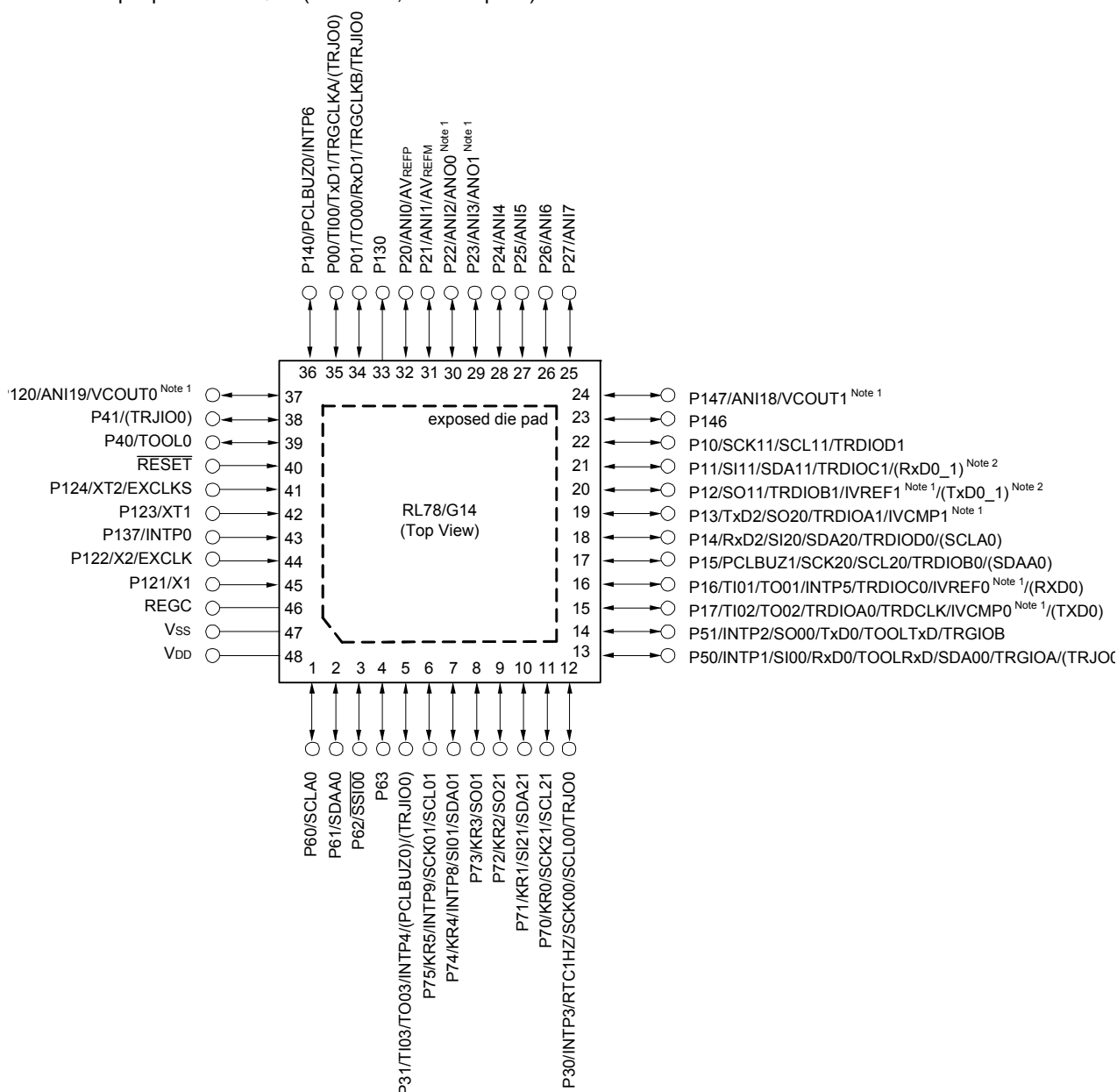
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

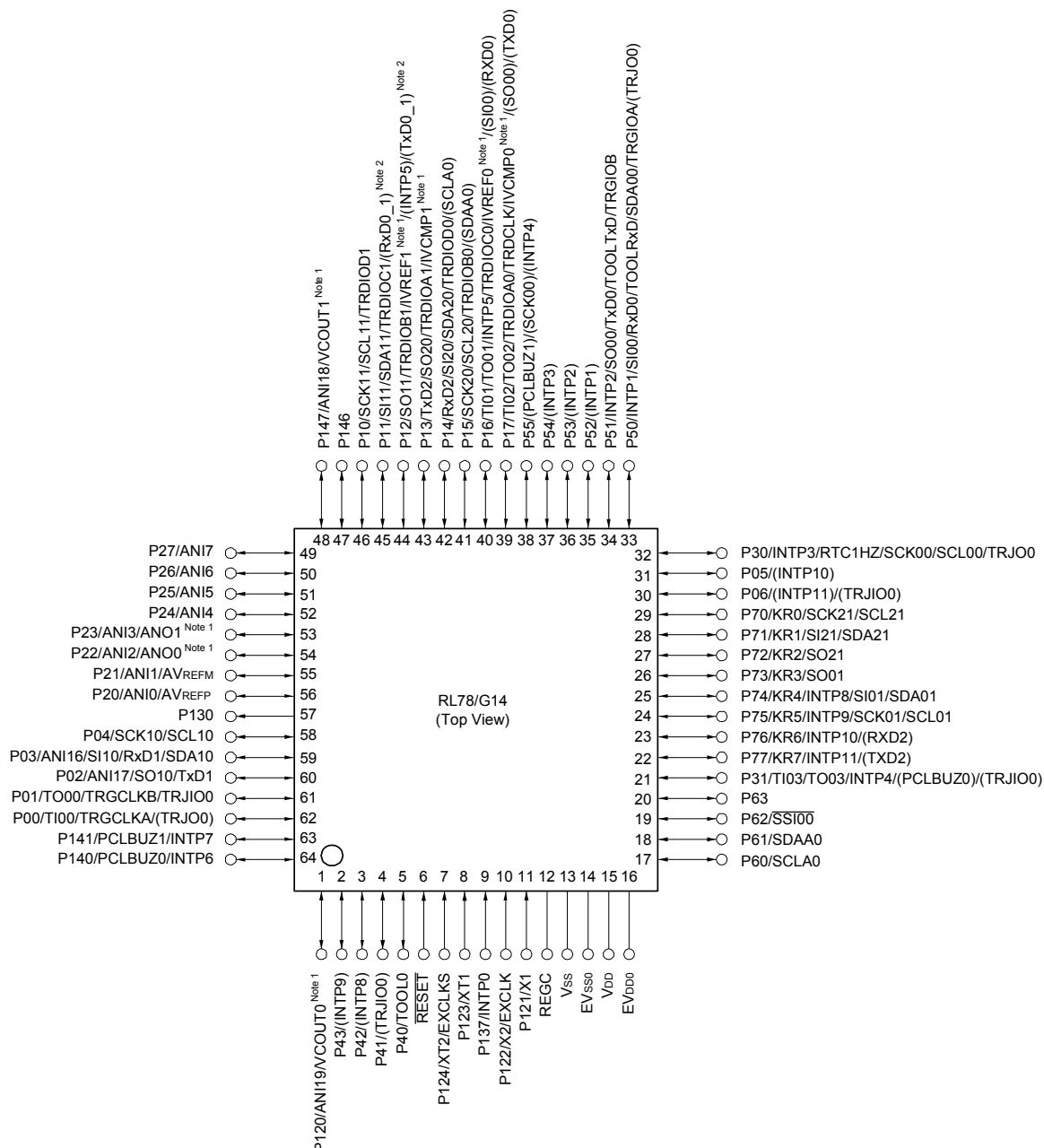
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

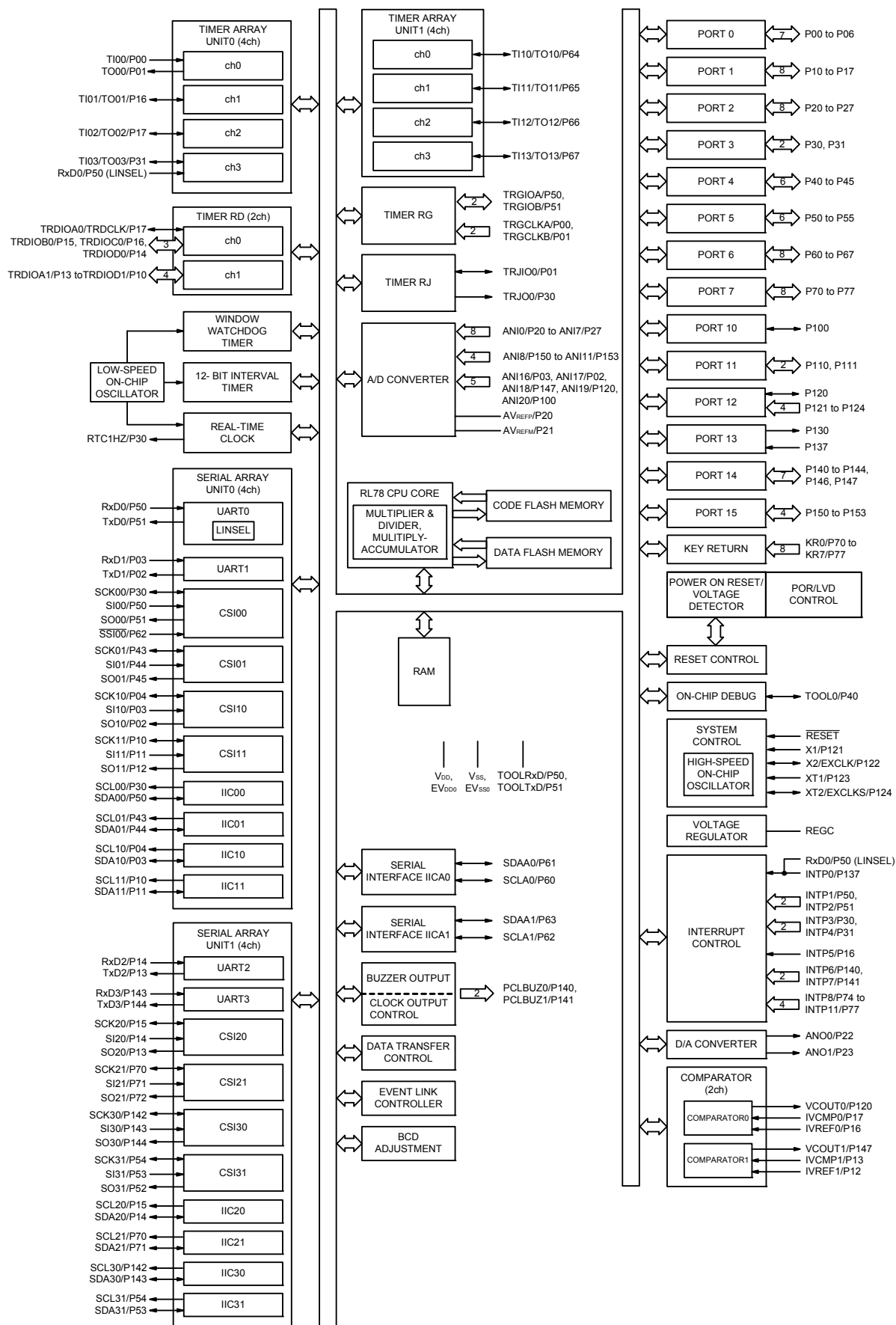
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.9 80-pin products



2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (fxT) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f _{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ VDD ≤ 5.5 V	-1.0		+1.0	%
			1.6 V ≤ VDD < 1.8 V	-5.0		+5.0	%
		-40 to -20°C	1.8 V ≤ VDD ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ VDD < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			150.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

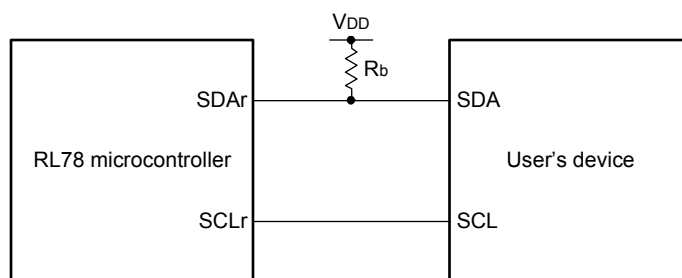
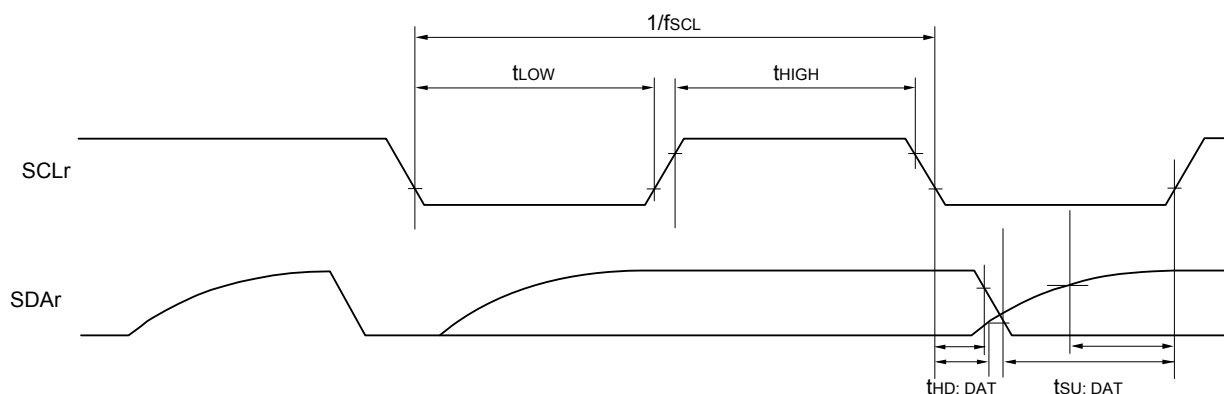
$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

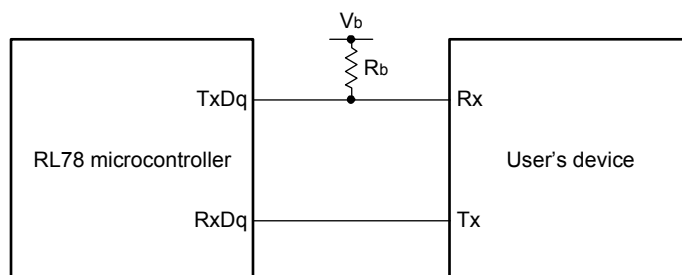
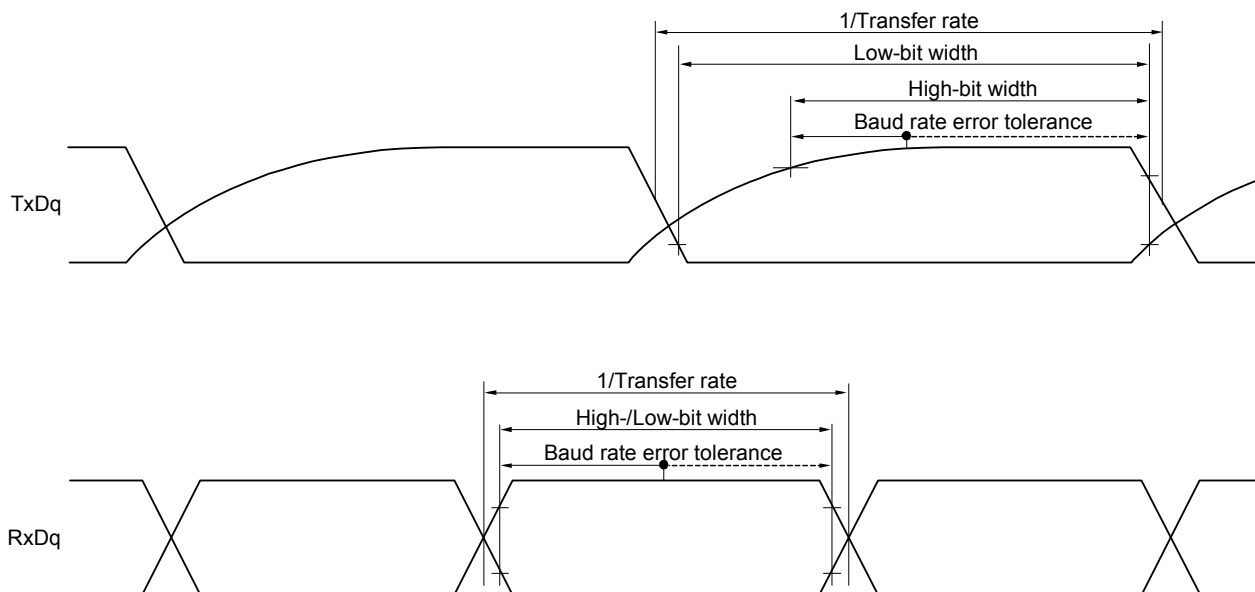
- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|-------------------------------------|
| HS (high-speed main) mode: | 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ VDD ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ VDD ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,

C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(2) I²C fast mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	tSU: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	tHD: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	tSU: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	tSU: STO	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Caution** The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ EVDD0 ≤ 5.5 V		-60.0	mA
	IOH2	Per pin for P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ VDD ≤ 5.5 V		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
 <Example> Where n = 80% and IOH = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			80.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA		EVDD0 - 0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA		EVDD0 - 0.6	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA		EVDD0 - 0.5	V
	VOH2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA		VDD - 0.5	V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
	VOL2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	250		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 24		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 36		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 76		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EVDD0 ≤ 5.5 V	66		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	66		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) Note 2	t _{SH1}		38		ns
Delay time from SCKp↓ to SOp output Note 3	t _{KS01}	C = 30 pF Note 4		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		reception		$f_{\text{MCK}}/12$ Note 1	bps
		4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ V _b $\leq$ 4.0 V			
		Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ V _b $\leq$ 2.7 V		$f_{\text{MCK}}/12$ Note 1	bps
		Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps
		2.4 V $\leq$ EVDD0 $<$ 3.3 V, 1.6 V $\leq$ V _b $\leq$ 2.0 V		$f_{\text{MCK}}/12$ Notes 1, 2	bps
		Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EVDD0 < VDD.2.4 V $\leq$ EVDD0 < 2.7 V: MAX. 1.3 Mbps**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 32 MHz (2.7 V $\leq$ VDD $\leq$ 5.5 V)16 MHz (2.4 V $\leq$ VDD $\leq$ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

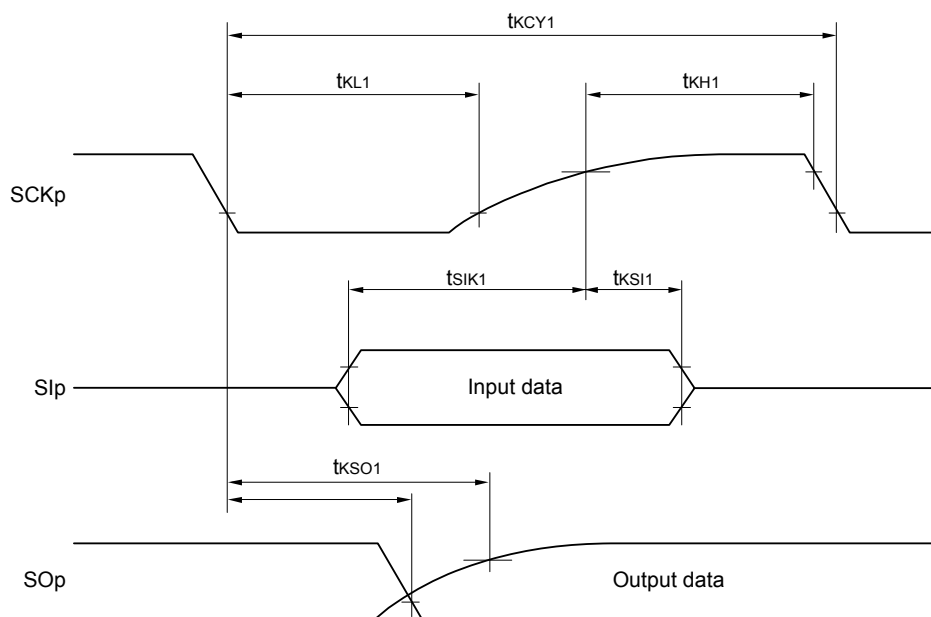
Remark 1. V_b [V]: Communication line voltage**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)**Remark 3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

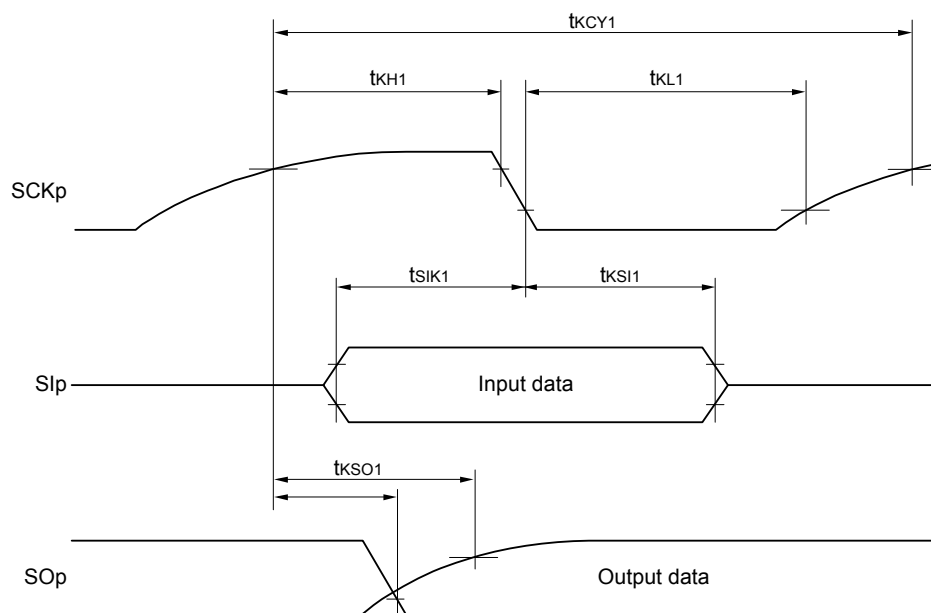
n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

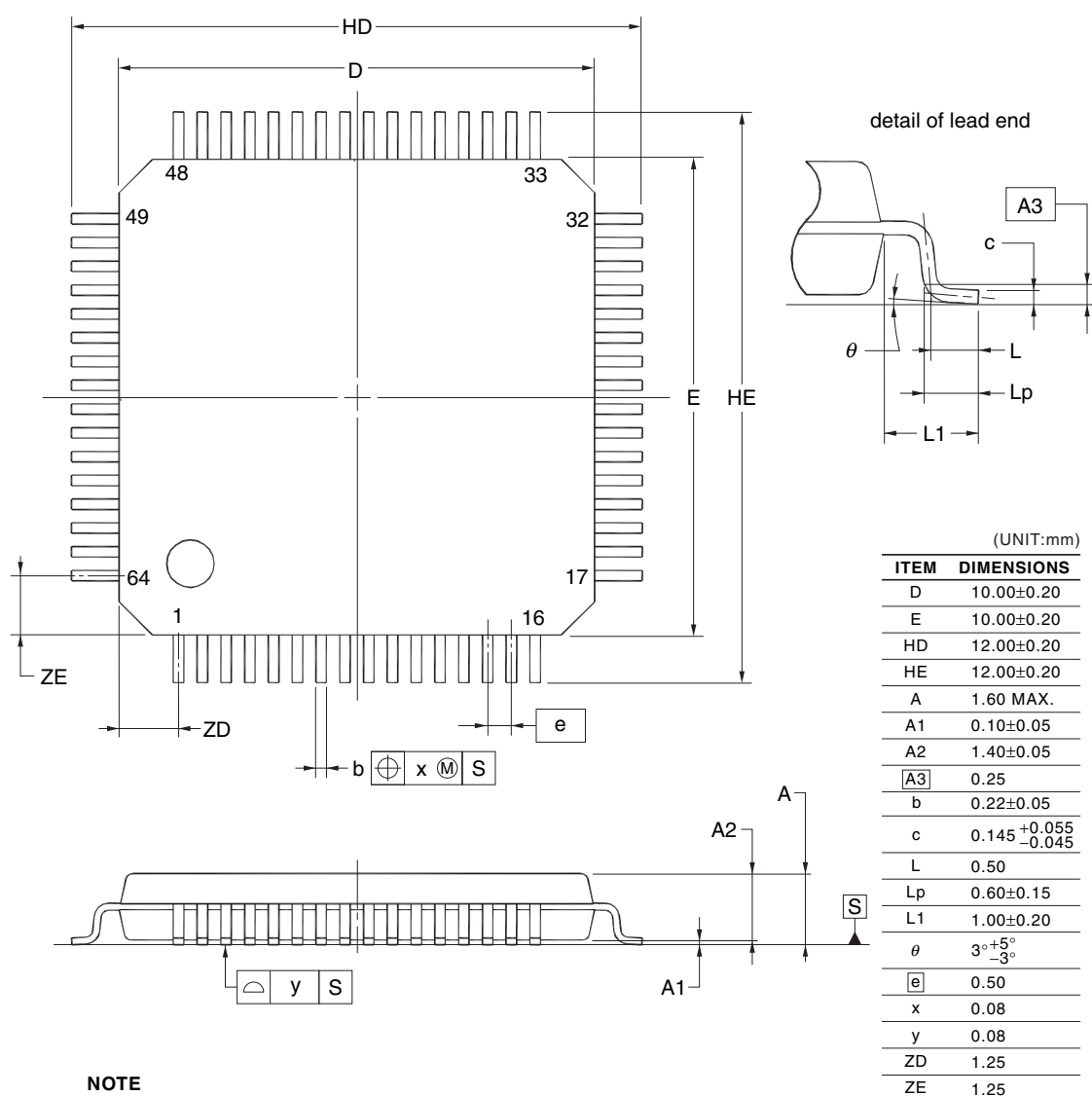


Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB,
 R5F104LJAFB
 R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB,
 R5F104LJDFB
 R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB,
 R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



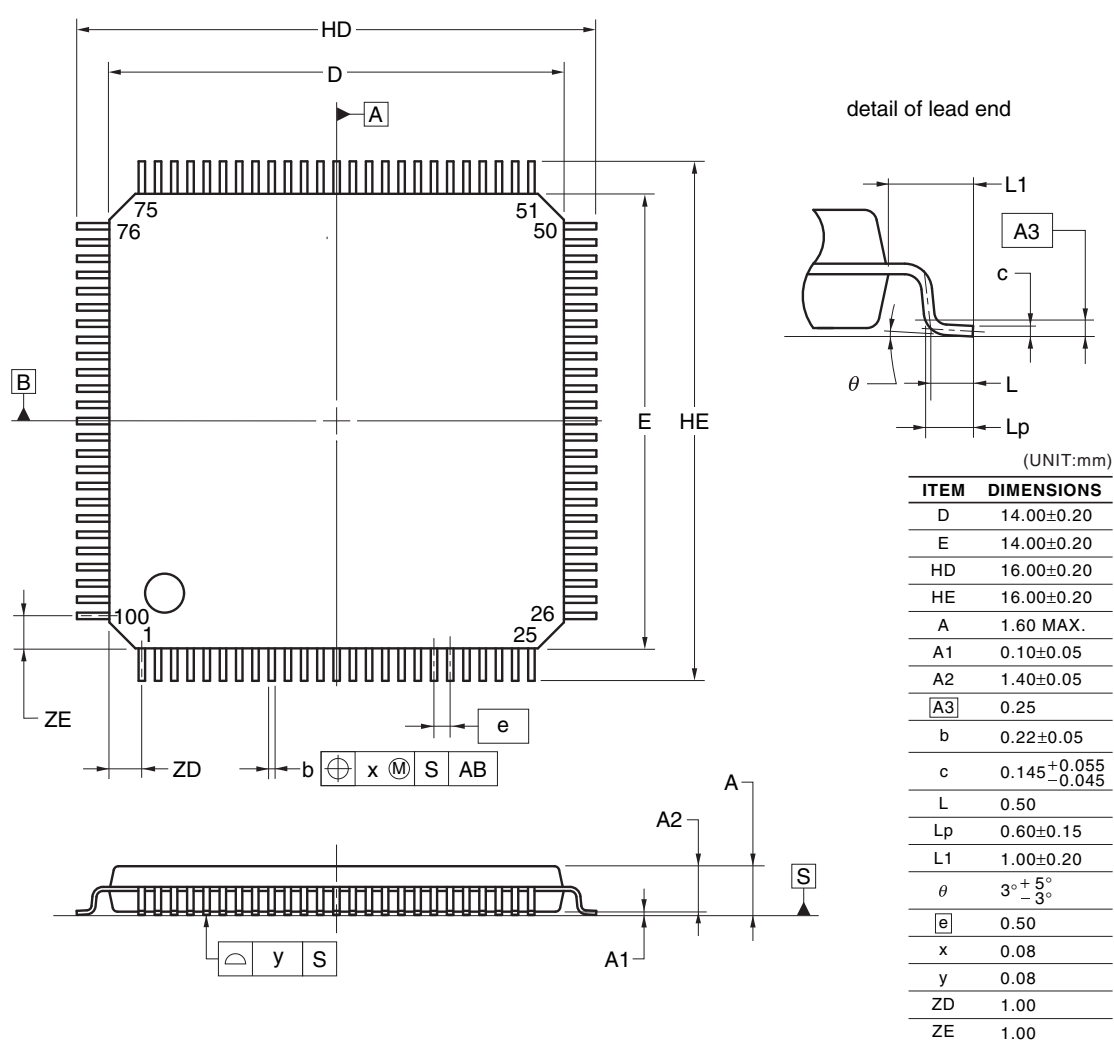
NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4.10 100-pin products

R5F104PFAFB, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB
 R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
 R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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