



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

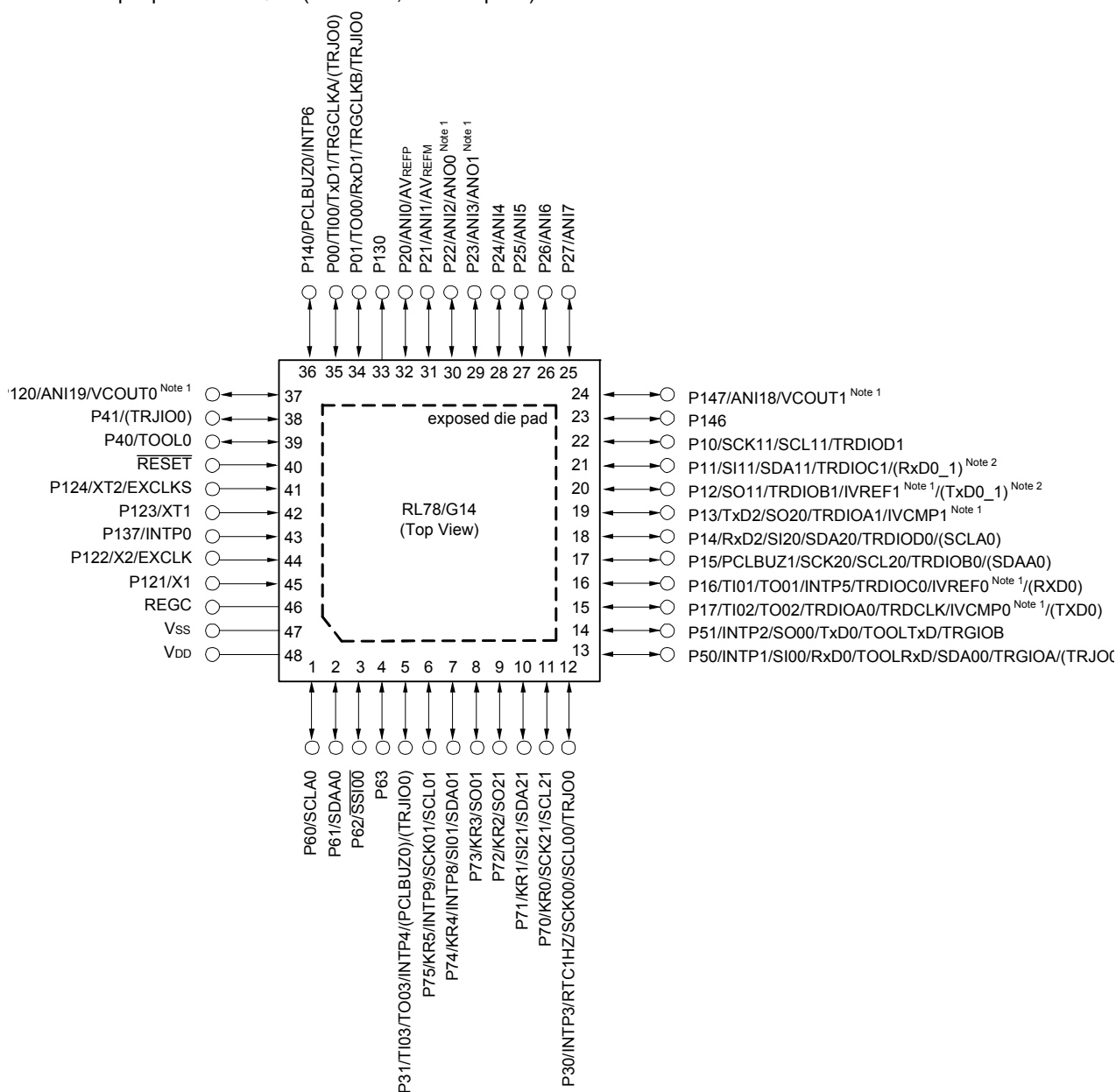
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104geafb-50">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104geafb-50</a>

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



**Note 1.** Mounted on the 96 KB or more code flash memory products.

**Note 2.** Mounted on the 384 KB or more code flash memory products.

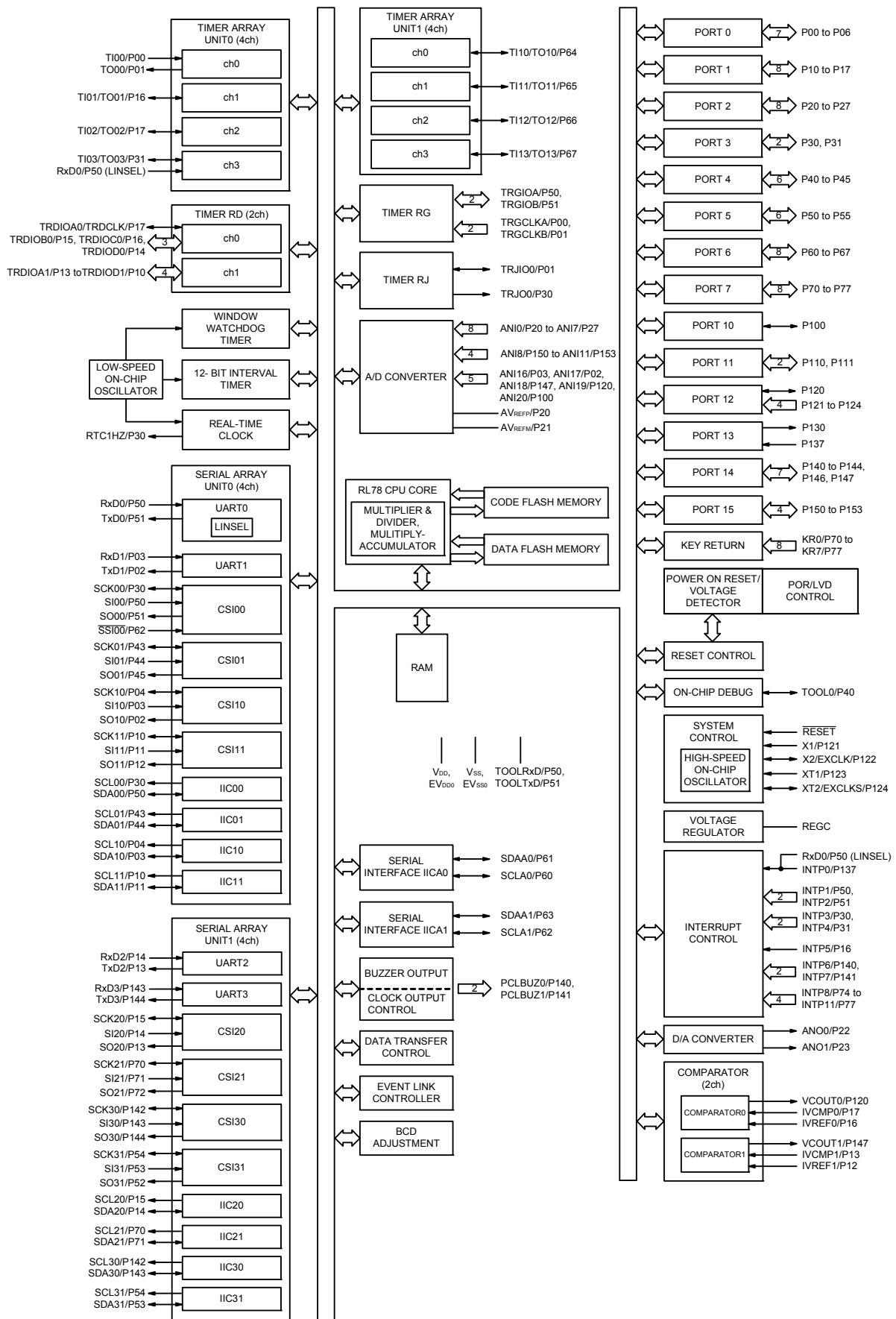
**Caution** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1  $\mu$ F).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

## 1.5.9 80-pin products



(2/2)

Item				
	44-pin R5F104Fx (x = F to H, J)	48-pin R5F104Gx (x = F to H, J)	52-pin R5F104Jx (x = F to H, J)	64-pin R5F104Lx (x = F to H, J)
Clock output/buzzer output	2 • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)			
8/10-bit resolution A/D converter	10 channels	10 channels	12 channels	12 channels
D/A converter	2 channels			
Comparator	2 channels			
Serial interface	[44-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels [48-pin, 52-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels			
I <sup>2</sup> C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)	31 sources	32 sources		33 sources
Event link controller (ELC)	Event input: 22 Event trigger output: 9			
Vectored interrupt sources	Internal	24	24	24
	External	7	10	13
Key interrupt	4	6	8	8
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit	• Power-on-reset: 1.51 ±0.04 V (T <sub>A</sub> = -40 to +85°C) 1.51 ±0.06 V (T <sub>A</sub> = -40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T <sub>A</sub> = -40 to +85°C) 1.50 ±0.06 V (T <sub>A</sub> = -40 to +105°C)			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)			
Operating ambient temperature	T <sub>A</sub> = -40 to +85°C (A: Consumer applications, D: Industrial applications), T <sub>A</sub> = -40 to +105°C (G: Industrial applications)			

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ( $V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ( $V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ( $V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ( $V_{DD} = 1.6$ to 5.5 V)	
	High-speed on-chip oscillator clock ( $f_{IH}$ )	HS (high-speed main) mode: 1 to 32 MHz ( $V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ( $V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ( $V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ( $V_{DD} = 1.6$ to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)	
Minimum instruction execution time		0.03125 $\mu$ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		0.05 $\mu$ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 $\mu$ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		<ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits <math>\times</math> 8 bits, 16 bits <math>\times</math> 16 bits), Division (16 bits <math>\div</math> 16 bits, 32 bits <math>\div</math> 32 bits)</li> <li>• Multiplication and Accumulation (16 bits <math>\times</math> 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li> </ul>	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	

**Note** In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

## 2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications TA = -40 to +85°C

R5F104xxAxx

D: Industrial applications TA = -40 to +85°C

R5F104xxDxx

G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C

R5F104xxGxx

**Caution 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

**Caution 2.** With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

**Caution 3.** The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			150.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ VDD ≤ 5.5 V		5.0	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.3.2 Supply current characteristics

#### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7		mA
						VDD = 3.0 V		5.1	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9		
						VDD = 3.0 V		4.0	6.9		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3		
						VDD = 3.0 V		3.8	6.3		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0		mA
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8		mA
						VDD = 2.0 V		1.3	1.8		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3		mA
						Resonator connection		3.4	5.5		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3		
						Resonator connection		3.4	5.5		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
			LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9		mA
						Resonator connection		1.2	2.0		
				fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9		
						Resonator connection		1.2	2.0		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)



- Note 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- |                             |   |
|-----------------------------|---|
| HS (high-speed main) mode:  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz |
|                             | 2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode:   | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz  |
| LV (low-voltage main) mode: | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz  |
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f<sub>HOCO</sub>: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f<sub>IH</sub>: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

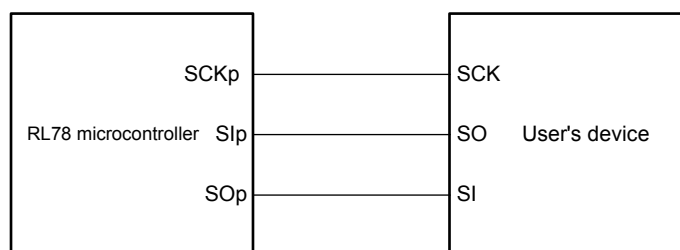
**Remark 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)****(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

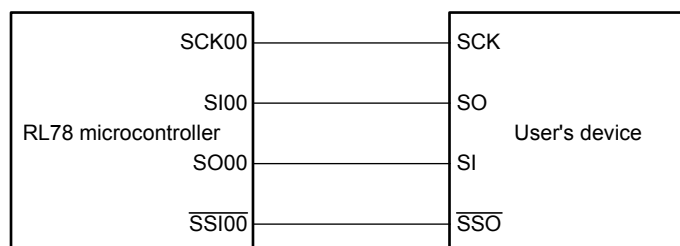
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SSI00 setup time	tSSIK	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
SSI00 hold time	tKSSI	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns

**Caution** Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**CSI mode connection diagram (during communication at same potential)**

**CSI mode connection diagram (during communication at same potential)**  
**(Slave Transmission of slave select input function (CSI00))**



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(2) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target pin: ANI16 to ANI20

(TA = -40 to +85°C,  $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	$\pm 5.0$	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	$\pm 8.5$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	$\mu\text{s}$
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	$\mu\text{s}$
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	$\mu\text{s}$
Zero-scale error Notes 1, 2	$E_{ZS}$	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 0.35$	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		$\pm 0.60$	%FSR
Full-scale error Notes 1, 2	$E_{FS}$	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 0.35$	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		$\pm 0.60$	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 3.5$	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		$\pm 6.0$	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 2.0$	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		$\pm 2.5$	LSB
Analog input voltage	$V_{AIN}$	ANI16 to ANI20	0		$AV_{REFP}$ and $EV_{DD0}$	V

**Note 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When  $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 1.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Zero-scale error/Full-scale error: Add  $\pm 0.05\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Integral linearity error/ Differential linearity error: Add  $\pm 0.5$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

**Note 4.** When  $AV_{REFP} < EV_{DD0} \leq V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 4.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Zero-scale error/Full-scale error: Add  $\pm 0.20\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Integral linearity error/ Differential linearity error: Add  $\pm 2.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

**Note 5.** When the conversion time is set to 57  $\mu\text{s}$  (min.) and 95  $\mu\text{s}$  (max.).

**Absolute Maximum Ratings****(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +105
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0.8 EVDD0		EVDD0	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2	EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0	EVDD0	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	1.5	EVDD0	V
	V <sub>IH3</sub>	P20 to P27, P150 to P156	0.7 VDD		VDD	V
	V <sub>IH4</sub>	P60 to P63	0.7 EVDD0		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8 VDD		VDD	V
Input voltage, low	V <sub>IL1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0		0.2 EVDD0	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	0	0.32	V
	V <sub>IL3</sub>	P20 to P27, P150 to P156	0		0.3 VDD	V
	V <sub>IL4</sub>	P60 to P63	0		0.3 EVDD0	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2 VDD	V

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>WDT</sub> when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub> or I<sub>DD2</sub> and I<sub>ADC</sub> when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>LVD</sub> when the LVD circuit is in operation.
- Note 8.** Current flowing during programming of the data flash.
- Note 9.** Current flowing during self-programming.
- Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.
- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub> or I<sub>DD2</sub> and I<sub>DAC</sub> when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub>, or I<sub>DD3</sub> and I<sub>CMP</sub> when the comparator circuit is in operation.
- Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency

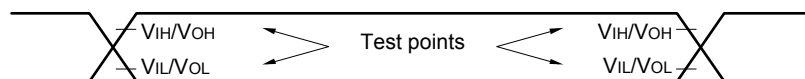
**Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is T<sub>A</sub> = 25°C

### 3.5 Peripheral Functions Characteristics

#### AC Timing Test Points



#### 3.5.1 Serial array unit

##### (1) During communication at same potential (UART mode)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq 5.5\text{ V}$ ,  $V_{SS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$f_{\text{MCK}}/12$ Note 2	bps
		Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when  $\text{FRQSEL4} = 1$ .

**Note 2.** The following conditions are required for low voltage interface when  $\text{EVDD0} < V_{DD}$ .

$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$ : MAX. 1.3 Mbps

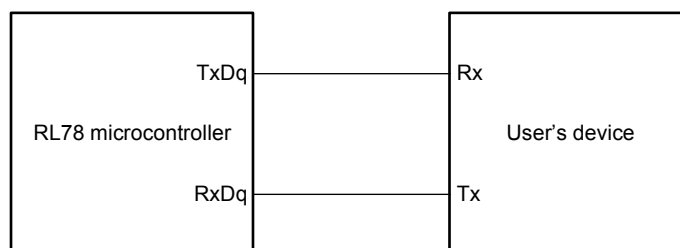
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ( $f_{\text{CLK}}$ ) are:

HS (high-speed main) mode: 32 MHz ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

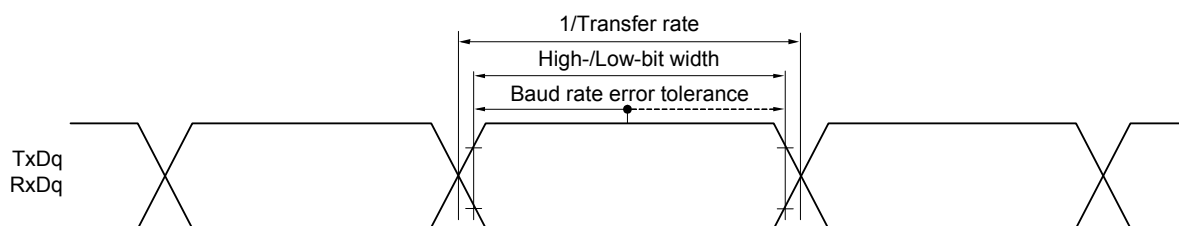
16 MHz ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

#### UART mode connection diagram (during communication at same potential)



#### UART mode bit width (during communication at same potential) (reference)



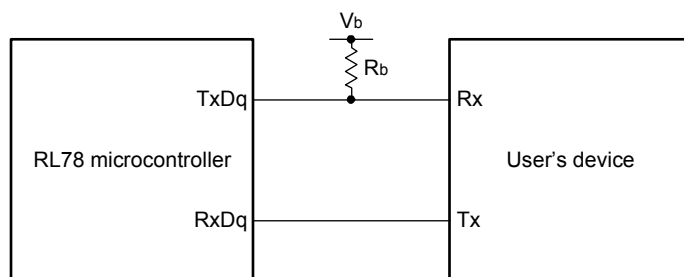
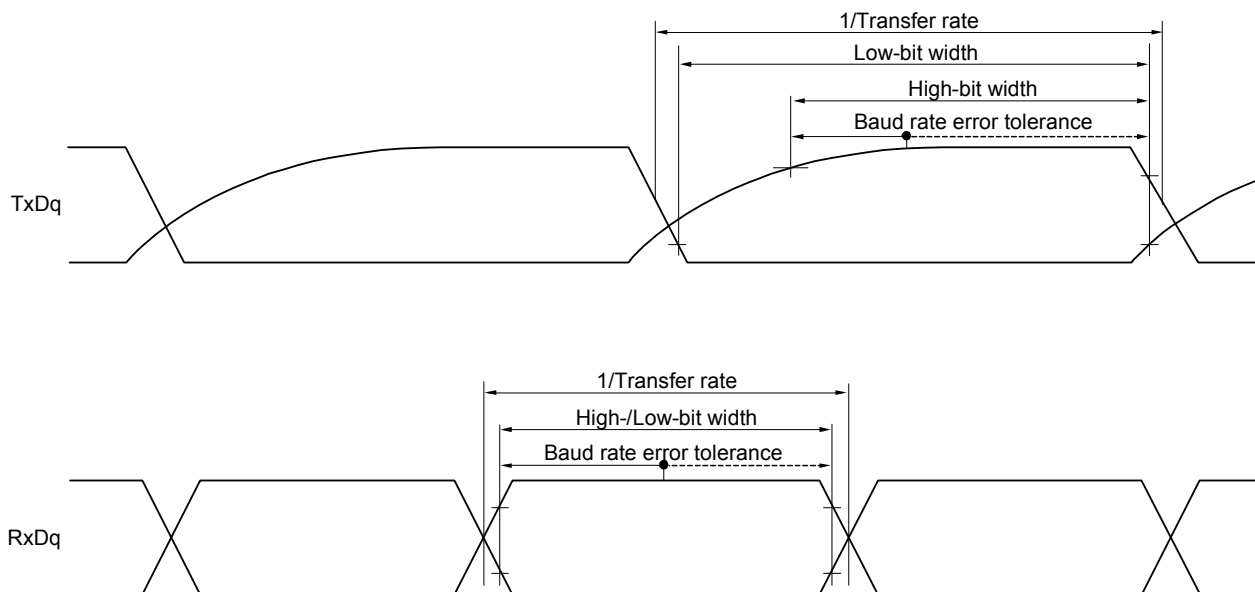
**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 2.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))



**UART mode connection diagram (during communication at different potential)****UART mode bit width (during communication at different potential) (reference)**

**Remark 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,

$C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(2) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target pin: ANI16 to ANI20

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,

$V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	$\pm 5.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error Notes 1, 2	$E_{ZS}$	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Full-scale error Notes 1, 2	$E_{FS}$	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 3.5$	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI16 to ANI20		0		$AV_{REFP}$ and $EV_{DD0}$	V

**Note 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When  $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 1.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
 Zero-scale error/Full-scale error: Add  $\pm 0.05\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
 Integral linearity error/ Differential linearity error: Add  $\pm 0.5$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

**Note 4.** When  $AV_{REFP} < EV_{DD0} \leq V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 4.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
 Zero-scale error/Full-scale error: Add  $\pm 0.20\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
 Integral linearity error/ Differential linearity error: Add  $\pm 2.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

### 3.6.6 LVD circuit characteristics

#### (1) Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

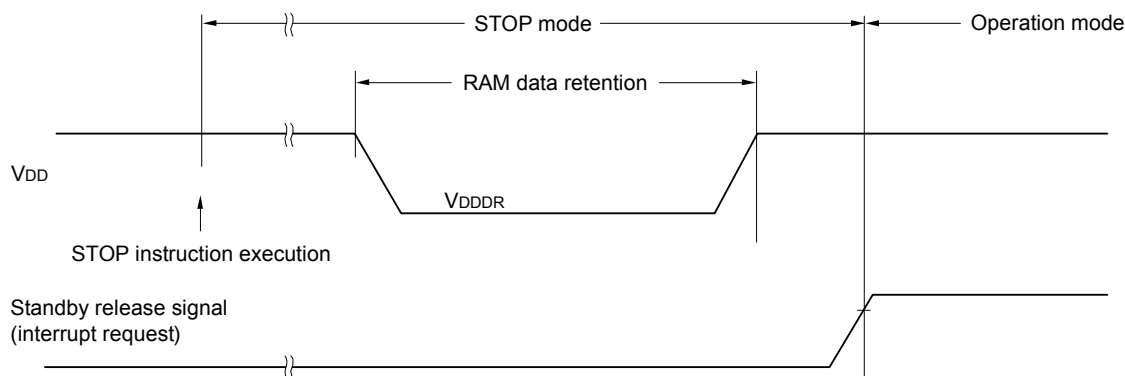
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.90	4.06	4.22	V
			Falling edge	3.83	3.98	4.13	V
		VLVD1	Rising edge	3.60	3.75	3.90	V
			Falling edge	3.53	3.67	3.81	V
		VLVD2	Rising edge	3.01	3.13	3.25	V
			Falling edge	2.94	3.06	3.18	V
		VLVD3	Rising edge	2.90	3.02	3.14	V
			Falling edge	2.85	2.96	3.07	V
		VLVD4	Rising edge	2.81	2.92	3.03	V
			Falling edge	2.75	2.86	2.97	V
		VLVD5	Rising edge	2.70	2.81	2.92	V
			Falling edge	2.64	2.75	2.86	V
		VLVD6	Rising edge	2.61	2.71	2.81	V
			Falling edge	2.55	2.65	2.75	V
		VLVD7	Rising edge	2.51	2.61	2.71	V
			Falling edge	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

### 3.7 RAM Data Retention Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.44 Note		5.5	V

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



### 3.8 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C <sub>erwr</sub>	Retained for 20 years T <sub>A</sub> = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T <sub>A</sub> = 25°C		1,000,000		
		Retained for 5 years T <sub>A</sub> = 85°C Note 4	100,000			
		Retained for 20 years T <sub>A</sub> = 85°C Note 4	10,000			

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**Note 4.** This temperature is the average value at which data are retained.

### 3.9 Dedicated Flash Memory Programmer Communication (UART)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} = V_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = V_{SS0} = V_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

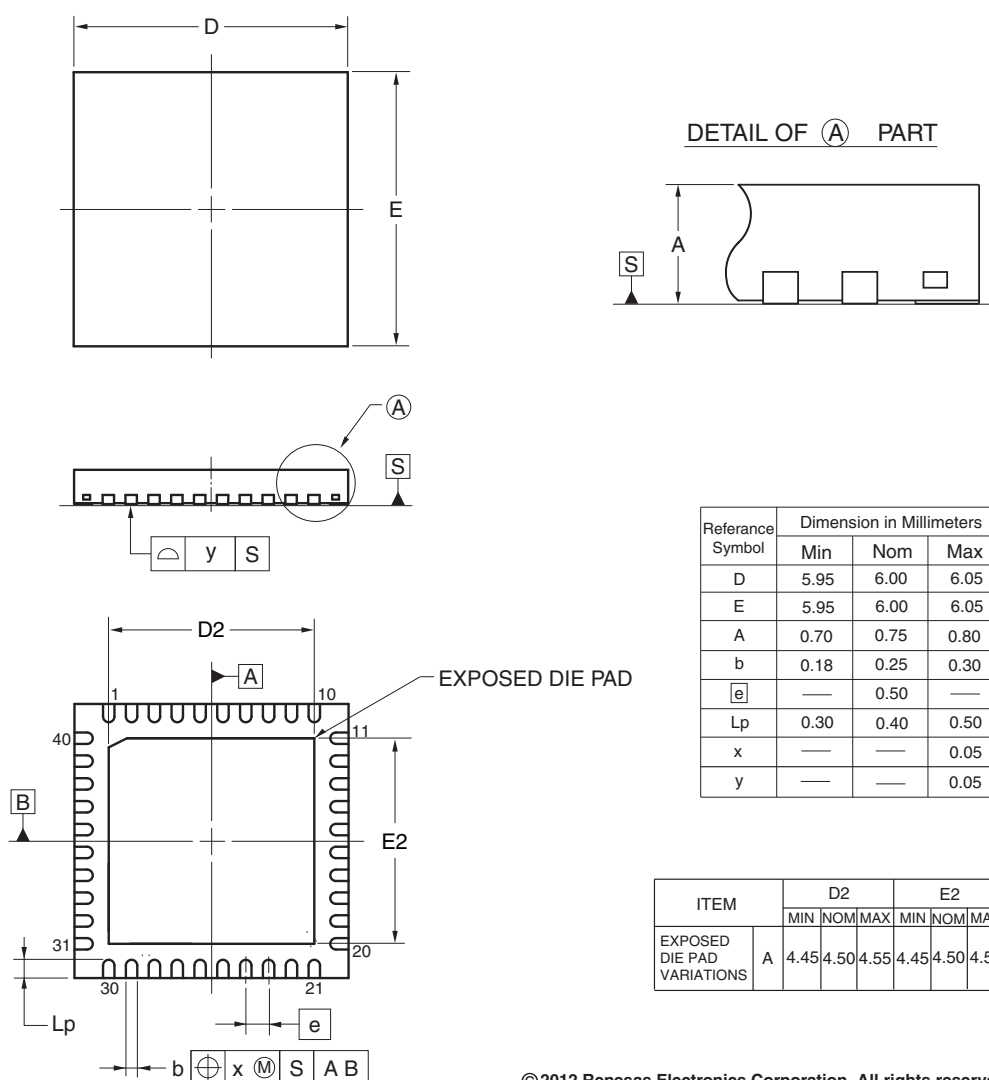
#### 4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA

R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA

R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA, R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



©2012 Renesas Electronics Corporation. All rights reserved.