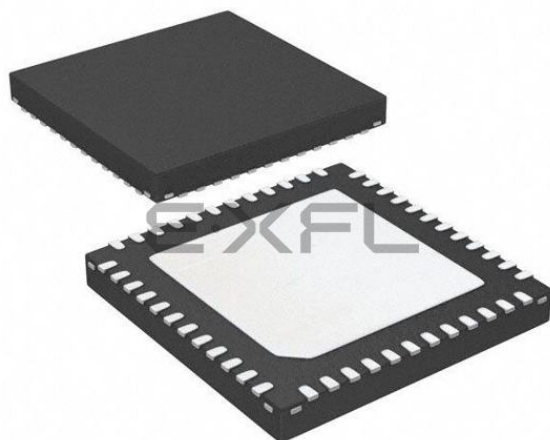




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104geana-u0

(4/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAF#V0, R5F104LHAF#V0, R5F104LJAF#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAF#X0, R5F104LHAF#X0, R5F104LJAF#X0 R5F104LKAF#30, R5F104LLAF#30 R5F104LKAF#50, R5F104LLAF#50
		D	R5F104LCDF#V0, R5F104LDDF#V0, R5F104LEDF#V0, R5F104LDFD#V0, R5F104LGDF#V0, R5F104LHDF#V0, R5F104LJDF#V0 R5F104LCDF#X0, R5F104LDDF#X0, R5F104LEDF#X0, R5F104LDFD#X0, R5F104LGDF#X0, R5F104LHDF#X0, R5F104LJDF#X0
		G	R5F104LCGF#V0, R5F104LDGF#V0, R5F104LEGF#V0, R5F104LFGF#V0, R5F104LGGF#V0, R5F104LHGF#V0, R5F104LJGF#V0 R5F104LCGF#X0, R5F104LDGF#X0, R5F104LEGF#X0, R5F104LFGF#X0, R5F104LGGF#X0, R5F104LHGF#X0, R5F104LJGF#X0 R5F104LKGf#30, R5F104LLGF#30 R5F104LKGf#50, R5F104LLGF#50
	64-pin plastic LQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LDFDB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LDFDB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCA#U0, R5F104LDA#U0, R5F104LEA#U0, R5F104LFA#U0, R5F104LGA#U0, R5F104LHA#U0, R5F104LJA#U0 R5F104LCA#W0, R5F104LDA#W0, R5F104LEA#W0, R5F104LFA#W0, R5F104LGA#W0, R5F104LHA#W0, R5F104LJA#W0 R5F104LKA#U0, R5F104LLA#U0 R5F104LKA#W0, R5F104LLA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFLGA#U0, R5F104LGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFLGA#W0, R5F104LGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LDFDP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LDFDP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

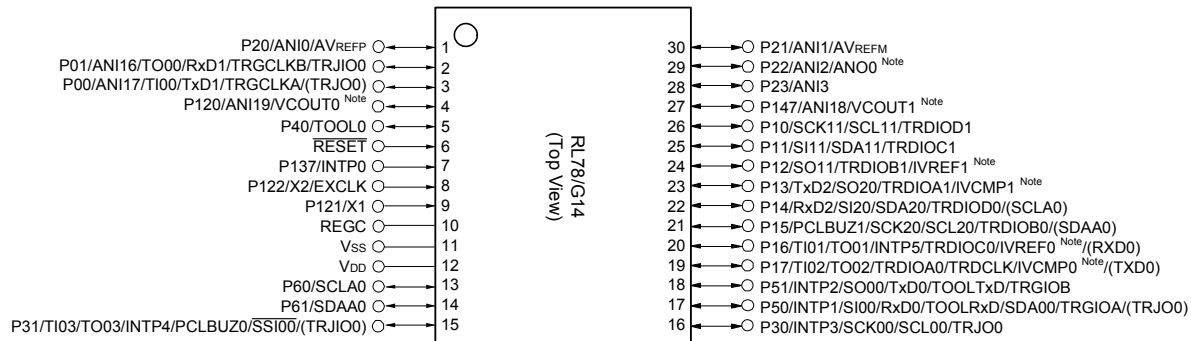
Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	16 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)

(Note is listed on the next page.)

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2	EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0	EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5	EVDD0	V
	VIH3	P20 to P27, P150 to P156	0.7 VDD		VDD	V
	VIH4	P60 to P63	0.7 EVDD0		6.0	V
	VIH5	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0		0.2 EVDD0	V
	VIL2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0	0.32	V
	VIL3	P20 to P27, P150 to P156	0		0.3 VDD	V
	VIL4	P60 to P63	0		0.3 EVDD0	V
	VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2 VDD	V

Caution The maximum value of VIH of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7		mA
						VDD = 3.0 V		5.1	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9		
						VDD = 3.0 V		4.0	6.9		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3		
						VDD = 3.0 V		3.8	6.3		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0		mA
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8		mA
						VDD = 2.0 V		1.3	1.8		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3		mA
						Resonator connection		3.4	5.5		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3		
						Resonator connection		3.4	5.5		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
			LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9		mA
						Resonator connection		1.2	2.0		
				fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9		
						Resonator connection		1.2	2.0		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|-------------------------------------|
| HS (high-speed main) mode: | 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ VDD ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ VDD ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.25		1	μs
		Subsystem clock (fSUB) operation		1.8 V ≤ VDD ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.25		1	μs
External system clock frequency	fex	2.7 V ≤ VDD ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ VDD ≤ 2.7 V			1.0		16.0	MHz
		1.8 V ≤ VDD < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ VDD < 1.8 V			1.0		4.0	MHz
	fexs				32		35	kHz
External system clock input high-level width, low-level width	texH, texL	2.7 V ≤ VDD ≤ 5.5 V			24			ns
		2.4 V ≤ VDD ≤ 2.7 V			30			ns
		1.8 V ≤ VDD < 2.4 V			60			ns
		1.6 V ≤ VDD < 1.8 V			120			ns
	texHS, texLS				13.7			μs
Ti00 to Ti03, Ti10 to Ti13 input high-level width, low-level width	ttrH, ttrL				1/fMCK + 10 Note			ns
Timer RJ input cycle	fc	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	100			ns
				1.8 V ≤ EVDD0 < 2.7 V	300			ns
				1.6 V ≤ EVDD0 < 1.8 V	500			ns
Timer RJ input high-level width, low-level width	trjIH, trjIL	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	40			ns
				1.8 V ≤ EVDD0 < 2.7 V	120			ns
				1.6 V ≤ EVDD0 < 1.8 V	200			ns

Note The following conditions are required for low voltage interface when EVDD0 < VDD

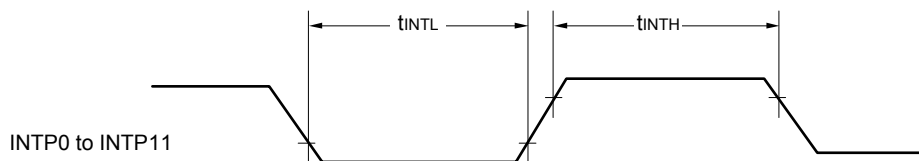
1.8 V ≤ EVDD0 < 2.7 V: MIN. 125 ns

1.6 V ≤ EVDD0 < 1.8 V: MIN. 250 ns

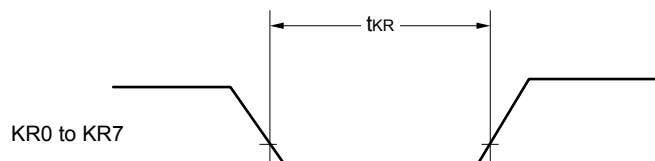
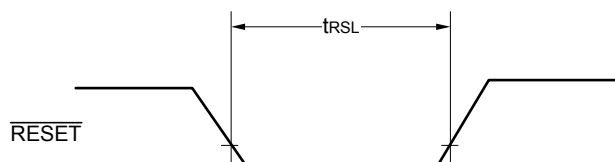
Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

Interrupt Request Input Timing



Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
Data hold time (transmission)	thd: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		0	405	0	405	ns

Note 1. The value must also be equal to or less than fMCK/4.**Note 2.** Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
				5.3		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4						
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
				5.3		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4						
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	fMCK/6 Notes 1, 2, 3		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
				5.3		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4						

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. Use it with EVDD0 ≥ Vb.**Note 3.** The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb [V]: Communication line voltage**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

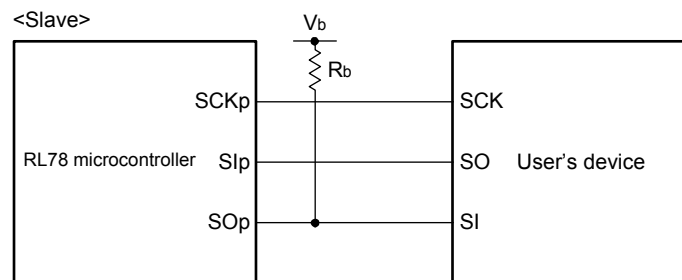
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fMCK	14/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	12/fMCK		—		—		ns
			8 MHz < fMCK ≤ 20 MHz	10/fMCK		—		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		10/fMCK		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fMCK	20/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	16/fMCK		—		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		—		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		—		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		10/fMCK		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	24 MHz < fMCK	48/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	36/fMCK		—		—		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		—		—		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		—		—		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		—		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		10/fMCK		ns
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		tkCY2/2 - 12		tkCY2/2 - 50		tkCY2/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		tkCY2/2 - 18		tkCY2/2 - 50		tkCY2/2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2		tkCY2/2 - 50		tkCY2/2 - 50		tkCY2/2 - 50		ns
Slp setup time (to SCKp↑) Note 3	tsIK2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2		1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns
Slp hold time (from SCKp↑) Note 4	tkSI2			1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output Note 5	tkSO2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ			2/fMCK + 120		2/fMCK + 573		2/fMCK + 573	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ			2/fMCK + 214		2/fMCK + 573		2/fMCK + 573	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rv = 5.5 kΩ			2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns

(Notes, Caution, and Remarks are listed on the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD0} \geq V_b$.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remark 1.** R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E _{zs}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	E _{fs}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI14		0		V _{DD}	V
		ANI16 to ANI20		0		EV _{DD0}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 4. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	4.36	mA	
					VDD = 3.0 V		0.80	4.36		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	3.67		
					VDD = 3.0 V		0.49	3.67		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.42		
					VDD = 3.0 V		0.62	3.42		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.85		
					VDD = 3.0 V		0.4	2.85		
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	2.08			
				VDD = 3.0 V		0.37	2.08			
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	2.45	mA	
					Resonator connection		0.40	2.57		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28	2.45		
					Resonator connection		0.40	2.57		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19	1.28		
					Resonator connection		0.25	1.36		
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input		0.19	1.28			
				Resonator connection		0.25	1.36			
		Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA		
				Resonator connection		0.44	0.76			
			fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57			
				Resonator connection		0.49	0.76			
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17			
				Resonator connection		0.59	1.36			
			fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97			
				Resonator connection		0.72	2.16			
			fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37			
				Resonator connection		1.16	3.56			
			fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		3.20	17.10			
				Resonator connection		3.40	17.50			
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
			TA = +25°C					0.24	0.51	
			TA = +50°C					0.29	1.10	
			TA = +70°C					0.41	1.90	
			TA = +85°C					0.90	3.30	
			TA = +105°C					3.10	17.00	

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.6	mA
						VDD = 3.0 V		2.6	
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.3	
						VDD = 3.0 V		2.3	
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.4	mA
						VDD = 3.0 V		5.4	
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.0	
						VDD = 3.0 V		5.0	
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.2	
						VDD = 3.0 V		4.2	
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	
						VDD = 3.0 V		4.0	
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		3.0	
						VDD = 3.0 V		3.0	
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.4	mA
						Resonator connection		3.6	
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.4	
						Resonator connection		3.6	
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.1	
						Resonator connection		2.2	
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.1	
						Resonator connection		2.2	
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.9	μA
						Resonator connection		4.9	
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.9	
						Resonator connection		4.9	
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.1	
						Resonator connection		5.1	
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.5	
						Resonator connection		5.5	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.5	
						Resonator connection		6.5	
				fSUB = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		13.0	
						Resonator connection		13.0	

(Notes and Remarks are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	250		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 24		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 36		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V	t _{KCY1} /2 - 76		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EVDD0 ≤ 5.5 V	66		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	66		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) Note 2	t _{KSH1}		38		ns
Delay time from SCKp↓ to SOp output Note 3	t _{KSO1}	C = 30 pF Note 4		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

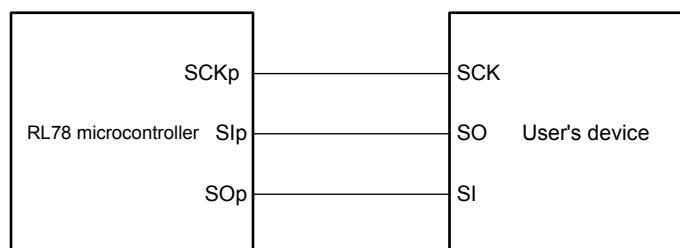
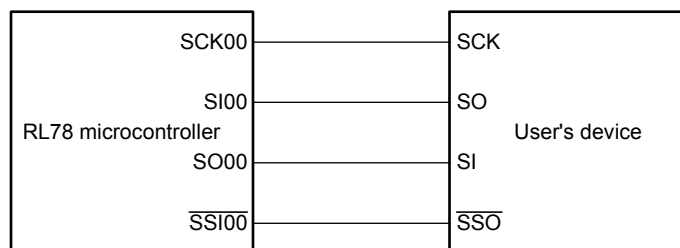
Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{\text{SSI00}}$ setup time	t_{SSIK}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
$\overline{\text{SSI00}}$ hold time	t_{kSSI}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns

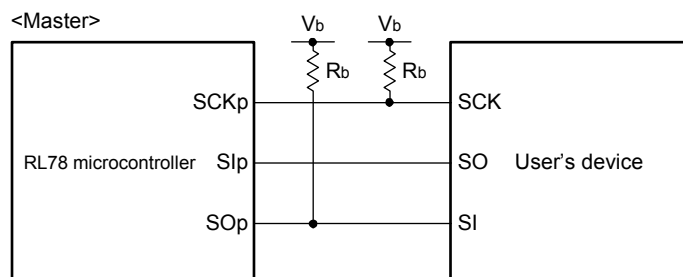
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)
CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))


Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

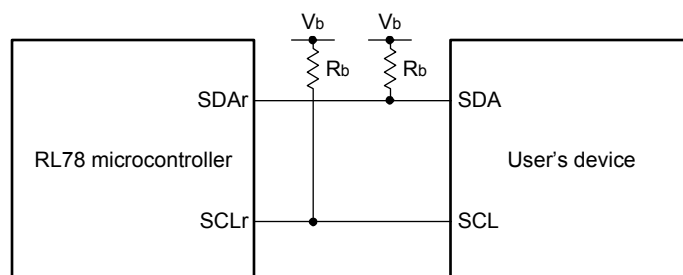
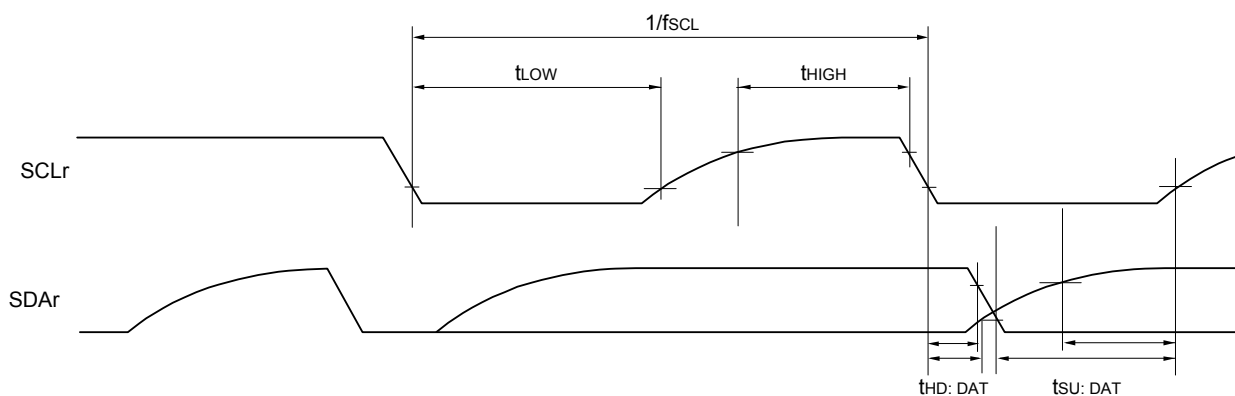
CSI mode connection diagram (during communication at different potential)

Remark 5. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 6. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 7. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 8. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

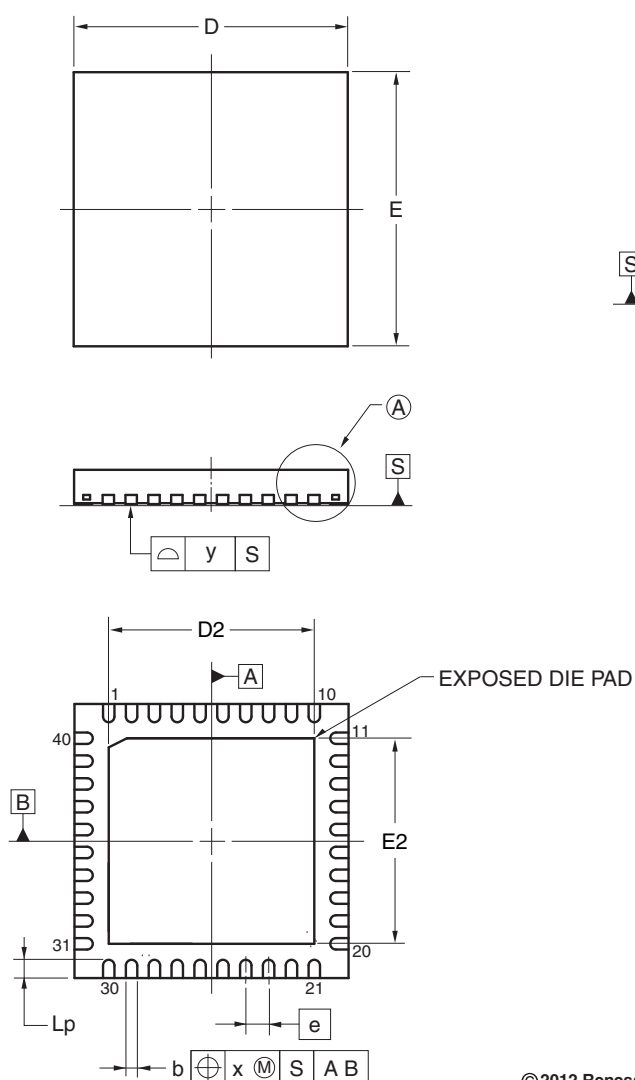
Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA,
R5F104EHANA
R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA,
R5F104EHDNA
R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA,
R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	4.45	4.50	4.55	4.45	4.50	4.55

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