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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104gfgfb-v0

(1/5)

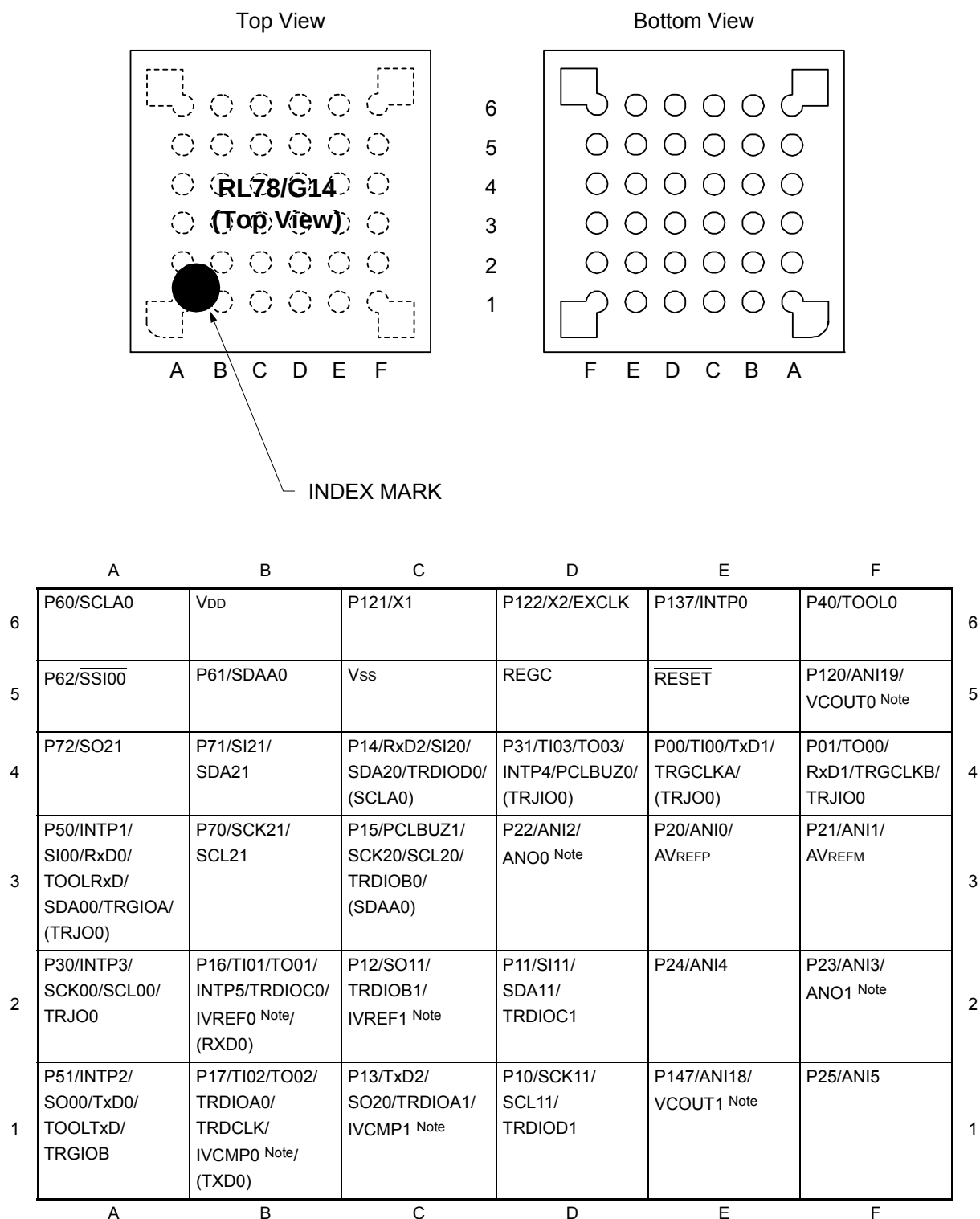
Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0 R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0 R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0 R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0 R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0 R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0 R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0 R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BDFP#V0, R5F104BGDFP#V0 R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0 R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0 R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0 R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications TA = -40 to +85°C

R5F104xxAxx

D: Industrial applications TA = -40 to +85°C

R5F104xxDxx

G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C

R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2	EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0	EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5	EVDD0	V
	VIH3	P20 to P27, P150 to P156	0.7 VDD		VDD	V
	VIH4	P60 to P63	0.7 EVDD0		6.0	V
	VIH5	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0		0.2 EVDD0	V
	VIL2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0	0.32	V
	VIL3	P20 to P27, P150 to P156	0		0.3 VDD	V
	VIL4	P60 to P63	0		0.3 EVDD0	V
	VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2 VDD	V

Caution The maximum value of VIH of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	Note 1		Note 1		Note 1	bps
									Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	Note 2		Note 2		Note 2	Mbps
									bps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	Note 3		Note 3		Note 3	Mbps
									bps

Note 1. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.

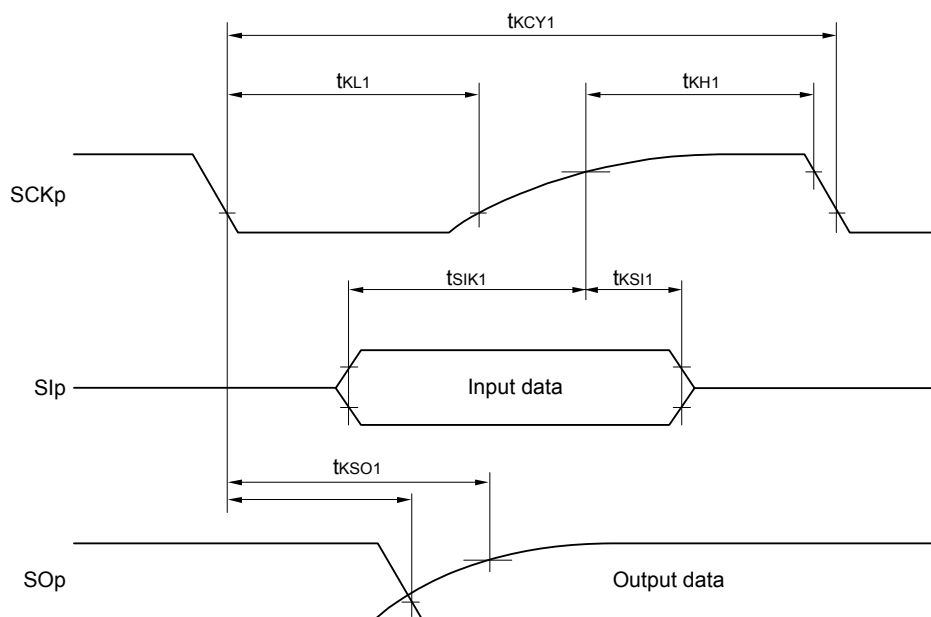
Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

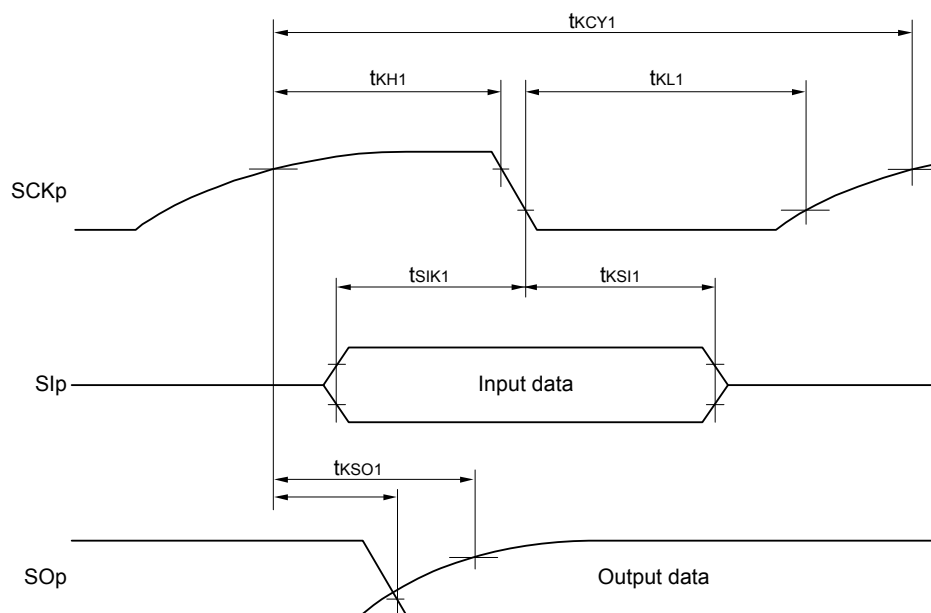
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(2) I²C fast mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	tsu: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	tHD: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	tsu: STO	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Caution** The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ EVDD0 ≤ 5.5 V		-60.0	mA
	IOH2	Per pin for P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ VDD ≤ 5.5 V		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
 <Example> Where n = 80% and IOH = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{DD0}				1 μA
	ILI _{H2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{DD}				1 μA
	ILI _{H3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{DD}	In input port or external clock input			1 μA
				In resonator connection			10 μA
Input leakage current, low	ILI _{L1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0}				-1 μA
	ILI _{L2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{SS}				-1 μA
	ILI _{L3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{SS}	In input port or external clock input			-1 μA
				In resonator connection			-10 μA
On-chip pull-up resistance	R _U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100 kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	tsik1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	tkS11	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/ EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time Note 1	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fMCK	28/fMCK	ns
			20 MHz < fMCK ≤ 24 MHz	24/fMCK	ns
			8 MHz < fMCK ≤ 20 MHz	20/fMCK	ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK	ns
			fMCK ≤ 4 MHz	12/fMCK	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fMCK	40/fMCK	ns
			20 MHz < fMCK ≤ 24 MHz	32/fMCK	ns
			16 MHz < fMCK ≤ 20 MHz	28/fMCK	ns
			8 MHz < fMCK ≤ 16 MHz	24/fMCK	ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK	ns
			fMCK ≤ 4 MHz	12/fMCK	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	24 MHz < fMCK	96/fMCK	ns
			20 MHz < fMCK ≤ 24 MHz	72/fMCK	ns
			16 MHz < fMCK ≤ 20 MHz	64/fMCK	ns
			8 MHz < fMCK ≤ 16 MHz	52/fMCK	ns
			4 MHz < fMCK ≤ 8 MHz	32/fMCK	ns
			fMCK ≤ 4 MHz	20/fMCK	ns
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	tkCY2/2 - 24		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	tkCY2/2 - 36		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	tkCY2/2 - 100		ns
Slp setup time (to SCKp↑) Note 2	tsIK2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/fMCK + 40		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fMCK + 40		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	1/fMCK + 60		ns
Slp hold time (from SCKp↑) Note 3	tsIS2		1/fMCK + 62		ns
Delay time from SCKp↓ to SOp output Note 4	tkSO2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/fMCK + 240	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fMCK + 428	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rv = 5.5 kΩ		2/fMCK + 1146	ns

(Notes, Caution, and Remarks are listed on the next page.)

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		5			μs

3.6.3 D/A converter characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVSS0 = EVSS1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

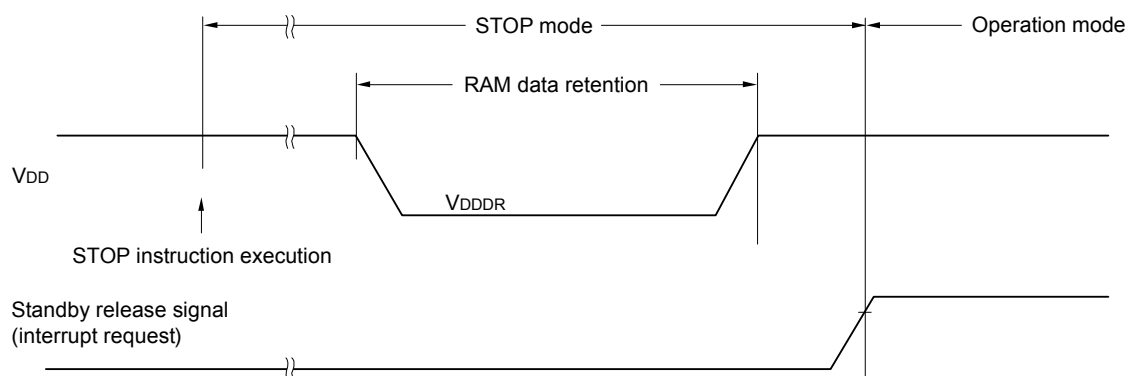
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.4 V ≤ VDD ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.4 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 5.5 V			3	μs
			2.4 V ≤ VDD < 2.7 V			6	μs

3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ Note 4	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

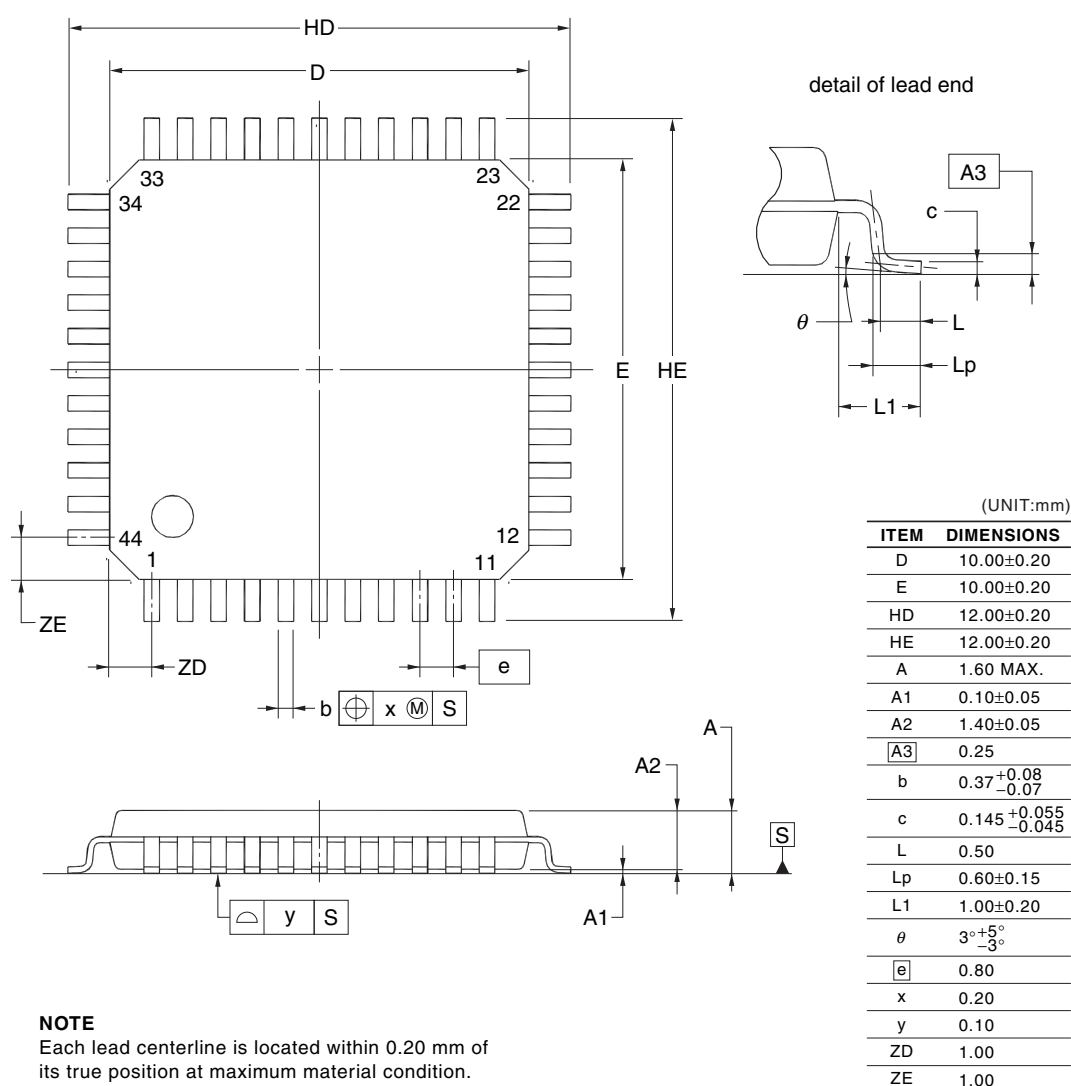
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.5 44-pin products

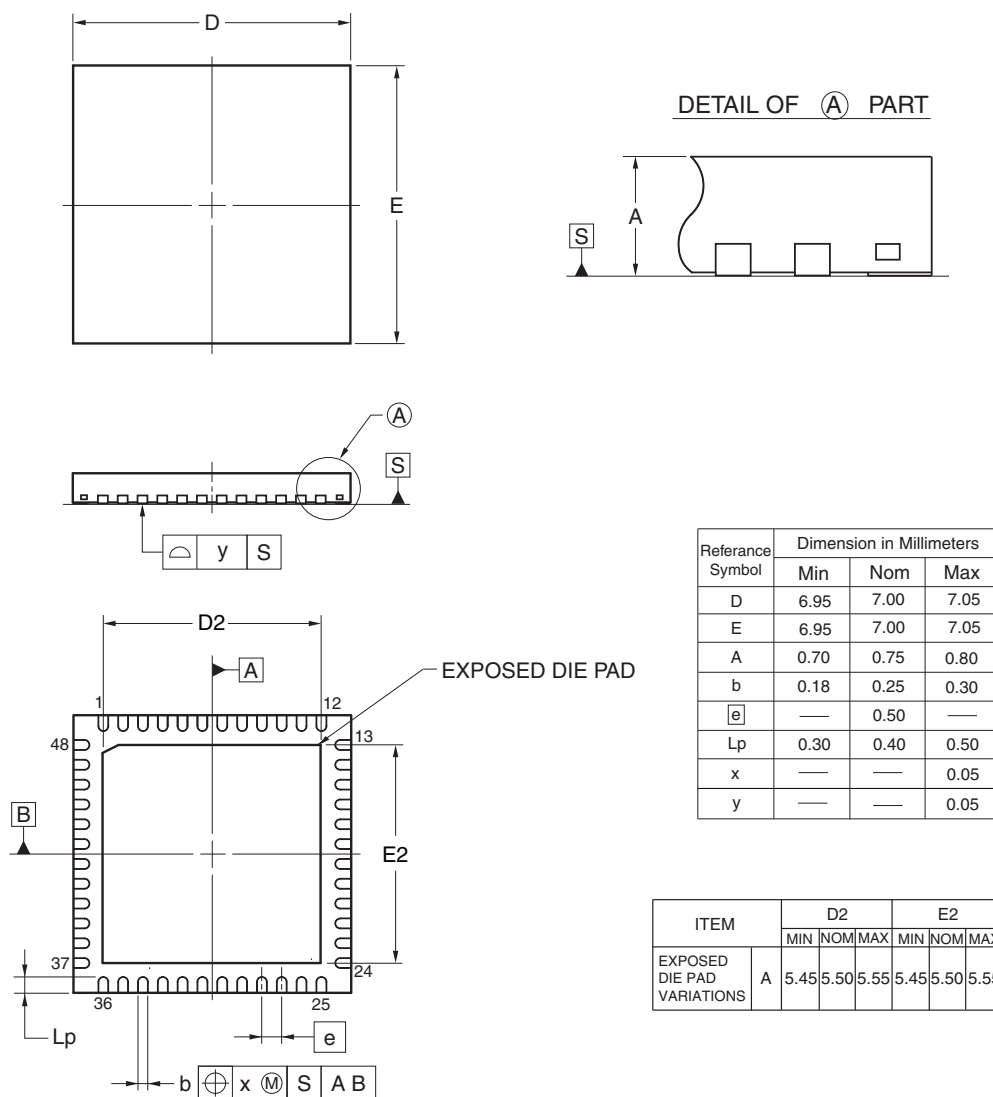
R5F104FAAFP, R5F104FCAFP, R5F104FDAFP, R5F104FEAFP, R5F104FFAFP, R5F104FGAFP,
 R5F104FHAFP, R5F104FJAFP
 R5F104FADFP, R5F104FCDFP, R5F104FDDFP, R5F104FEDFP, R5F104FFDFP, R5F104FGDFP,
 R5F104FHDFP, R5F104FJDFP
 R5F104FAGFP, R5F104FCGFP, R5F104FDGFP, R5F104FEGFP, R5F104FFGFP, R5F104FGGFP,
 R5F104FHGFP, R5F104FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA,
 R5F104GHANA, R5F104GJANA
 R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA,
 R5F104GHDNA, R5F104GJDNA
 R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,
 R5F104GHGNA, R5F104GJGNA
 R5F104GKANA, R5F104GLANA
 R5F104GKGNA, R5F104GLGNA

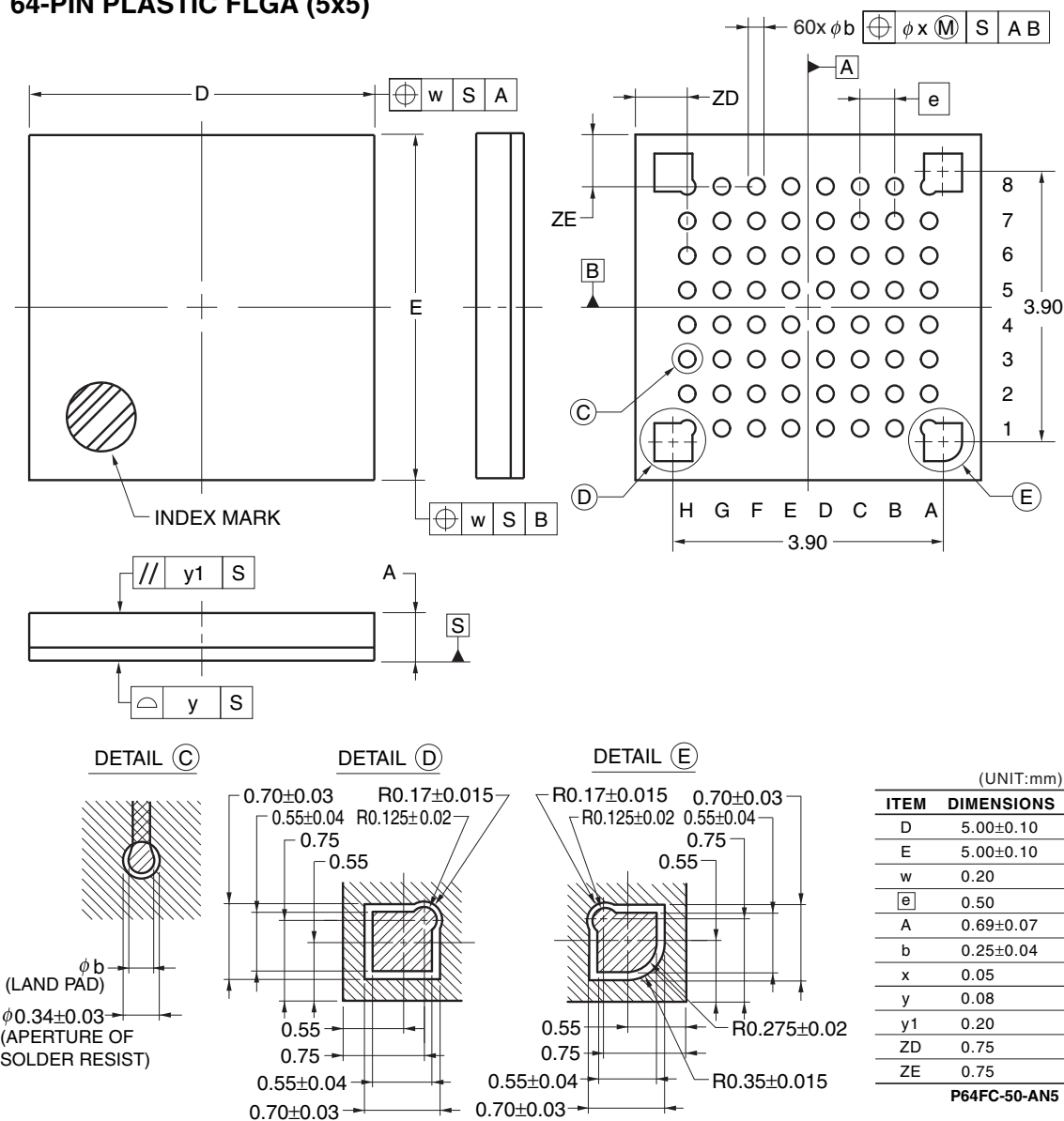
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



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R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
 R5F104LKALA, R5F104LLALA
 R5F104LCGLA, R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
 R5F104LKGLA, R5F104LLGLA

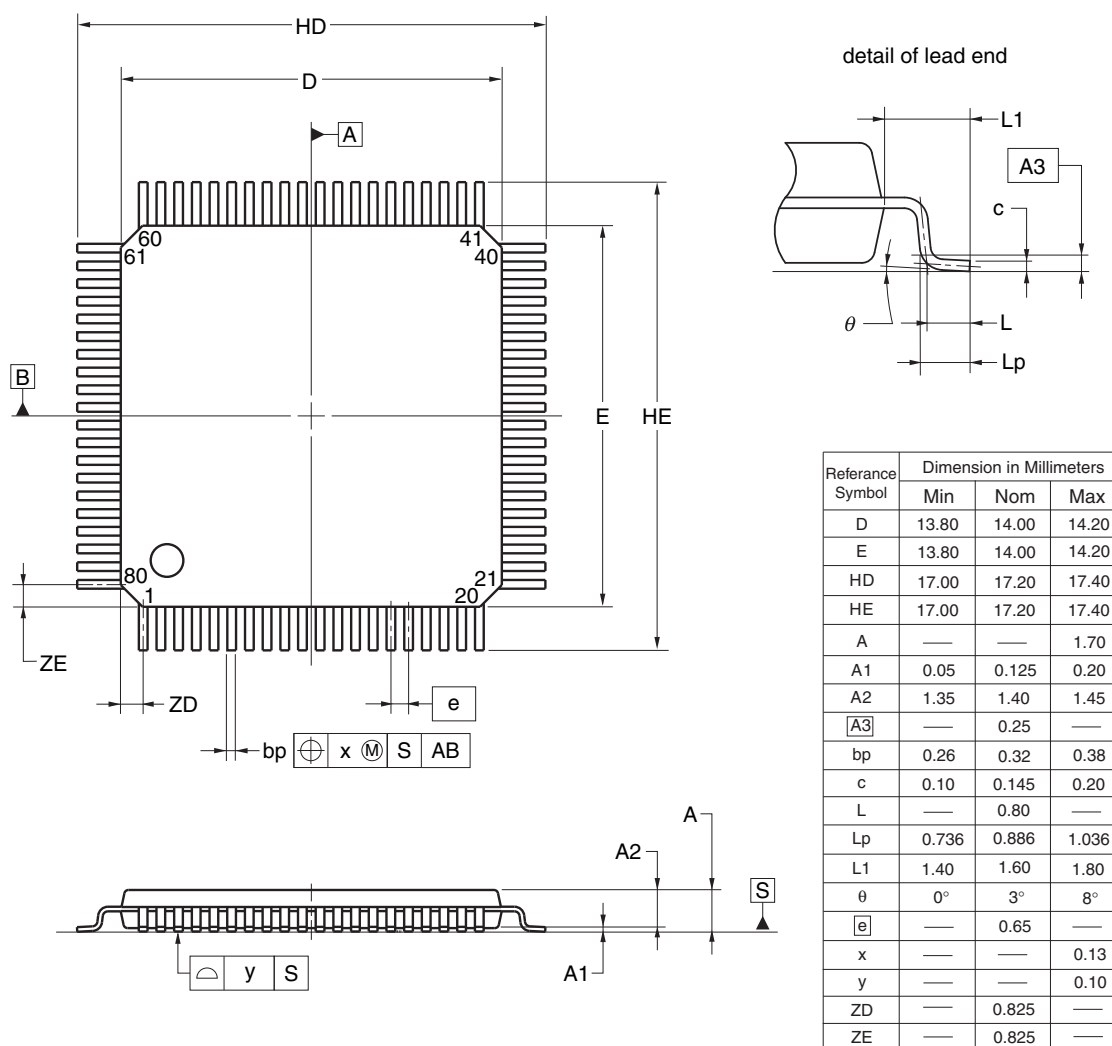
64-PIN PLASTIC FLGA (5x5)



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R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJFAFA
 R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
 R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
 R5F104MKAFA, R5F104MLAFA
 R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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