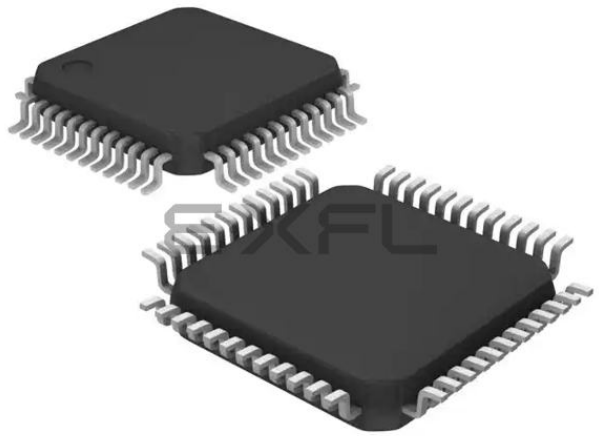
# Renesas Electronics America Inc - R5F104GHGFB#V0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 10x8/10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ghgfb-v0 |

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| Pin count | Package | Fields of Application Note | Ordering Part Number |
|---|---|---|---|
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch) | A | R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0<br>R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0<br>R5F104GKAFB#30, R5F104GLAFB#30<br>R5F104GKAFB#50, R5F104GLAFB#50 |
| | | D | R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GFDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0<br>R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GFDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0 |
| | | G | R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0<br>R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0<br>R5F104GKGFB#30, R5F104GLGFB#30<br>R5F104GKGFB#50, R5F104GLGFB#50 |
| | 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch) | A | R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0<br>R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0<br>R5F104GKANA#U0, R5F104GLANA#U0<br>R5F104GKANA#W0, R5F104GLANA#W0 |
| | | D | R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0<br>R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0 |
| | | G | R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0<br>R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0<br>R5F104GKGNA#U0, R5F104GLGNA#U0<br>R5F104GKGNA#W0, R5F104GLGNA#W0 |
| 52 pins | 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch) | A | R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0<br>R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0 |
| | | D | R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0<br>R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0 |
| | | G | R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0<br>R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0 |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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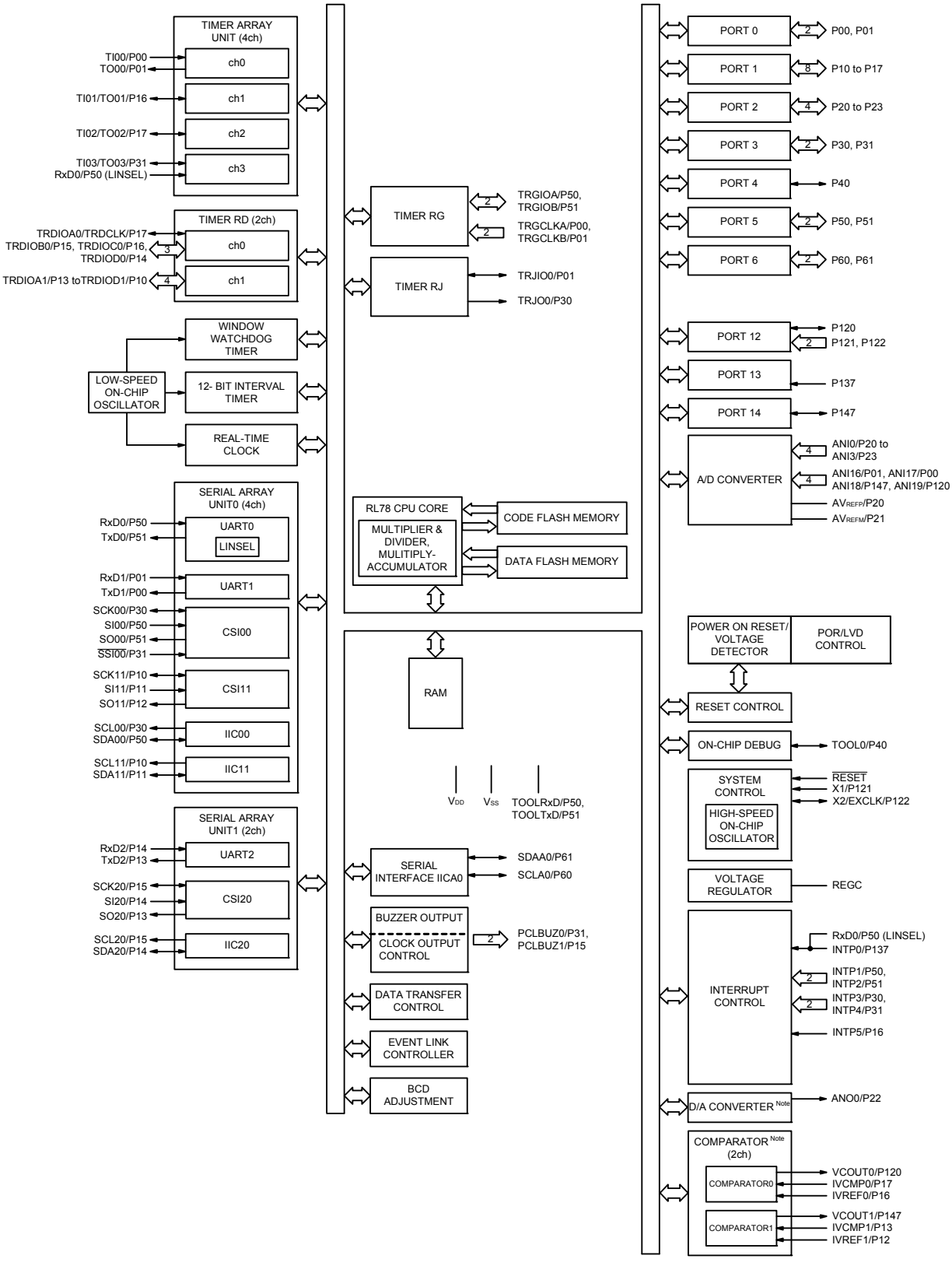
| Pin count | Package | Fields of Application Note | Ordering Part Number |
|---|---|---|---|
| 80 pins | 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch) | A | R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFB#V0, R5F104MJAFB#V0<br>R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFB#X0, R5F104MJAFB#X0<br>R5F104MKAFB#30, R5F104MLAFB#30<br>R5F104MKAFB#50, R5F104MLAFB#50 |
| | | D | R5F104MFDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0<br>R5F104MFDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0 |
| | | G | R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0<br>R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0<br>R5F104MKGFB#30, R5F104MLGFB#30<br>R5F104MKGFB#X0, R5F104MLGFB#50 |
| | 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch) | A | R5F104MFAFA#V0, R5F104MGAFA#V0, R5F104MHAFA#V0, R5F104MJAFA#V0<br>R5F104MFAFA#X0, R5F104MGAFA#X0, R5F104MHAFA#X0, R5F104MJAFA#X0<br>R5F104MKAFA#30, R5F104MLAFA#30<br>R5F104MKAFA#50, R5F104MLAFA#50 |
| | | D | R5F104MFDFA#V0, R5F104MGDFA#V0, R5F104MHDFA#V0, R5F104MJDFA#V0<br>R5F104MFDFA#X0, R5F104MGDFA#X0, R5F104MHDFA#X0, R5F104MJDFA#X0 |
| | | G | R5F104MFGFA#V0, R5F104MGGFA#V0, R5F104MHGFA#V0, R5F104MJGFA#V0<br>R5F104MFGFA#X0, R5F104MGGFA#X0, R5F104MHGFA#X0, R5F104MJGFA#X0<br>R5F104MKGFA#30, R5F104MLGFA#30<br>R5F104MKGFA#50, R5F104MLGFA#50 |
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch) | A | R5F104PFAFB#V0, R5F104PGAFB#V0, R5F104PHAFB#V0, R5F104PJAFB#V0<br>R5F104PFAFB#X0, R5F104PGAFB#X0, R5F104PHAFB#X0, R5F104PJAFB#X0<br>R5F104PKAFB#30, R5F104PLAFB#30<br>R5F104PKAFB#50, R5F104PLAFB#50 |
| | | D | R5F104PFDFB#V0, R5F104PGDFB#V0, R5F104PHDFB#V0, R5F104PJDFB#V0<br>R5F104PFDFB#X0, R5F104PGDFB#X0, R5F104PHDFB#X0, R5F104PJDFB#X0 |
| | | G | R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0<br>R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0<br>R5F104PKGFB#30, R5F104PLGFB#30<br>R5F104PKGFB#50, R5F104PLGFB#50 |
| | 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch) | A | R5F104PFAFA#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFA#V0<br>R5F104PFAFA#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFA#X0<br>R5F104PKAFA#30, R5F104PLAFA#30<br>R5F104PKAFA#50, R5F104PLAFA#50 |
| | | D | R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFA#V0<br>R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFA#X0 |
| | | G | R5F104PFGFA#V0, R5F104PGGFA#V0, R5F104PHGFA#V0, R5F104PJGFA#V0<br>R5F104PFGFA#X0, R5F104PGGFA#X0, R5F104PHGFA#X0, R5F104PJGFA#X0<br>R5F104PKGFA#30, R5F104PLGFA#30<br>R5F104PKGFA#50, R5F104PLGFA#50 |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution** **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

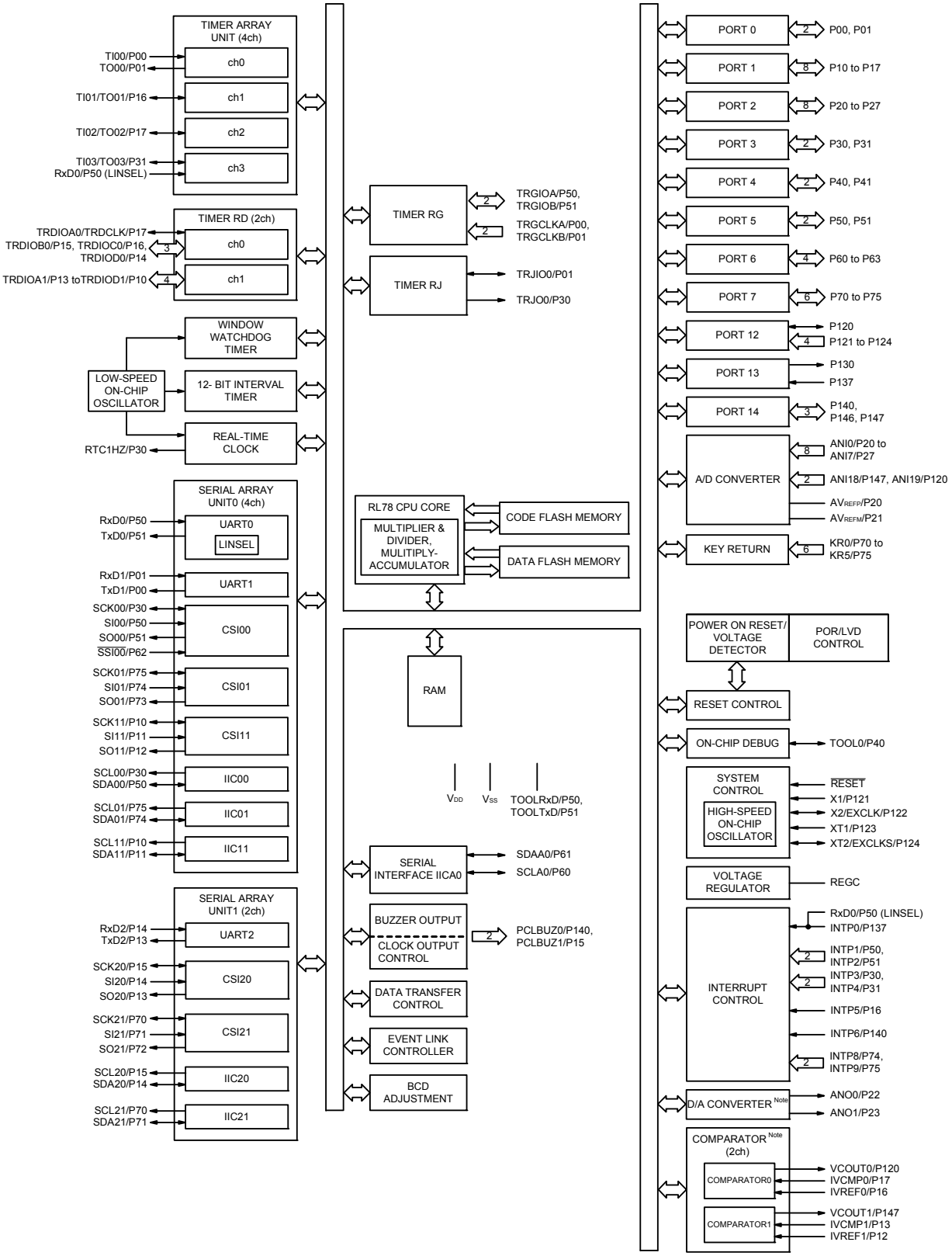
## 1.5 Block Diagram

### 1.5.1 30-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.6 48-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

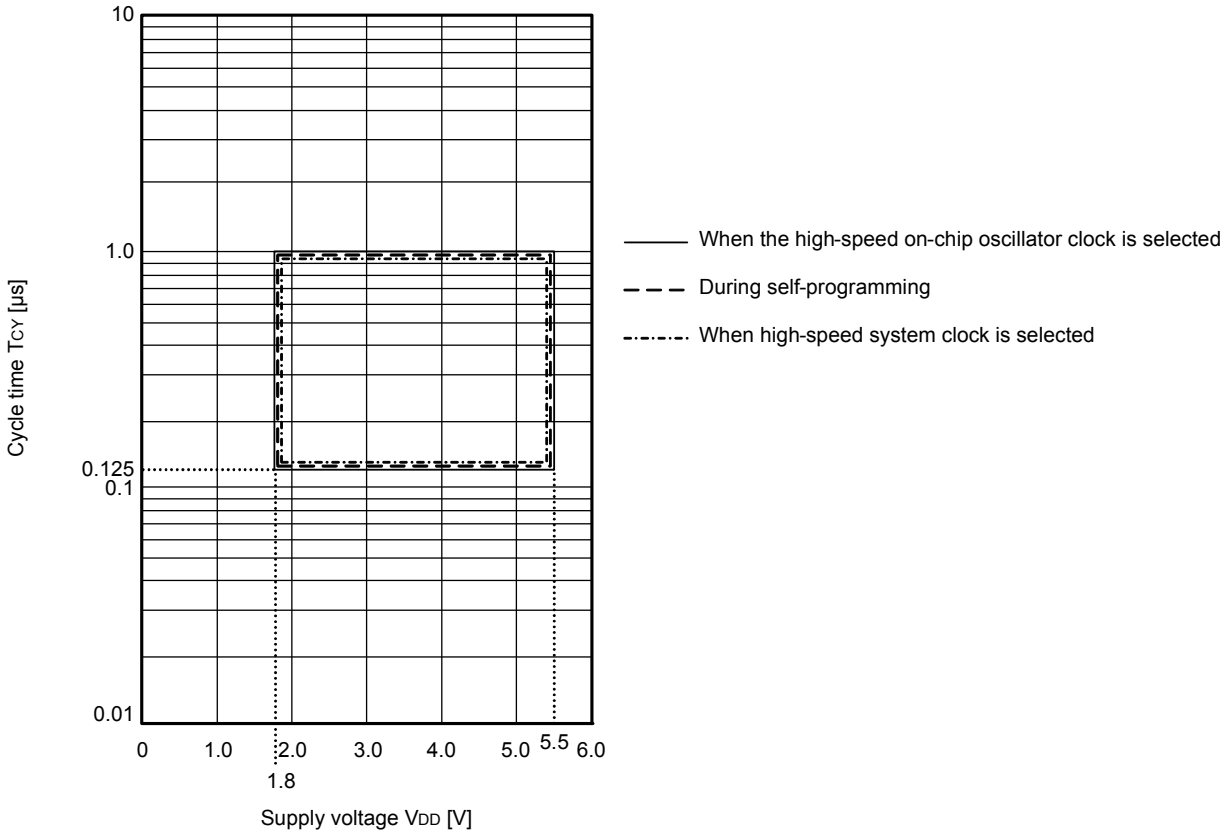
### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)(2/2)**

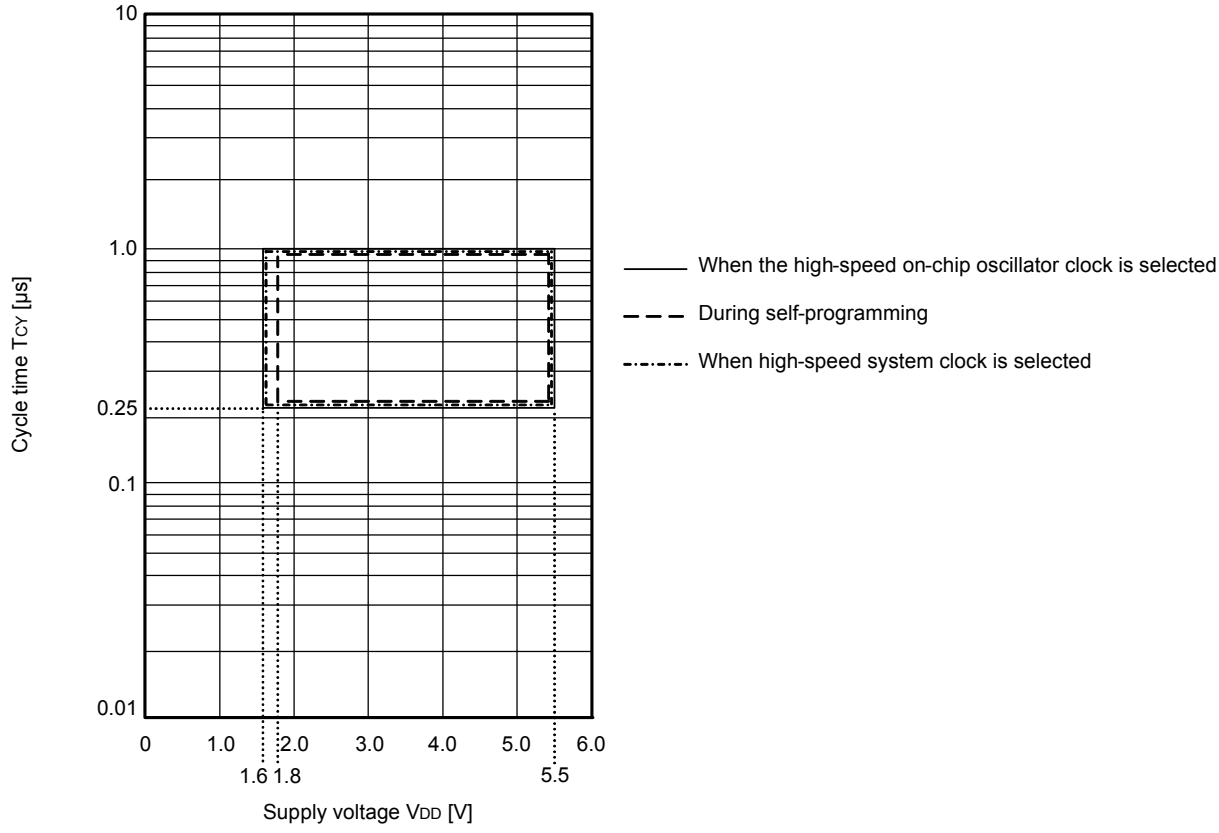
| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 3.09 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 3.09 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.40 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.40 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.38 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 710 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 710 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 700 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 700 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 550 | μA |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 550 | |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |

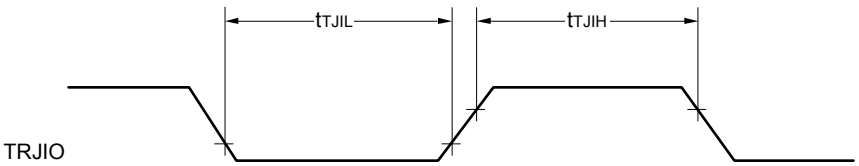
(**Notes** and **Remarks** are listed on the next page.)

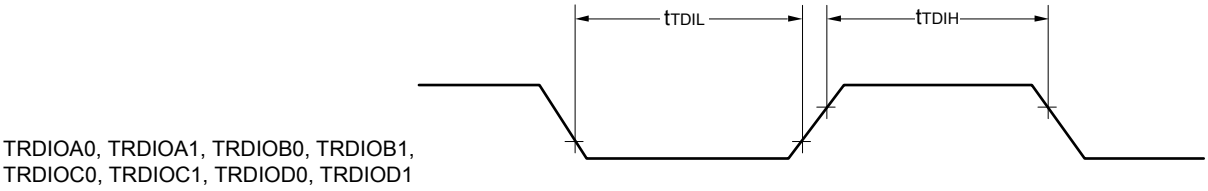
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)

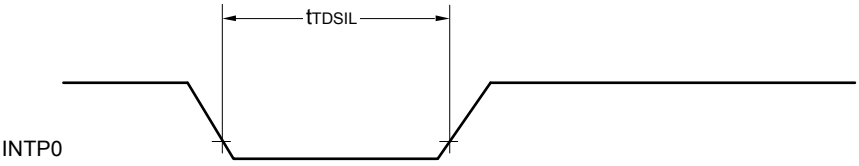


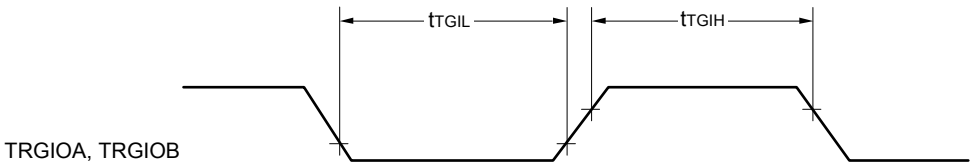

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



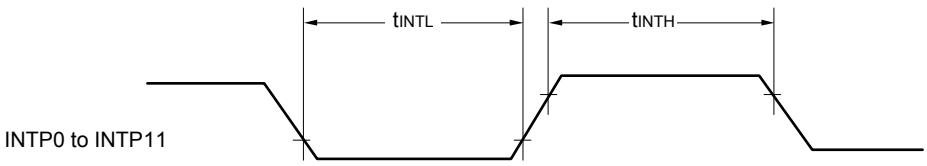

tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1

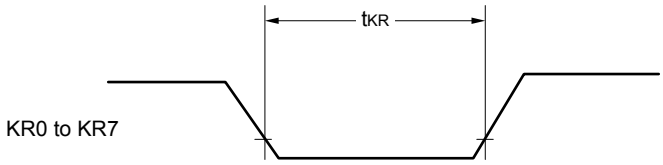

tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

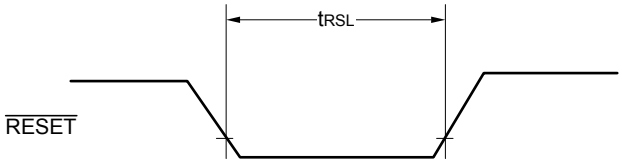
Interrupt Request Input Timing




Key Interrupt Input Timing




$\overline{\text{RESET}}$ Input Timing



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

## 2.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |

(**Notes**, **Caution**, and **Remark** are listed on the next page.)

## 2.6.4 Comparator

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage range | Ivref | | | 0 | | $EV_{DD0}$ - 1.4 | V |
| | Ivcmp | | | -0.3 | | $EV_{DD0}$ + 0.3 | V |
| Output delay | td | $V_{DD}$ = 3.0 V<br>Input slew rate > 50 mV/µs | Comparator high-speed mode, standard mode | | | 1.2 | µs |
| | | | Comparator high-speed mode, window mode | | | 2.0 | µs |
| | | | Comparator low-speed mode, standard mode | | 3.0 | 5.0 | µs |
| High-electric-potential reference voltage | VTW+ | Comparator high-speed mode, window mode | | | 0.76 $V_{DD}$ | | V |
| Low-electric-potential reference voltage | VTW- | Comparator high-speed mode, window mode | | | 0.24 $V_{DD}$ | | V |
| Operation stabilization wait time | $t_{CMP}$ | | | 100 | | | µs |
| Internal reference voltage Note | $V_{BGR}$ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode | | 1.38 | 1.45 | 1.50 | V |

**Note** Not usable in LS (low-speed main) mode, LV (low-voltage main) mode, sub-clock operation, or STOP mode.

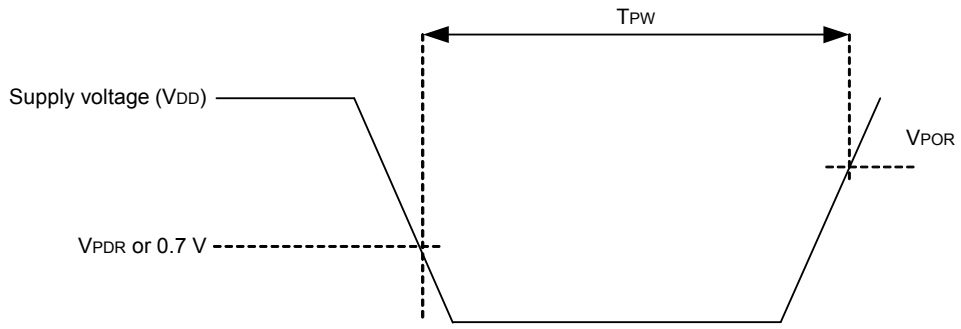
## 2.6.5 POR circuit characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power on/down reset threshold | $V_{POR}$ | Voltage threshold on $V_{DD}$ rising | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Voltage threshold on $V_{DD}$ falling Note 1 | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note 2 | $T_{PW}$ | | 300 | | | µs |

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

**Note 2.** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R>

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 5.16 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 5.16 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 4.47 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 4.47 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 4.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 4.08 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 3.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 3.51 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 2.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 2.38 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.83 | mA |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.83 | |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.31 | 0.76 | µA |
| | | | | | Resonator connection | | 0.50 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.38 | 0.76 | |
| | | | | | Resonator connection | | 0.57 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.47 | 3.59 | |
| | | | | | Resonator connection | | 0.70 | 3.78 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.80 | 6.20 | |
| | | | | | Resonator connection | | 1.00 | 6.39 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.65 | 10.56 | |
| | | | | | Resonator connection | | 1.84 | 10.75 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 8.00 | 65.7 | |
| | | | | | Resonator connection | | 8.00 | 65.7 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.63 | µA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.63 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.47 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.08 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.44 | |
| | | | $T_A$ = +105°C | | | | 6.50 | 67.14 | |

(**Notes** and **Remarks** are listed on the next page.)

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note 2 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 1.3 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

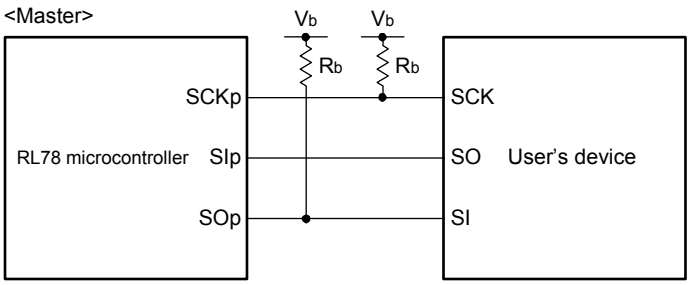
**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

**CSI mode connection diagram (during communication at different potential**




**Remark 5.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 6.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 7.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 8.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

## 3.6.6 LVD circuit characteristics

**(1) Reset Mode and Interrupt Mode**

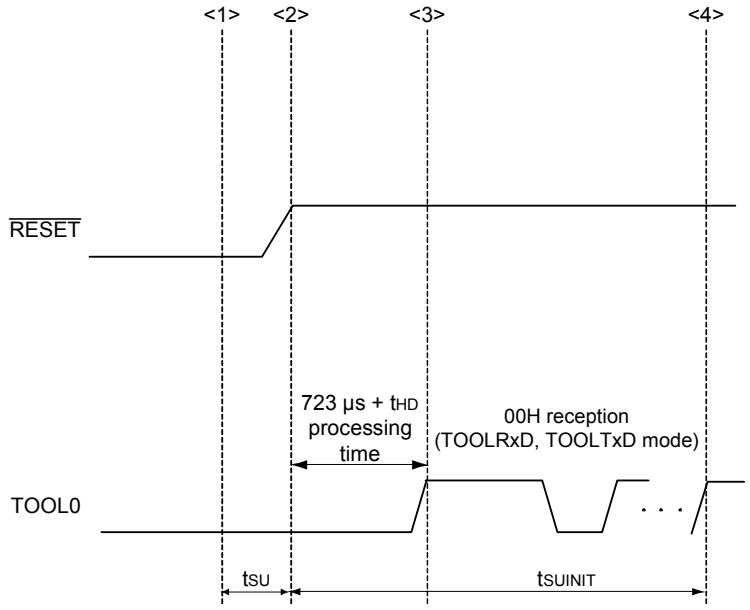
**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.90 | 4.06 | 4.22 | V |
| | | | Falling edge | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Rising edge | 3.60 | 3.75 | 3.90 | V |
| | | | Falling edge | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Rising edge | 3.01 | 3.13 | 3.25 | V |
| | | | Falling edge | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Rising edge | 2.90 | 3.02 | 3.14 | V |
| | | | Falling edge | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Rising edge | 2.81 | 2.92 | 3.03 | V |
| | | | Falling edge | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Rising edge | 2.70 | 2.81 | 2.92 | V |
| | | | Falling edge | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Rising edge | 2.61 | 2.71 | 2.81 | V |
| | | | Falling edge | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Rising edge | 2.51 | 2.61 | 2.71 | V |
| | | | Falling edge | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

## 3.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



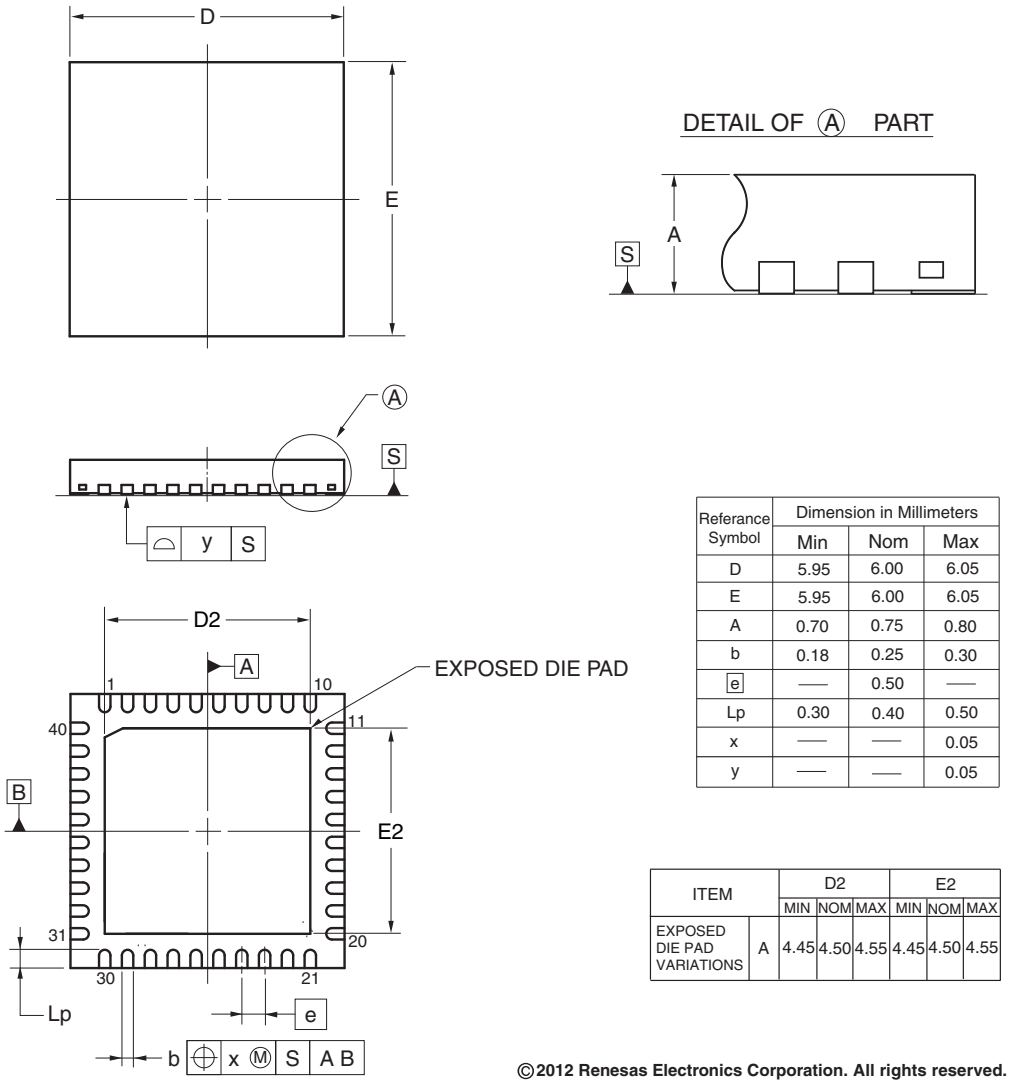

<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

## 4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA
R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA
R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA, R5F104EHGNA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-4 | 0.09 |

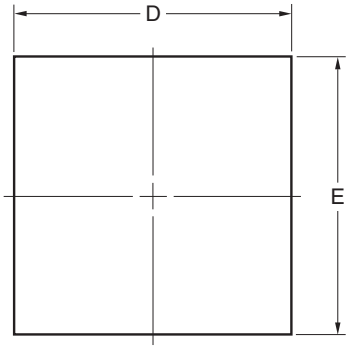


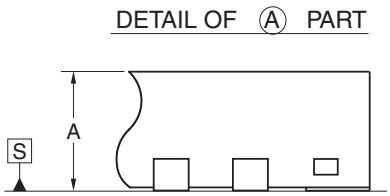

| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

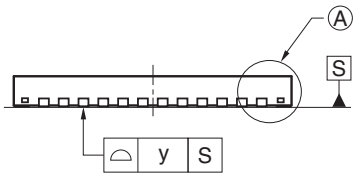
| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 4.45 | 4.50 | 4.55 | 4.45 | 4.50 | 4.55 |

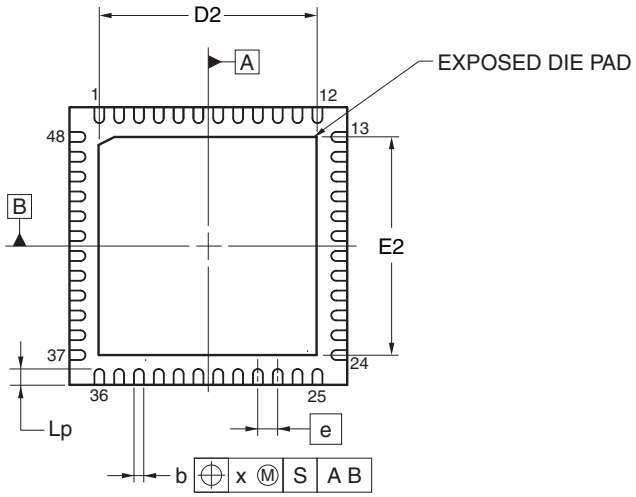
R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA, R5F104GHANA, R5F104GJANA
R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA, R5F104GHDNA, R5F104GJDNA
R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA, R5F104GHGNA, R5F104GJGNA
R5F104GKANA, R5F104GLANA
R5F104GKGNA, R5F104GLGNA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-5 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 5.45 | 5.50 | 5.55 | 5.45 | 5.50 | 5.55 |