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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104gkafb-30">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104gkafb-30</a>

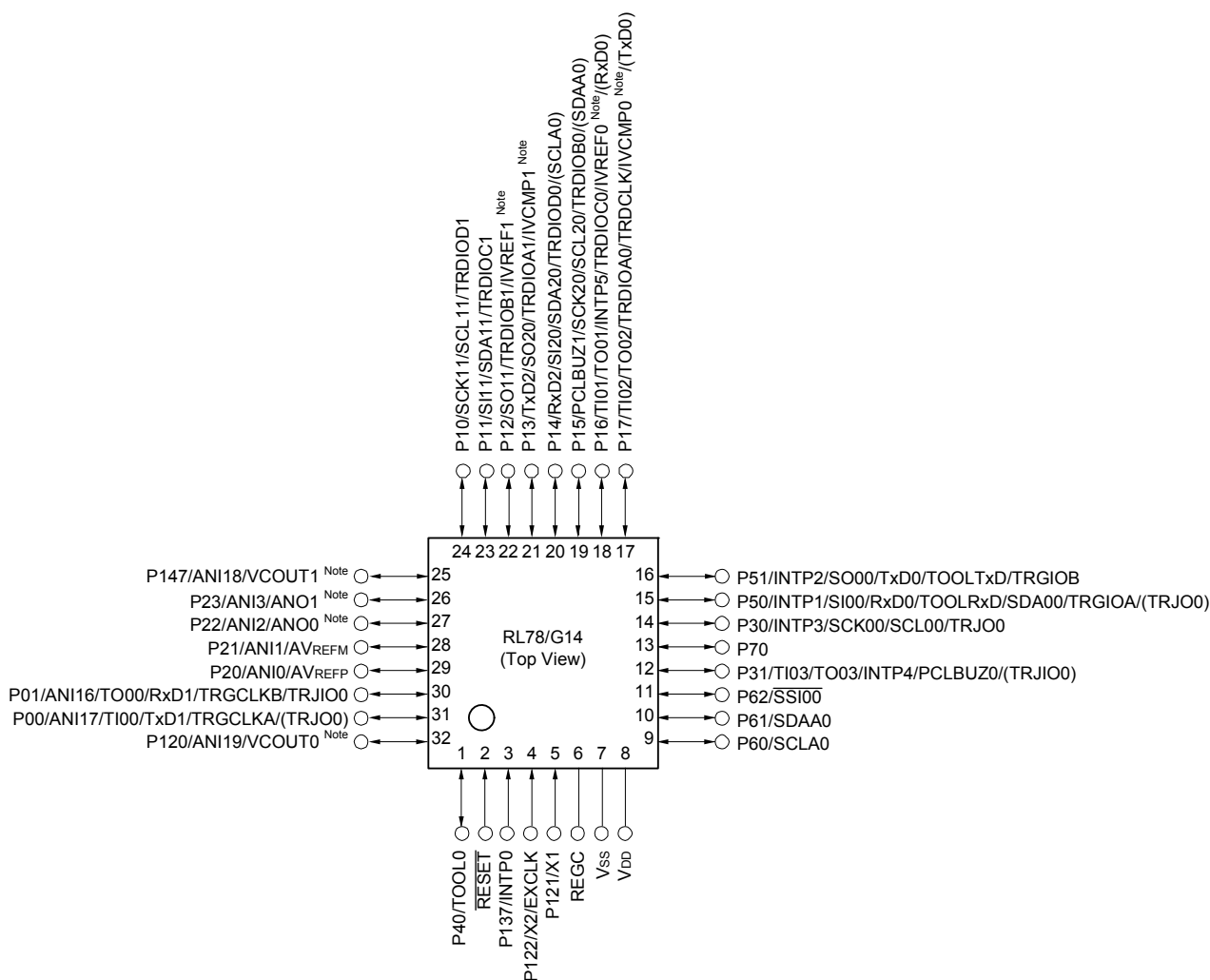
(3/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0 R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 R5F104GKAFB#30, R5F104GLAFB#30 R5F104GKAFB#50, R5F104GLAFB#50
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0 R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0 R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0 R5F104GKGB#30, R5F104GLGB#30 R5F104GKGB#50, R5F104GLGB#50
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0 R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0 R5F104GKANA#U0, R5F104GLANA#U0 R5F104GKANA#W0, R5F104GLANA#W0
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0 R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0 R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0 R5F104GKGNA#U0, R5F104GLGNA#U0 R5F104GKGNA#W0, R5F104GLGNA#W0
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHFAFA#V0, R5F104JJFAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHFAFA#X0, R5F104JJFAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



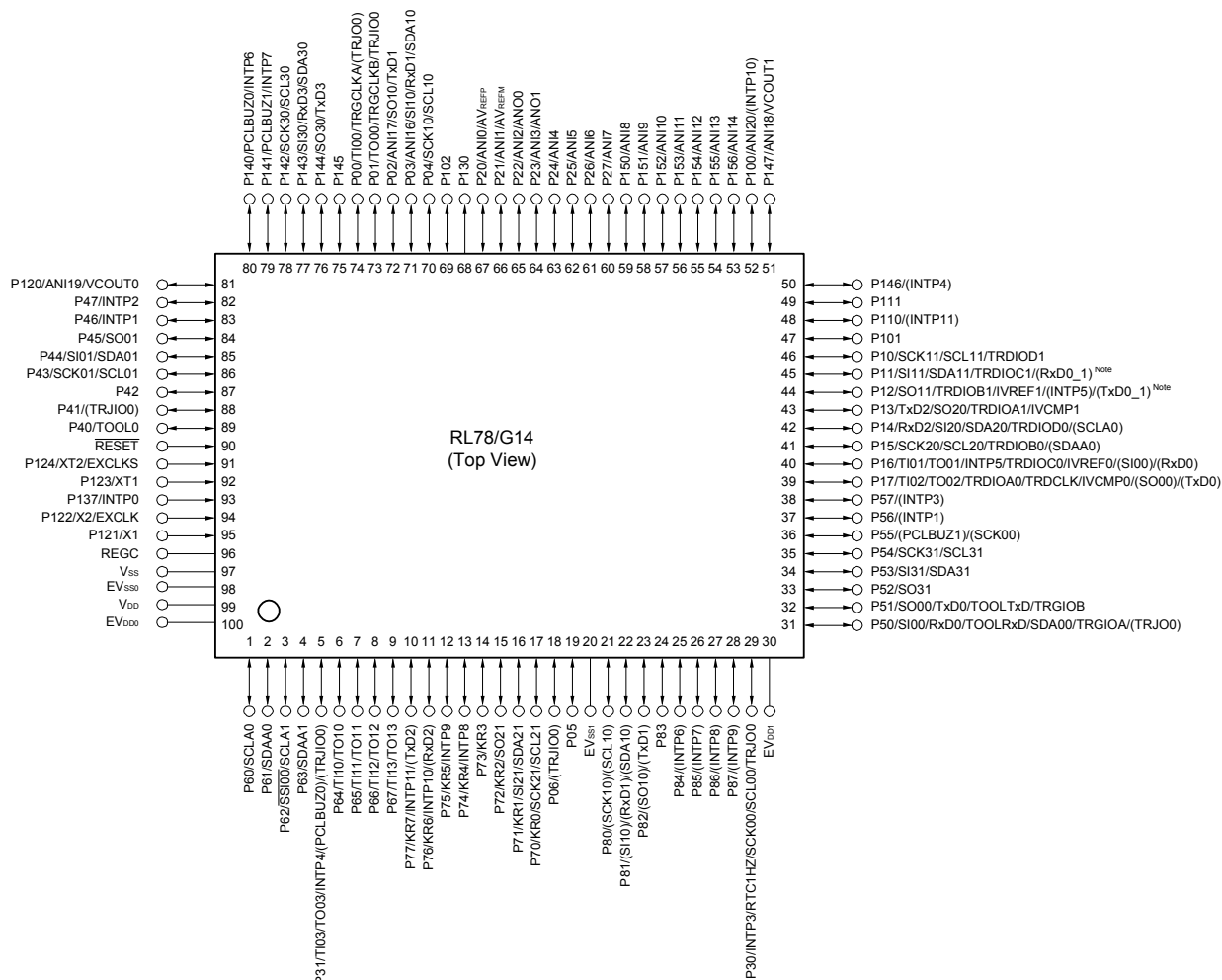
**Note** Mounted on the 96 KB or more code flash memory products.

**Caution** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1  $\mu$ F).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



**Note** Mounted on the 384 KB or more code flash memory products.

**Caution 1.** Make EVSS0, EVSS1 pins the same potential as Vss pin.

**Caution 2.** Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

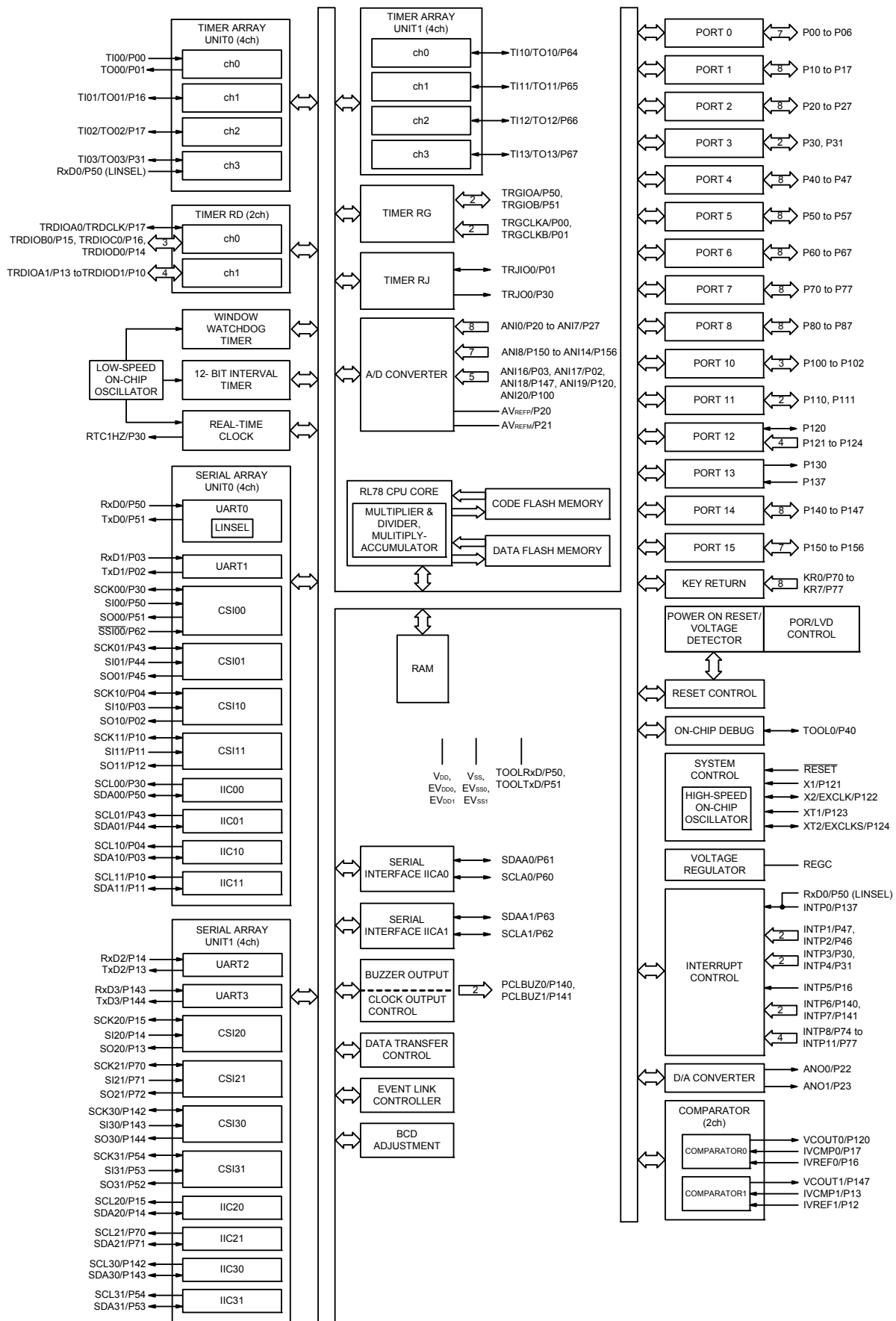
**Caution 3.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVSS0 and EVSS1 pins to separate ground lines.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

## 1.5.10 100-pin products



[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Code flash memory (KB)		96 to 128	96 to 128	96 to 128	96 to 192
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 16 Note	12 to 16 Note	12 to 16 Note	12 to 20 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ( $V_{DD} = 2.7$ to $5.5$ V), HS (high-speed main) mode: 1 to 16 MHz ( $V_{DD} = 2.4$ to $5.5$ V), LS (low-speed main) mode: 1 to 8 MHz ( $V_{DD} = 1.8$ to $5.5$ V), LV (low-voltage main) mode: 1 to 4 MHz ( $V_{DD} = 1.6$ to $5.5$ V)			
	High-speed on-chip oscillator clock ( $f_{IH}$ )	HS (high-speed main) mode: 1 to 32 MHz ( $V_{DD} = 2.7$ to $5.5$ V), HS (high-speed main) mode: 1 to 16 MHz ( $V_{DD} = 2.4$ to $5.5$ V), LS (low-speed main) mode: 1 to 8 MHz ( $V_{DD} = 1.8$ to $5.5$ V), LV (low-voltage main) mode: 1 to 4 MHz ( $V_{DD} = 1.6$ to $5.5$ V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to $5.5$ V			
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)			
Minimum instruction execution time		0.03125 $\mu$ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)			
		0.05 $\mu$ s (High-speed system clock: $f_{MX} = 20$ MHz operation)			
		—			30.5 $\mu$ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)
Instruction set		<ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits <math>\times</math> 8 bits, 16 bits <math>\times</math> 16 bits), Division (16 bits <math>\div</math> 16 bits, 32 bits <math>\div</math> 32 bits)</li> <li>• Multiplication and Accumulation (16 bits <math>\times</math> 16 bits <math>\div</math> 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li> </ul>			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)

(Note is listed on the next page.)

(2/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
D/A converter		1 channel	2 channels		
Comparator		2 channels			
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels			
	I <sup>2</sup> C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources			31 sources
Event link controller (ELC)		Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V ( $T_A = -40$ to +85°C) 1.51 ±0.06 V ( $T_A = -40$ to +105°C) • Power-down-reset: 1.50 ±0.04 V ( $T_A = -40$ to +85°C) 1.50 ±0.06 V ( $T_A = -40$ to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		$V_{DD} = 1.6$ to 5.5 V ( $T_A = -40$ to +85°C) $V_{DD} = 2.4$ to 5.5 V ( $T_A = -40$ to +105°C)			
Operating ambient temperature		$T_A = -40$ to +85°C (A: Consumer applications, D: Industrial applications), $T_A = -40$ to +105°C (G: Industrial applications)			

**Note** The illegal instruction is generated when instruction code FFH is executed.  
 Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item		48-pin	64-pin
		R5F104Gx (x = K, L)	R5F104Lx (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)	
8/10-bit resolution A/D converter		10 channels	12 channels
D/A converter		2 channels	
Comparator		2 channels	
Serial interface		[48-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels	
		I <sup>2</sup> C bus	1 channel
Data transfer controller (DTC)		32 sources	33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9	
Vectored interrupt sources	Internal	24	24
	External	10	13
Key interrupt		6	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T <sub>A</sub> = -40 to +85°C) 1.51 ±0.06 V (T <sub>A</sub> = -40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T <sub>A</sub> = -40 to +85°C) 1.50 ±0.06 V (T <sub>A</sub> = -40 to +105°C)	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)	
Operating ambient temperature		T <sub>A</sub> = -40 to +85°C (A: Consumer applications, D: Industrial applications), T <sub>A</sub> = -40 to +105°C (G: Industrial applications)	

**Note** The illegal instruction is generated when instruction code FFH is executed.  
 Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.



## 2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications TA = -40 to +85°C

R5F104xxAxx

D: Industrial applications TA = -40 to +85°C

R5F104xxDxx

G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C

R5F104xxGxx

**Caution 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

**Caution 2.** With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

**Caution 3.** The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

**Absolute Maximum Ratings****(2/2)**

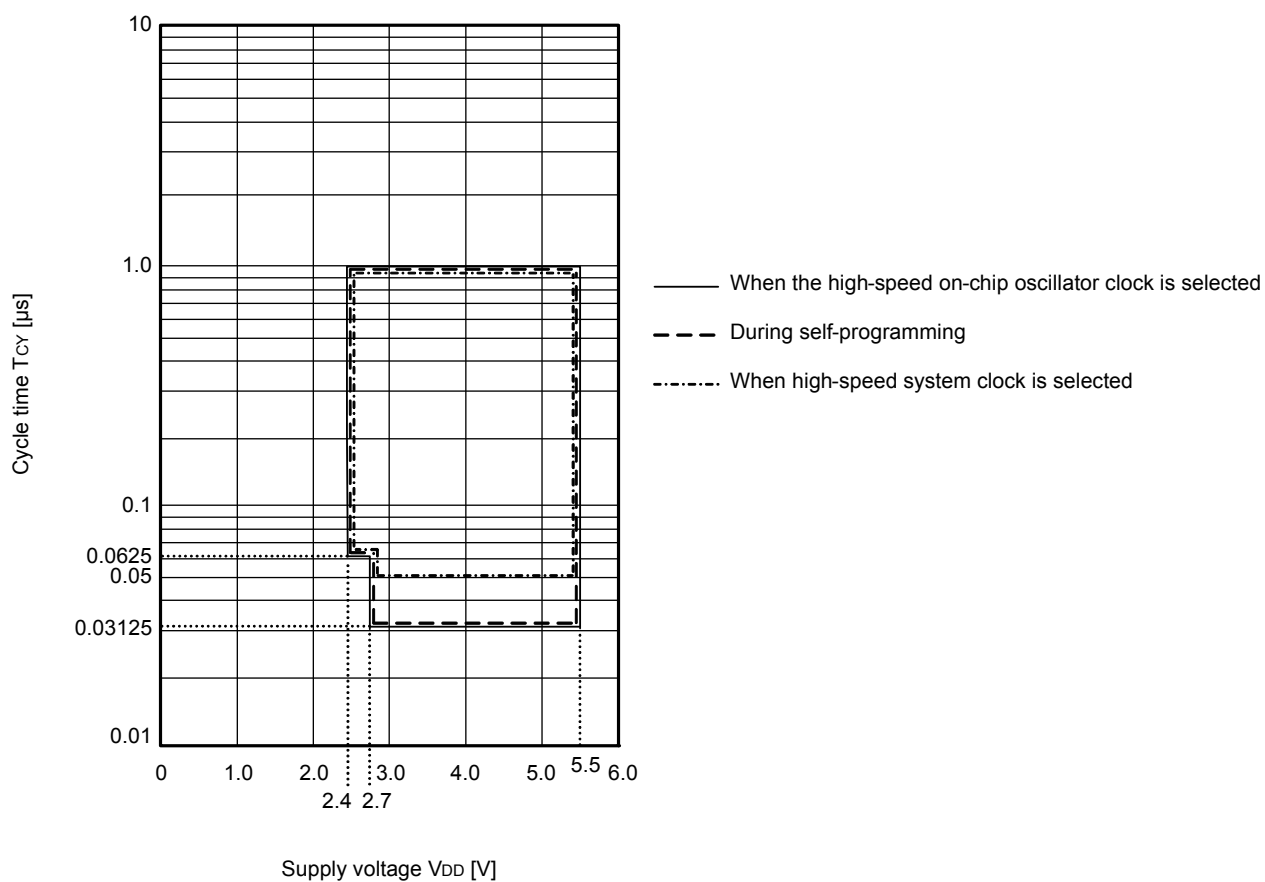
Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	Tstg			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Note 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- |                             |   |
|-----------------------------|---|
| HS (high-speed main) mode:  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz |
|                             | 2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode:   | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz  |
| LV (low-voltage main) mode: | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz  |
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f<sub>HOCO</sub>: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f<sub>IH</sub>: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

## Minimum Instruction Execution Time during Main System Clock Operation

T<sub>CY</sub> vs V<sub>DD</sub> (HS (high-speed main) mode)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)****(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
									Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	fMCK/6 Notes 1, 2, 3		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** Use it with EVDD0 ≥ Vb.**Note 3.** The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 &lt; 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 &lt; 2.4 V: MAX. 1.3 Mbps

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Vb [V]: Communication line voltage**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

**Note 4.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use it with  $EV_{DD0} \geq V_b$ .

**Note 6.** The smaller maximum transfer rate derived by using  $f_{mck}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 7.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 30- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

## 3.2 Oscillator Characteristics

### 3.2.1 X1, XT1 characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency ( $f_X$ ) <sup>Note</sup>	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	
XT1 clock oscillation frequency ( $f_{XT1}$ ) <sup>Note</sup>	Crystal resonator		32	32.768	35	kHz

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time.  
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

### 3.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	$f_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		+1.0	%
		-40 to $-20^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
		$+85$ to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	$f_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0.8 EVDD0		EVDD0	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2	EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0	EVDD0	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	1.5	EVDD0	V
	V <sub>IH3</sub>	P20 to P27, P150 to P156	0.7 VDD		VDD	V
	V <sub>IH4</sub>	P60 to P63	0.7 EVDD0		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8 VDD		VDD	V
Input voltage, low	V <sub>IL1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0		0.2 EVDD0	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	0	0.32	V
	V <sub>IL3</sub>	P20 to P27, P150 to P156	0		0.3 VDD	V
	V <sub>IL4</sub>	P60 to P63	0		0.3 EVDD0	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2 VDD	V

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

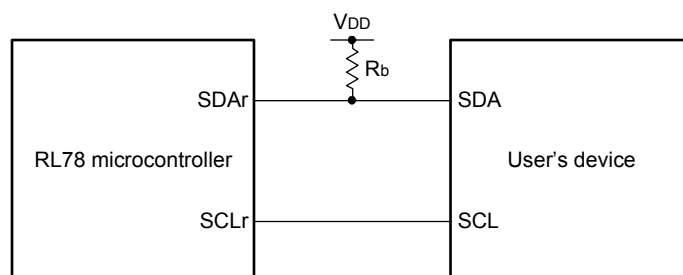
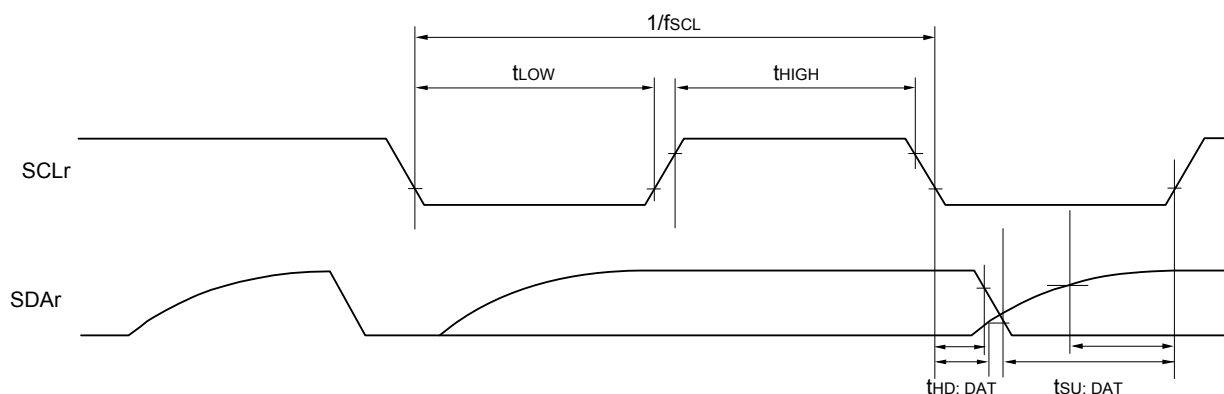


## (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.6	mA
						VDD = 3.0 V		2.6	
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.3	
						VDD = 3.0 V		2.3	
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.4	mA
						VDD = 3.0 V		5.4	
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.0	
						VDD = 3.0 V		5.0	
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.2	
						VDD = 3.0 V		4.2	
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	
						VDD = 3.0 V		4.0	
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		3.0	
						VDD = 3.0 V		3.0	
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.4	mA
						Resonator connection		3.6	
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.4	
						Resonator connection		3.6	
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.1	
						Resonator connection		2.2	
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.1	
						Resonator connection		2.2	
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.9	μA
						Resonator connection		4.9	
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.9	
						Resonator connection		4.9	
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.1	
						Resonator connection		5.1	
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.5	
						Resonator connection		5.5	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.5	
						Resonator connection		6.5	
				fSUB = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		13.0	
						Resonator connection		13.0	

(Notes and Remarks are listed on the next page.)

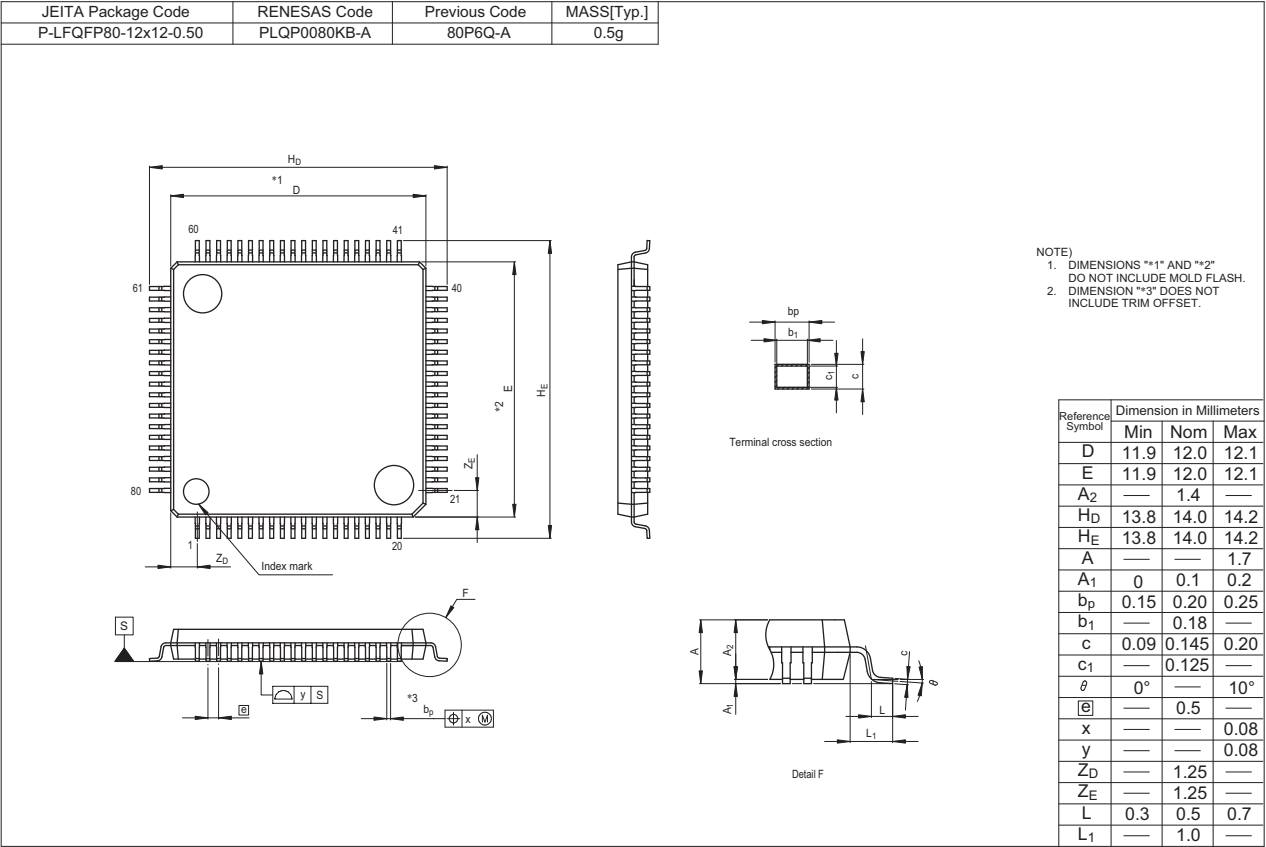
**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**

**Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance

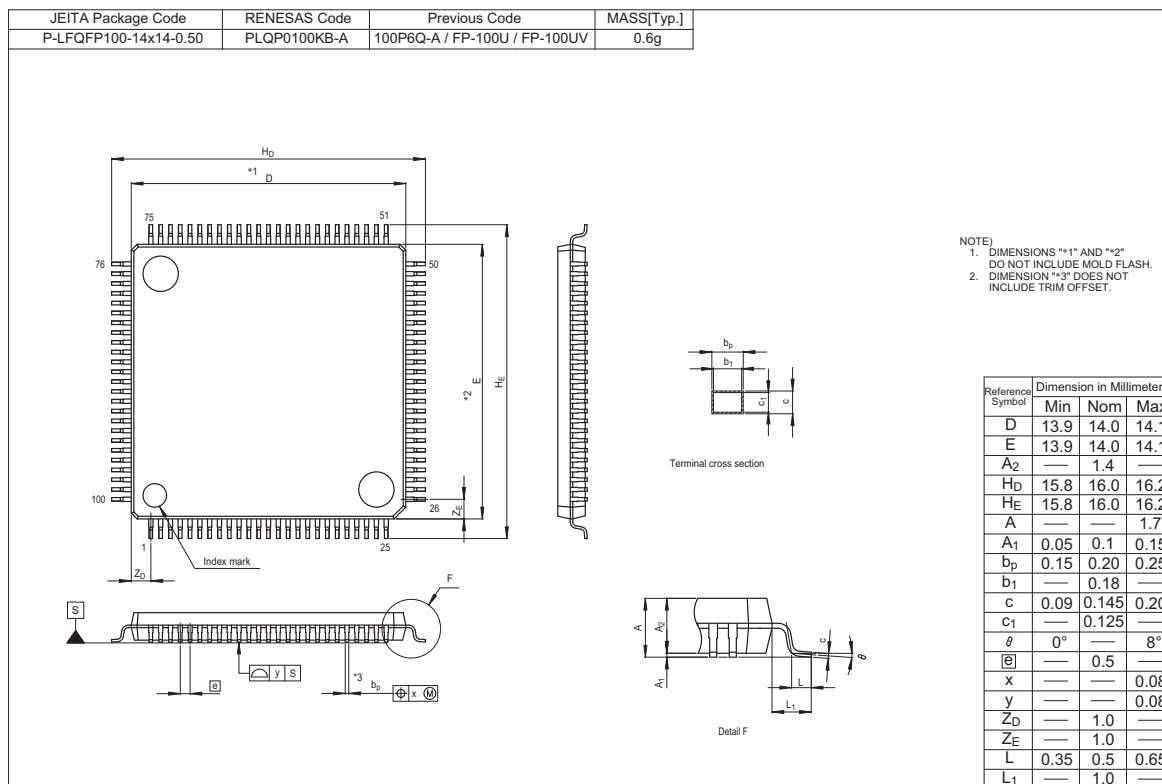
**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),  
h: POM number (h = 0, 1, 3 to 5, 7, 14)

**Remark 3.**  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

R5F104MKAFB, R5F104MLAFB  
R5F104MKGFB, R5F104MLGFB



R5F104PKAFB, R5F104PLAFB  
R5F104PKGFB, R5F104PLGFB



## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.