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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

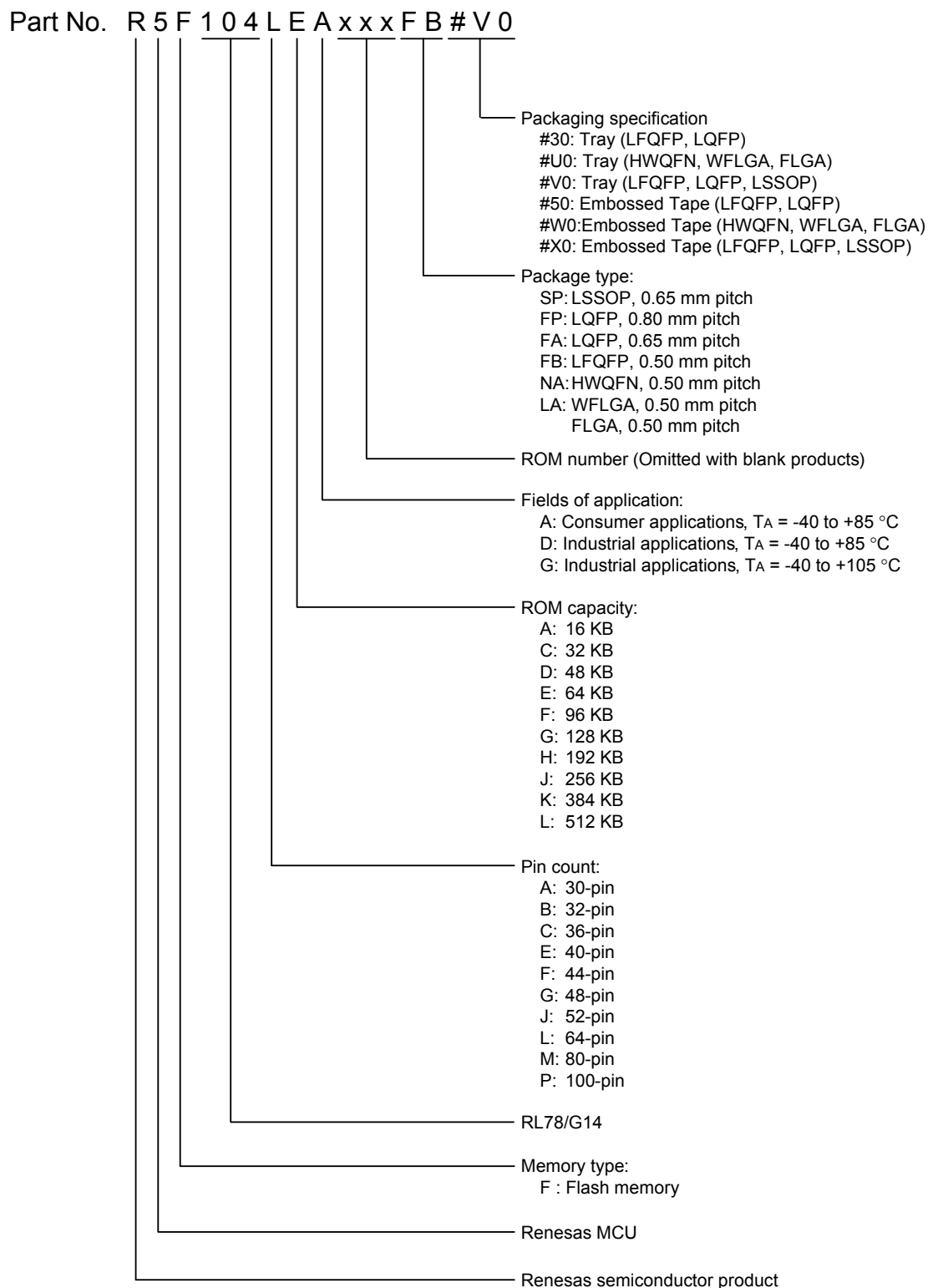
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104glafb-30

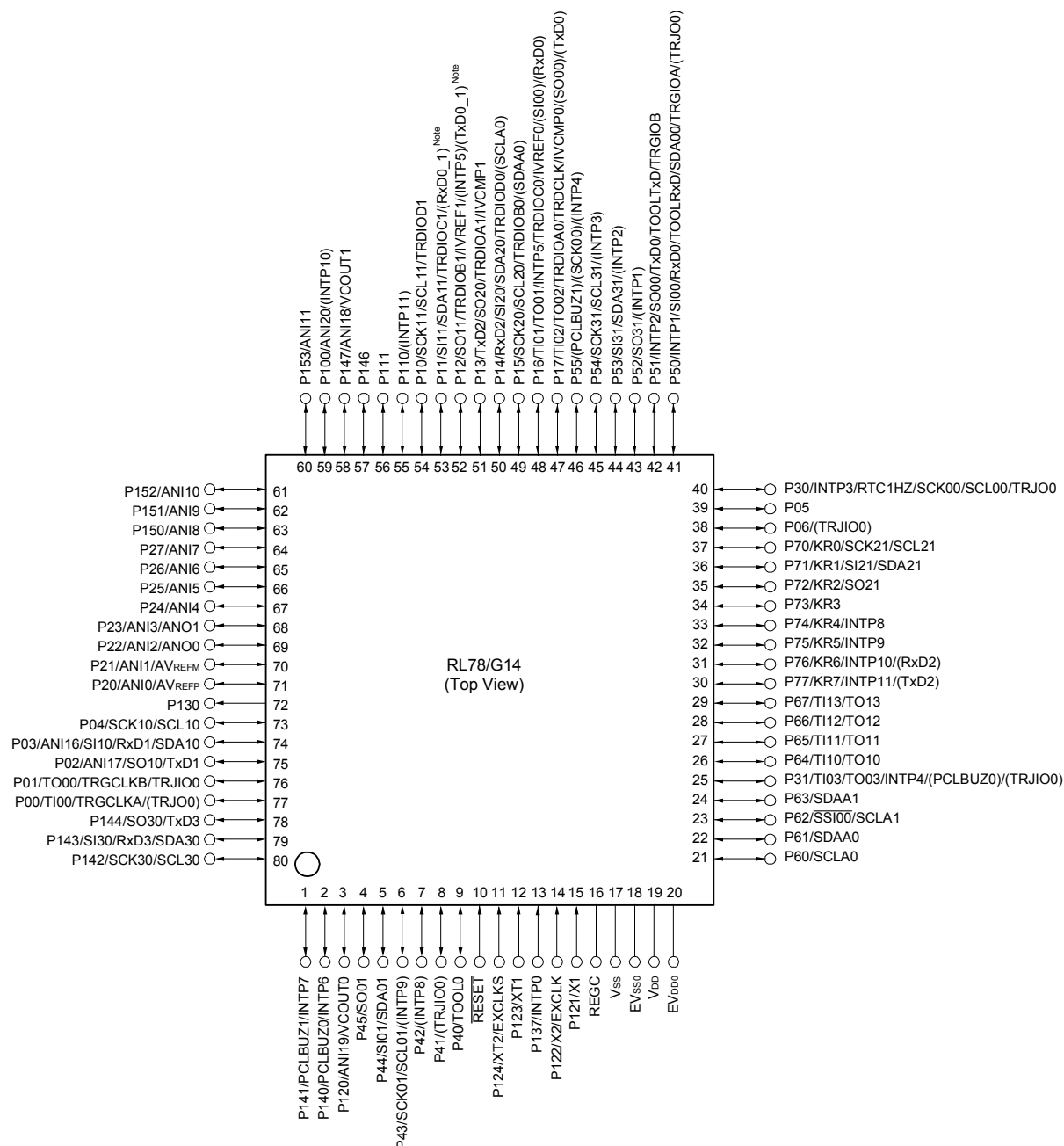
1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14



1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

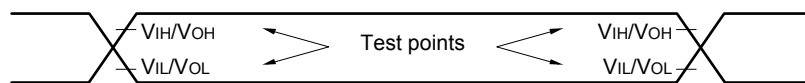
- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|-------------------------------------|
| HS (high-speed main) mode: | 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ VDD ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ VDD ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

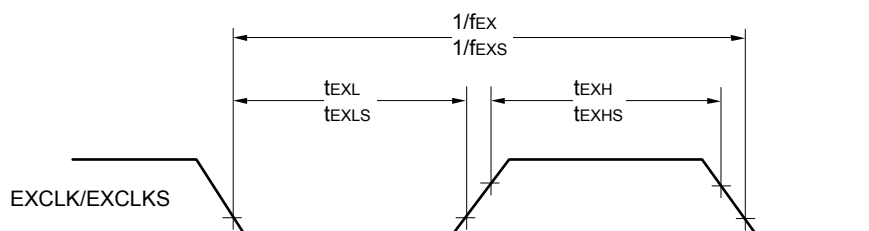
(2/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	2MHz < fCLK ≤ 32 MHz	1			μs
			fCLK ≤ 2 MHz	1/fCLK + 1			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		2.5/fCLK			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	1.6 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11	1.6 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
			1.6 V ≤ EVDD0 < 1.8 V	1			μs
RESET low-level width	tRSL			10			μs

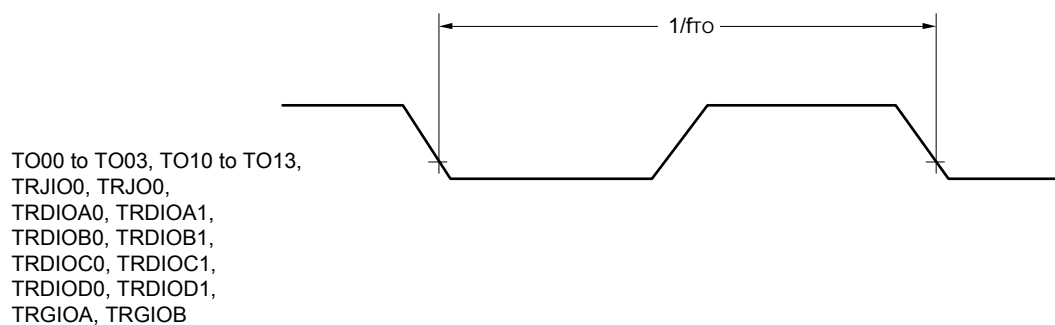
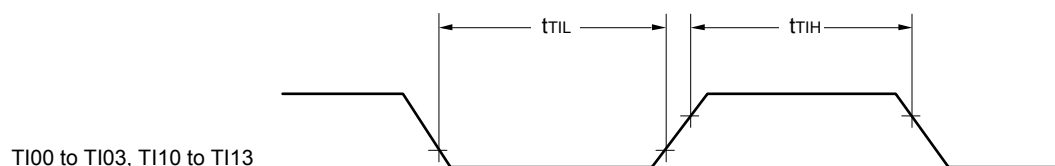
AC Timing Test Points



External System Clock Timing



TI/TO Timing



(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V			2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V			1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V			0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8 \text{ V} \leq EV_{DD0} < 3.3 \text{ V}$ and $1.6 \text{ V} \leq V_b \leq 2.0 \text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		200		1150		1150		ns
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 - 120		t _{KCY1} /2 - 120		t _{KCY1} /2 - 120		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 - 7		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 - 10		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		121		479		479		ns
Slp hold time (from SCKp↑) Note 1	t _{KSI1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp out- put Note 1	t _{KSO1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns

Note Use it with EVDD0 ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/3)**

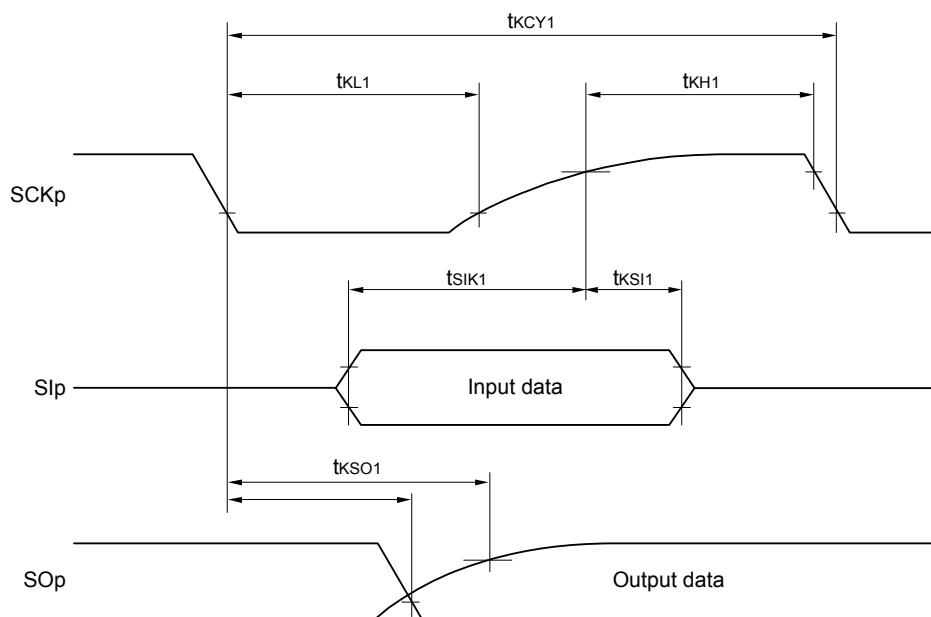
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** Use it with EVDD0 ≥ Vb.

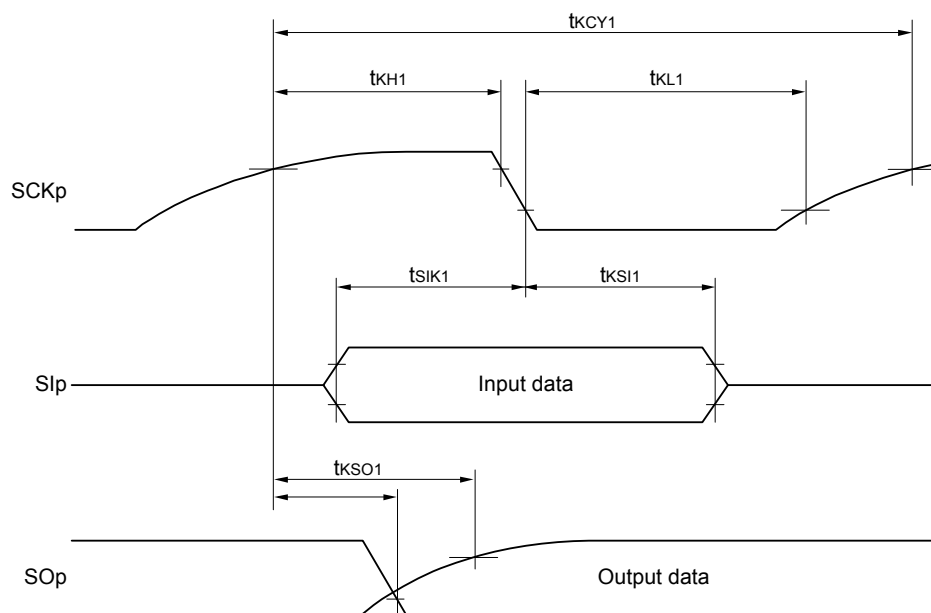
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0.8 EVDD0		EVDD0	V
	V _{IH2}	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2	EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0	EVDD0	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	1.5	EVDD0	V
	V _{IH3}	P20 to P27, P150 to P156	0.7 VDD		VDD	V
	V _{IH4}	P60 to P63	0.7 EVDD0		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8 VDD		VDD	V
Input voltage, low	V _{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	0		0.2 EVDD0	V
	V _{IL2}	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P27, P150 to P156	0		0.3 VDD	V
	V _{IL4}	P60 to P63	0		0.3 EVDD0	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2 VDD	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

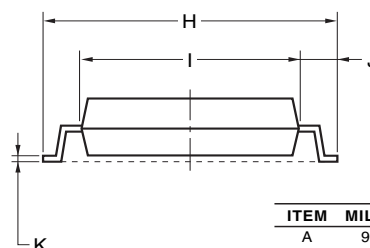
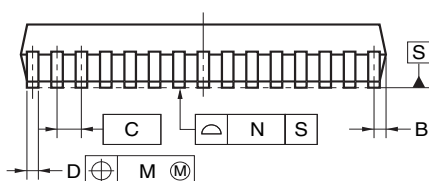
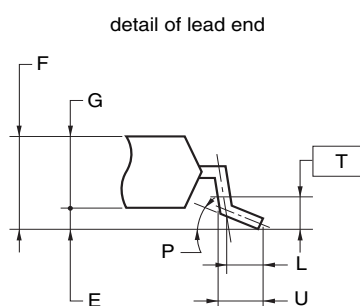
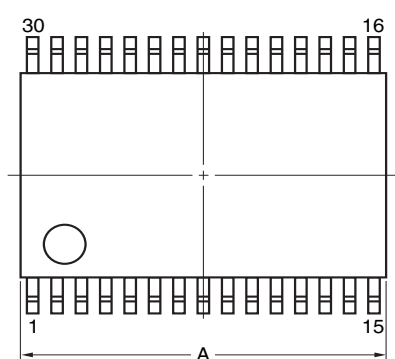
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	$2\text{ MHz} < f_{\text{CLK}} \leq 32\text{ MHz}$	1			μs
			$f_{\text{CLK}} \leq 2\text{ MHz}$	$1/f_{\text{CLK}} + 1$			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		$2.5/f_{\text{CLK}}$			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	1			μs
		INTP1 to INTP11	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250			ns
$\overline{\text{RESET}}$ low-level width	tRSL			10			μs

4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
 R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
 R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

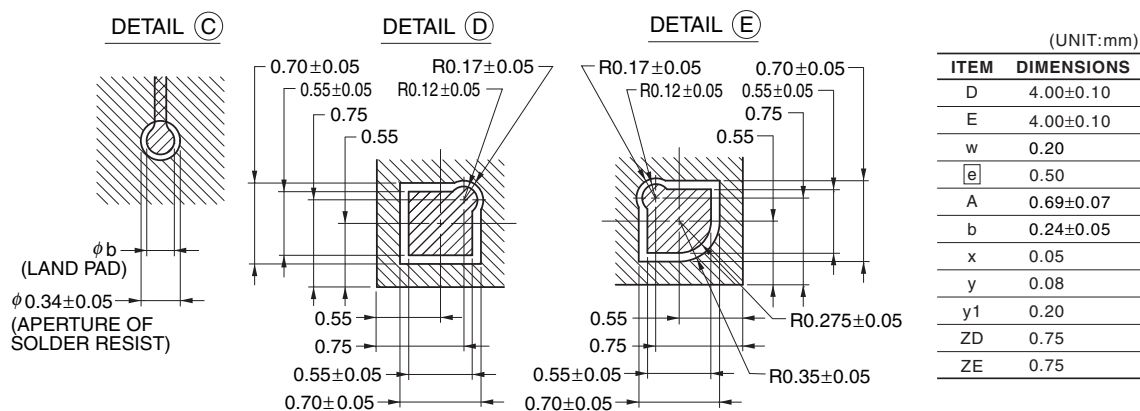
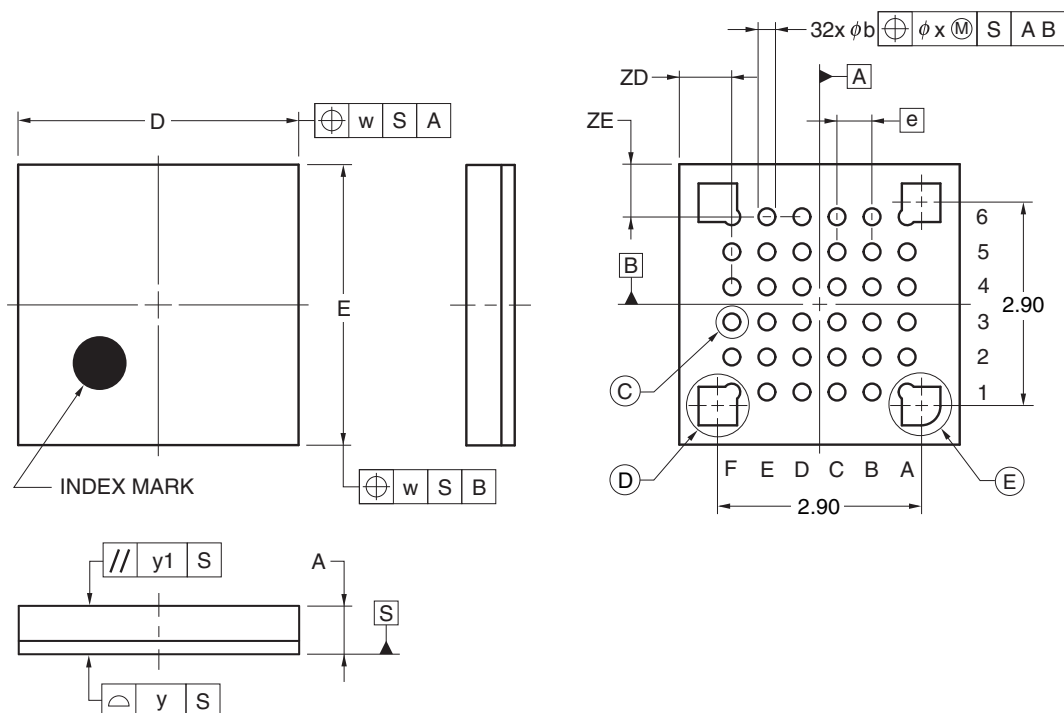
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

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4.3 36-pin products

R5F104CAALA, R5F104CCALA, R5F104CDALA, R5F104CEALA, R5F104CFALA, R5F104CGALA
R5F104CAGLA, R5F104CCGLA, R5F104CDGLA, R5F104CEGLA, R5F104CFGLA, R5F104CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

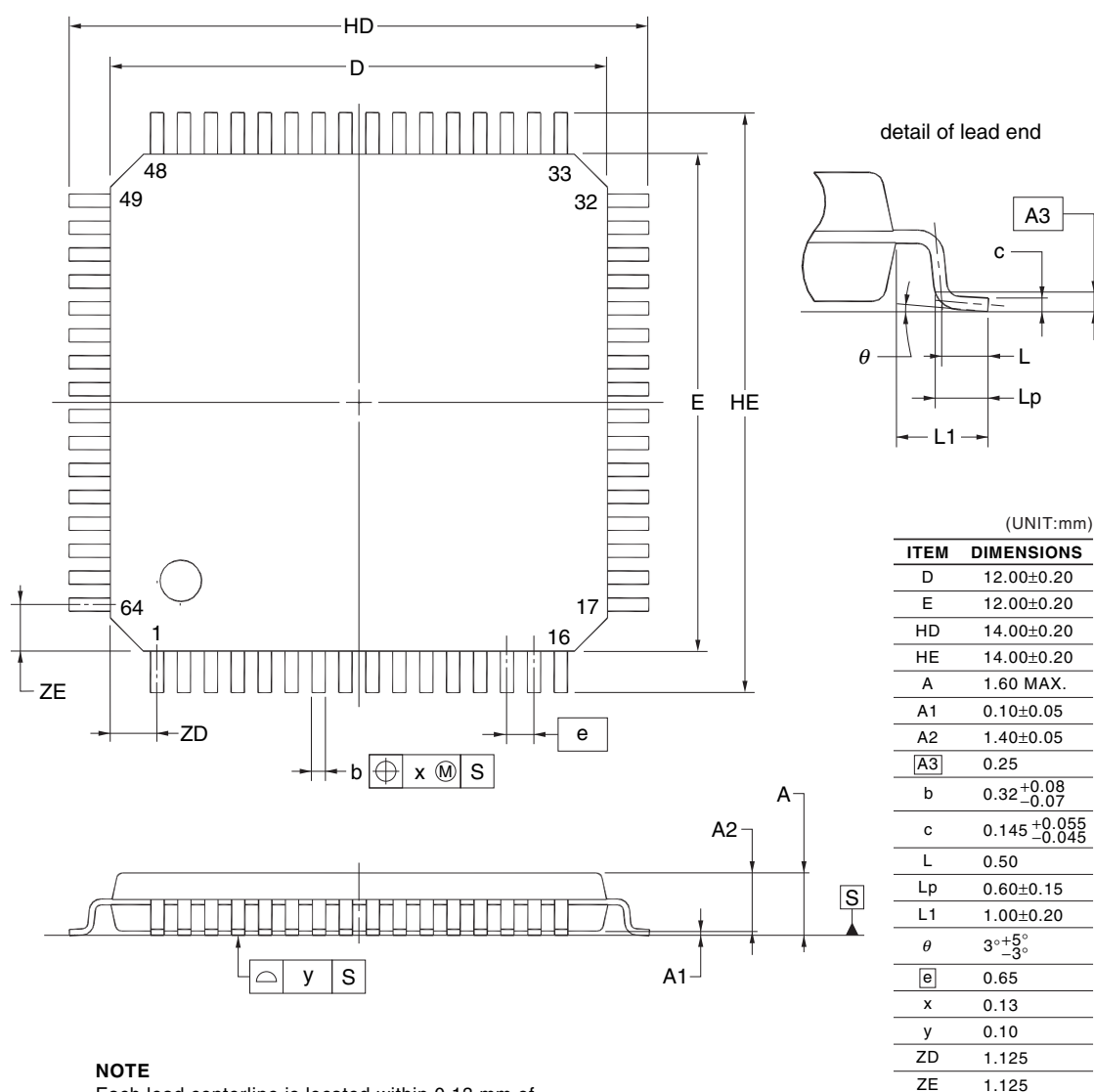


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4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFa, R5F104LHAFA, R5F104LJAFA
 R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFa, R5F104LHDFa, R5F104LJDFA
 R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
 R5F104LKAFA, R5F104LLAFA
 R5F104LKGFA, R5F104LLGFA

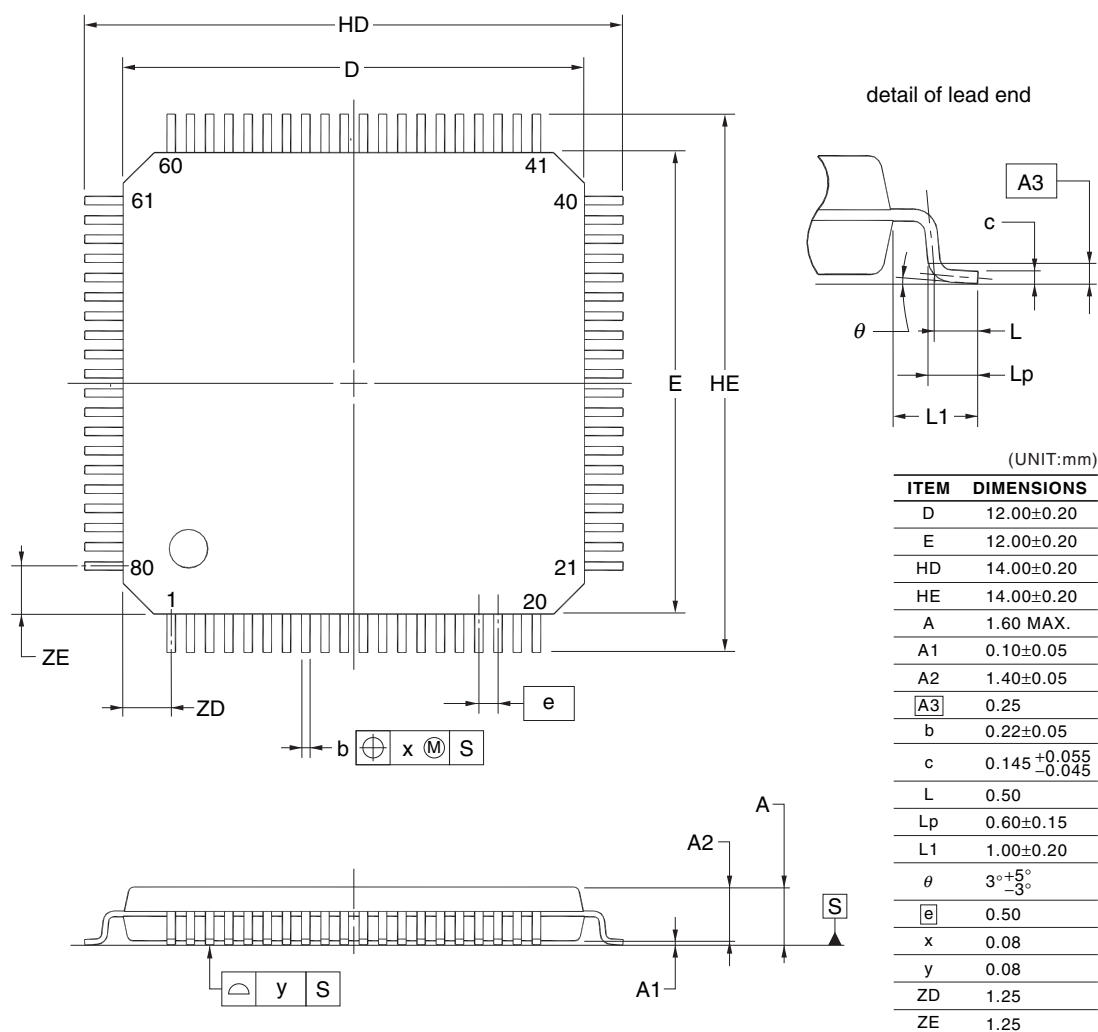
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



4.9 80-pin products

R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
 R5F104MDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
 R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

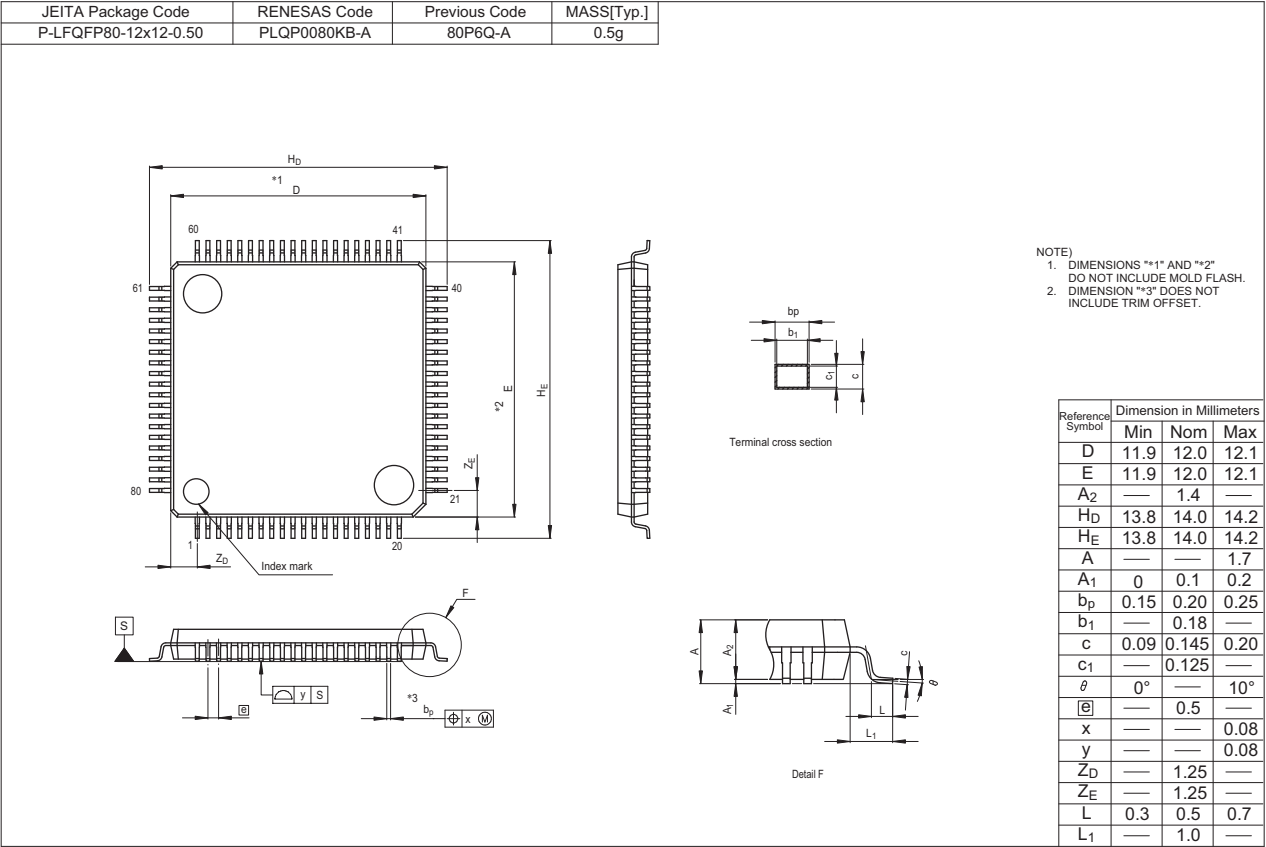
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



NOTE

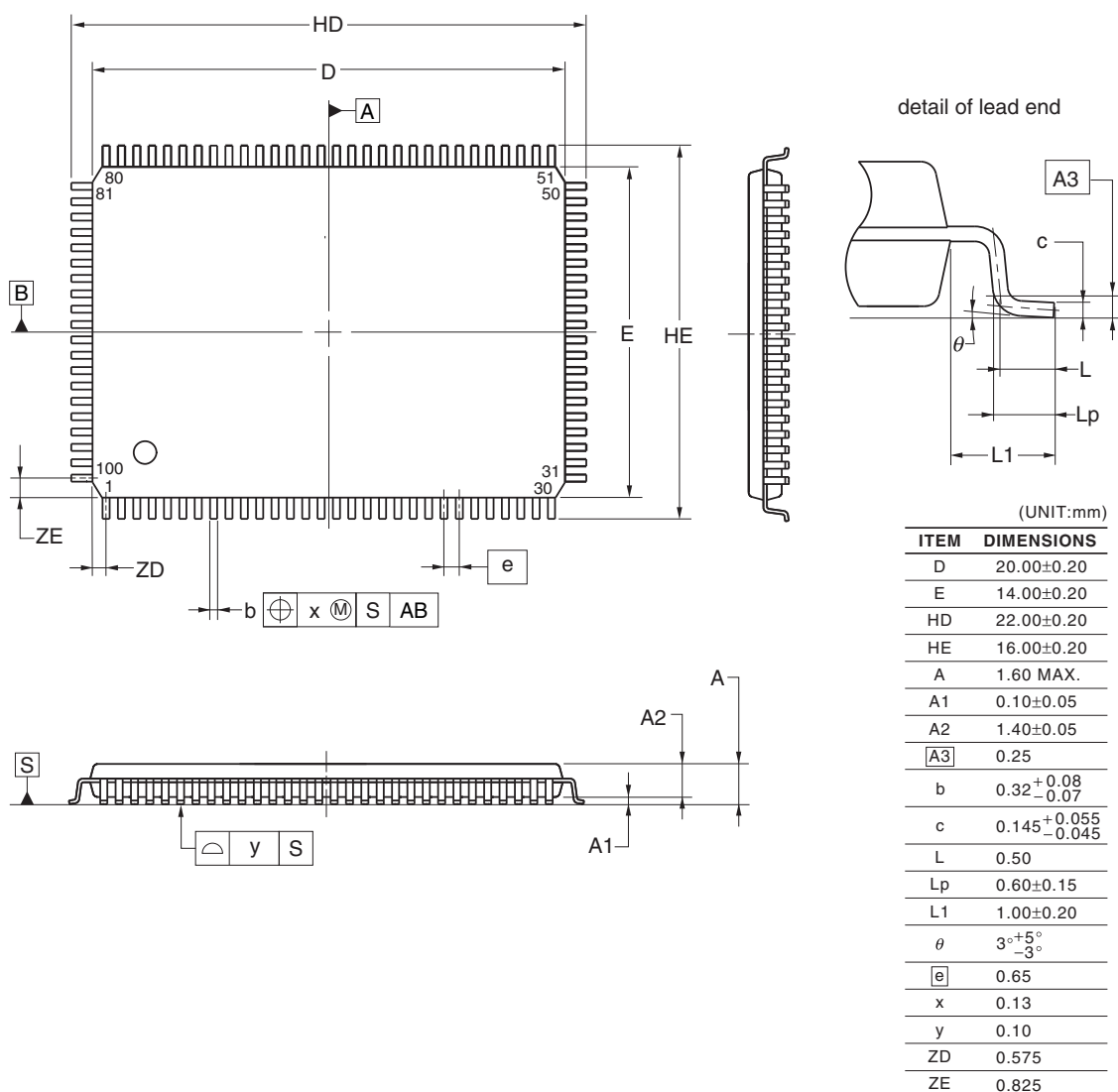
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB



R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJFAFA
 R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFA
 R5F104PFGFA, R5F104PGGFA, R5F104PHGFA, R5F104PJGFA
 R5F104PKAFA, R5F104PLAFA
 R5F104PKGFA, R5F104PLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



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REVISION HISTORY	RL78/G14 Datasheet
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Rev.	Date	Description	
		Page	Summary
2.00	Oct 25, 2013	112 to 169 171 to 187	Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS Modification of 4.1 30-pin products to 4.10 100-pin products
3.00	Feb 07, 2014	All 1 2 3 6 to 8 15, 16 17 18, 19 20 21, 22 35, 37, 39, 41, 43, 45, 47 42, 43 46, 47 65 to 68 118 137 to 140 180 189, 190 191 193 to 195 198, 199 201, 202	Addition of products with maximum 512 KB flash ROM and 48 KB RAM Modification of 1.1 Features Modification of ROM, RAM capacities and addition of note 3 Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14 Addition of part number Modification of 1.3.6 48-pin products Modification of 1.3.7 52-pin products Modification of 1.3.8 64-pin products Modification of 1.3.9 80-pin products Modification of 1.3.10 100-pin products Modification of operating ambient temperature in 1.6 Outline of Functions Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB) Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB) Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products Modification of 2.7 Data Memory Retention Characteristics Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products Modification of 3.7 Data Memory Retention Characteristics Addition and modification of 4.6 48-pin products Modification of 4.7 52-pin products Addition and modification of 4.8 64-pin products Addition and modification of 4.9 80-pin products Addition and modification of 4.10 100-pin products
3.20	Jan 05, 2015	p.2 p.6 p.6 to 8 p.17 p.36, 39, 42, 45, 48, 50, 52 p.46, 48 p.47 p.62, 64, 66, 68, 70, 72	Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information Deletion of note 2 in 1.2 Ordering Information Deletion of note 2 in 1.3.7 52-pin products Modification of description in 1.6 Outline of Functions Deletion of description of 52-pin in 1.6 Outline of Functions Modification of note of 1.6 Outline of Functions Modification of specifications in 2.3.2 Supply current characteristics