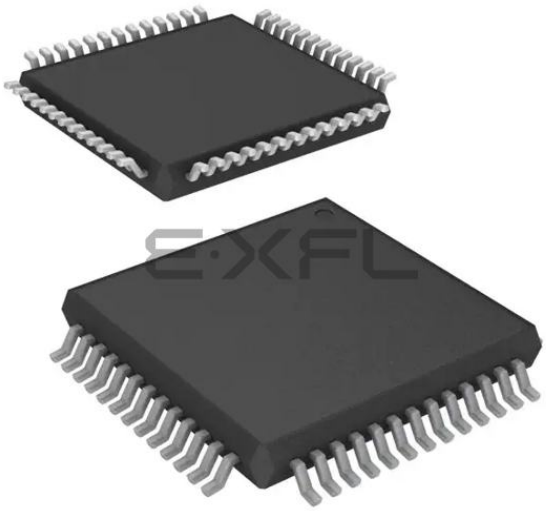
# Renesas Electronics America Inc - R5F104JEGFA#V0 Datasheet



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## What is "Embedded - Microcontrollers"?

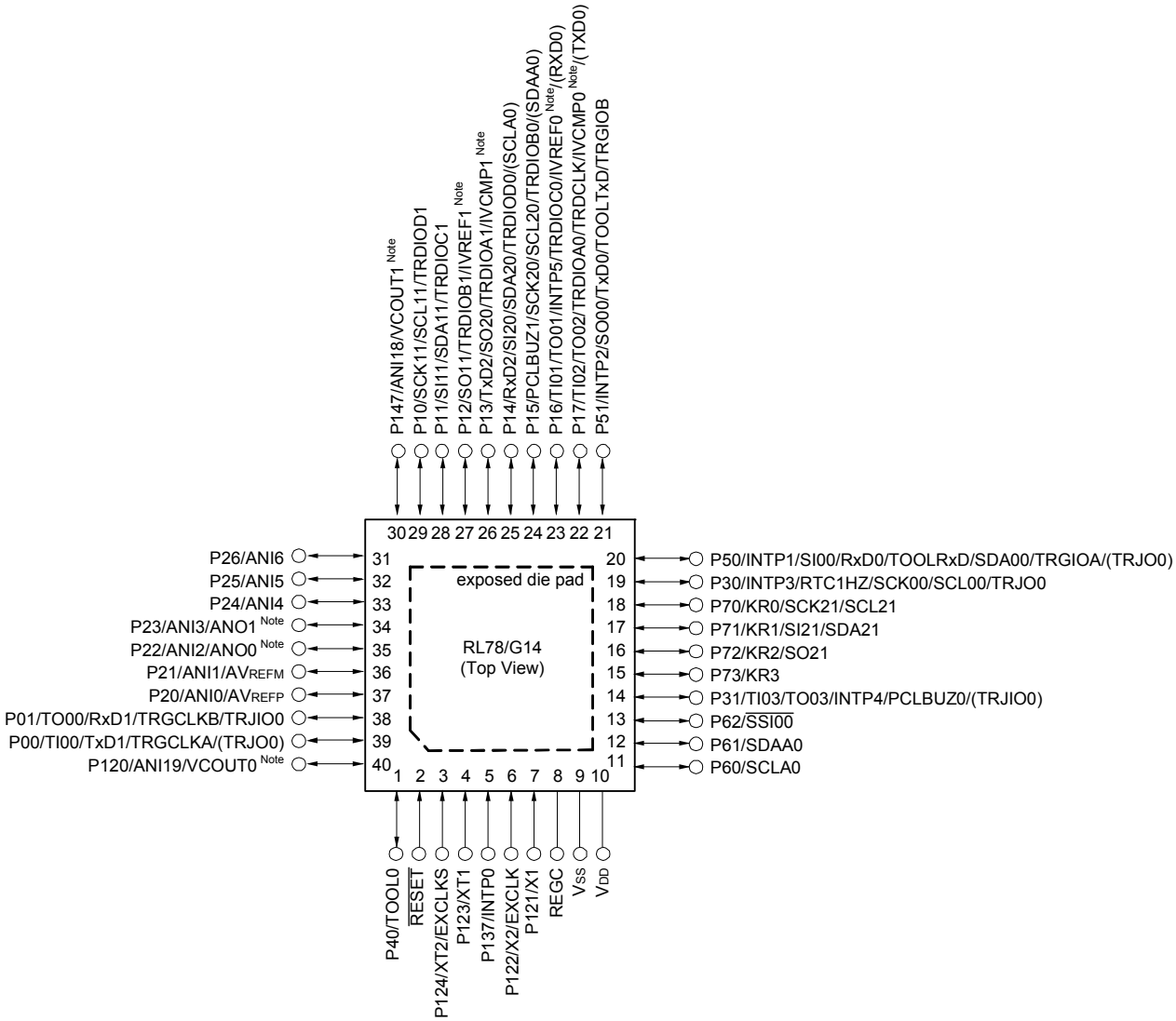
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 5.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104jegfa-v0 |

### 1.3.4 40-pin products

• 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

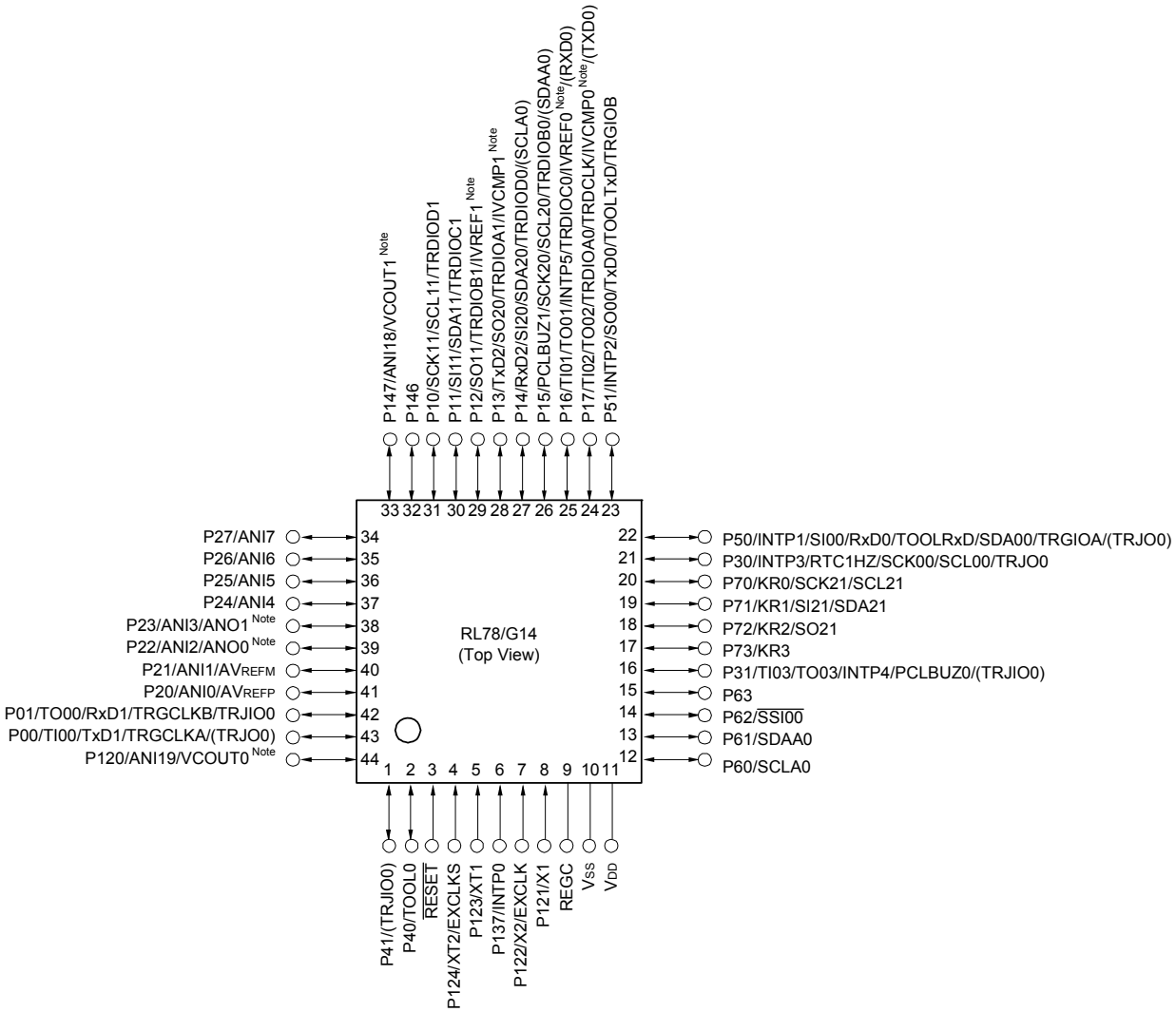
**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

### 1.3.5 44-pin products

• 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

(2/2)

| Item | | 48-pin<br>R5F104Gx<br>(x = K, L) | 64-pin<br>R5F104Lx<br>(x = K, L) |
|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br>(Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br>(Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/10-bit resolution A/D converter | | 10 channels | 12 channels |
| D/A converter | | 2 channels | |
| Comparator | | 2 channels | |
| Serial interface | | [48-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[64-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | |
| | $I^2C$ bus | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 32 sources | 33 sources |
| Event link controller (ELC) | | Event input: 22<br>Event trigger output: 9 | |
| Vectored interrupt sources | Internal | 24 | 24 |
| | External | 10 | 13 |
| Key interrupt | | 6 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | |
| On-chip debug function | | Provided | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.57 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.57 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.00 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.00 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 1.49 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 1.49 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 250 | 800 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 250 | 800 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 755 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 755 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 1.63 | mA |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 1.63 | |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 580 | µA |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 580 | |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.28 | 0.66 | µA |
| | | | | | Resonator connection | | 0.47 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.34 | 0.66 | |
| | | | | | Resonator connection | | 0.53 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.37 | 2.35 | |
| | | | | | Resonator connection | | 0.56 | 2.54 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.61 | 4.08 | |
| | | | | | Resonator connection | | 0.80 | 4.27 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.55 | 8.09 | |
| | | | | | Resonator connection | | 1.74 | 8.28 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.57 | µA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |

(**Notes** and **Remarks** are listed on the next page.)

## 2.4 AC Characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

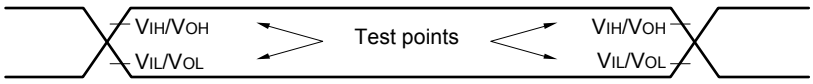
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03, TI10 to TI13 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 500 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 200 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
1.8 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MIN. 250 ns

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

## 2.5 Peripheral Functions Characteristics

AC Timing Test Points




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | — | | | 1.3 | | 0.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MAX. 0.6 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

### (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 38 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | — | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

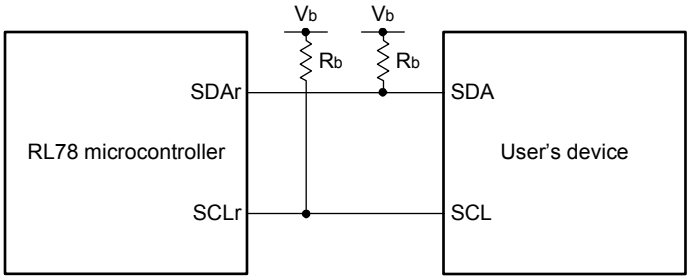
### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

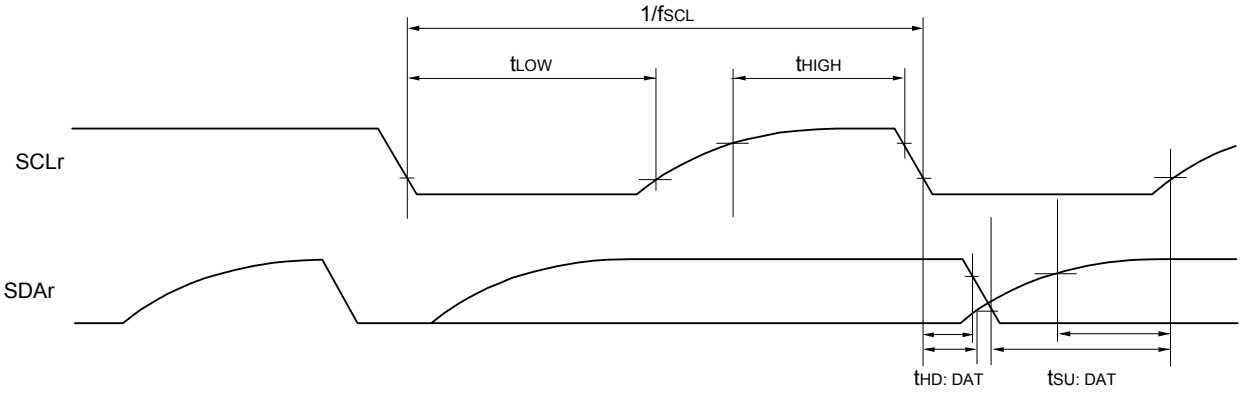
| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 7 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | | 60 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | | 130 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

## 2.6.6 LVD circuit characteristics

### (1) Reset Mode and Interrupt Mode

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.98 | 4.06 | 4.14 | V |
| | | | Falling edge | 3.90 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | Rising edge | 3.68 | 3.75 | 3.82 | V |
| | | | Falling edge | 3.60 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | Rising edge | 3.07 | 3.13 | 3.19 | V |
| | | | Falling edge | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Rising edge | 2.96 | 3.02 | 3.08 | V |
| | | | Falling edge | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Rising edge | 2.86 | 2.92 | 2.97 | V |
| | | | Falling edge | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Rising edge | 2.76 | 2.81 | 2.87 | V |
| | | | Falling edge | 2.70 | 2.75 | 2.81 | V |
| | | $V_{LVD6}$ | Rising edge | 2.66 | 2.71 | 2.76 | V |
| | | | Falling edge | 2.60 | 2.65 | 2.70 | V |
| | | $V_{LVD7}$ | Rising edge | 2.56 | 2.61 | 2.66 | V |
| | | | Falling edge | 2.50 | 2.55 | 2.60 | V |
| | | $V_{LVD8}$ | Rising edge | 2.45 | 2.50 | 2.55 | V |
| | | | Falling edge | 2.40 | 2.45 | 2.50 | V |
| | | $V_{LVD9}$ | Rising edge | 2.05 | 2.09 | 2.13 | V |
| | | | Falling edge | 2.00 | 2.04 | 2.08 | V |
| | | $V_{LVD10}$ | Rising edge | 1.94 | 1.98 | 2.02 | V |
| | | | Falling edge | 1.90 | 1.94 | 1.98 | V |
| | | $V_{LVD11}$ | Rising edge | 1.84 | 1.88 | 1.91 | V |
| | | | Falling edge | 1.80 | 1.84 | 1.87 | V |
| | | $V_{LVD12}$ | Rising edge | 1.74 | 1.77 | 1.81 | V |
| | | | Falling edge | 1.70 | 1.73 | 1.77 | V |
| | | $V_{LVD13}$ | Rising edge | 1.64 | 1.67 | 1.70 | V |
| | | | Falling edge | 1.60 | 1.63 | 1.66 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = -40 to +105°C

R5F104xxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.**

**Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When RL78/G14 is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

<R>

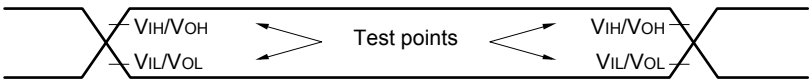
### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

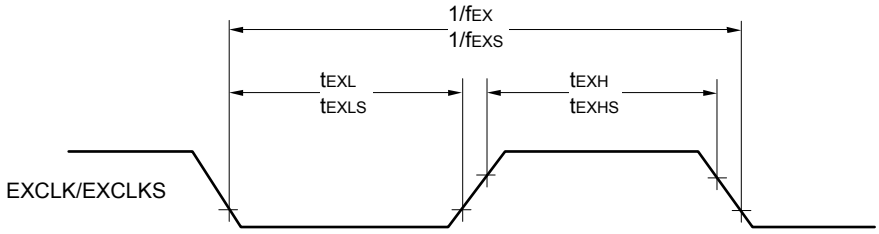
| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 5.16 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 5.16 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 4.47 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 4.47 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 4.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 4.08 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 3.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 3.51 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 2.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 2.38 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.83 | mA |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.83 | |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.31 | 0.76 | µA |
| | | | | | Resonator connection | | 0.50 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.38 | 0.76 | |
| | | | | | Resonator connection | | 0.57 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.47 | 3.59 | |
| | | | | | Resonator connection | | 0.70 | 3.78 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.80 | 6.20 | |
| | | | | | Resonator connection | | 1.00 | 6.39 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.65 | 10.56 | |
| | | | | | Resonator connection | | 1.84 | 10.75 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 8.00 | 65.7 | |
| | | | | | Resonator connection | | 8.00 | 65.7 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.63 | µA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.63 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.47 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.08 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.44 | |
| | | | $T_A$ = +105°C | | | | 6.50 | 67.14 | |

(**Notes** and **Remarks** are listed on the next page.)

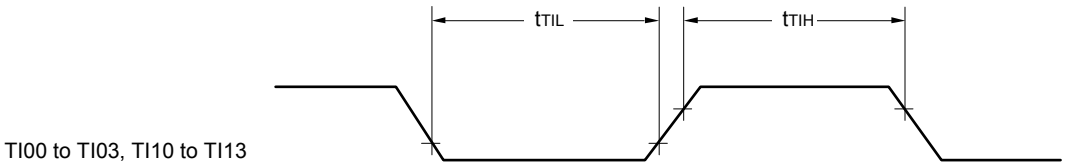
AC Timing Test Points

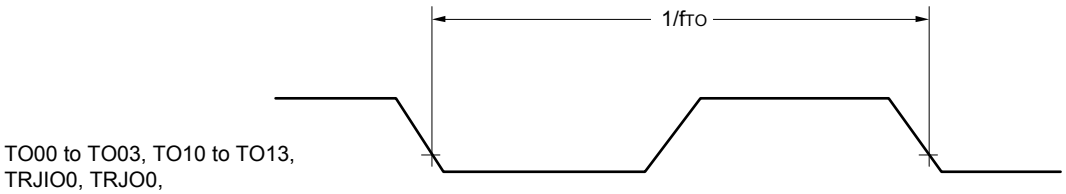



External System Clock Timing




TI/TO Timing



**(2) Interrupt & Reset Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Voltage detection threshold | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

## 3.6.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

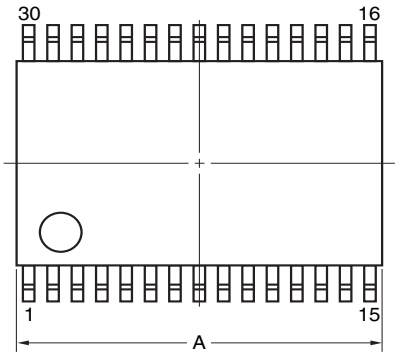
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

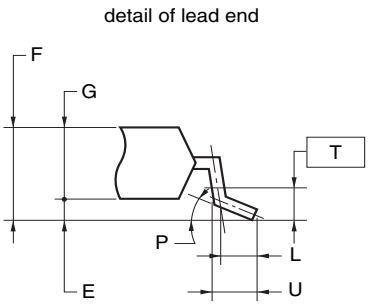
# 4. PACKAGE DRAWINGS

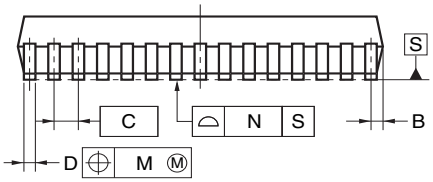
## 4.1 30-pin products

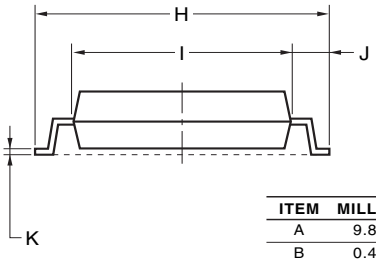
R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |



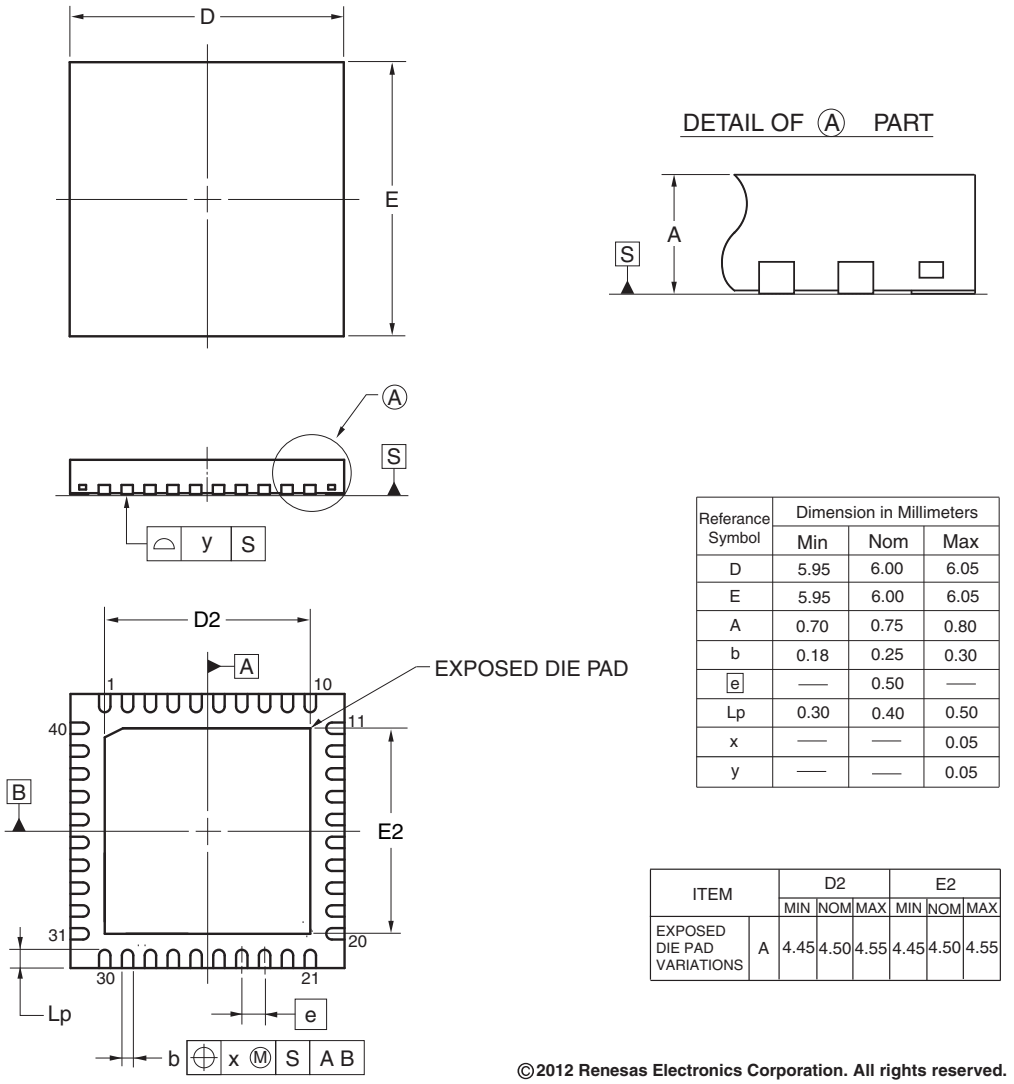

**NOTE**
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

## 4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA
R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA
R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA, R5F104EHGNA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-4 | 0.09 |



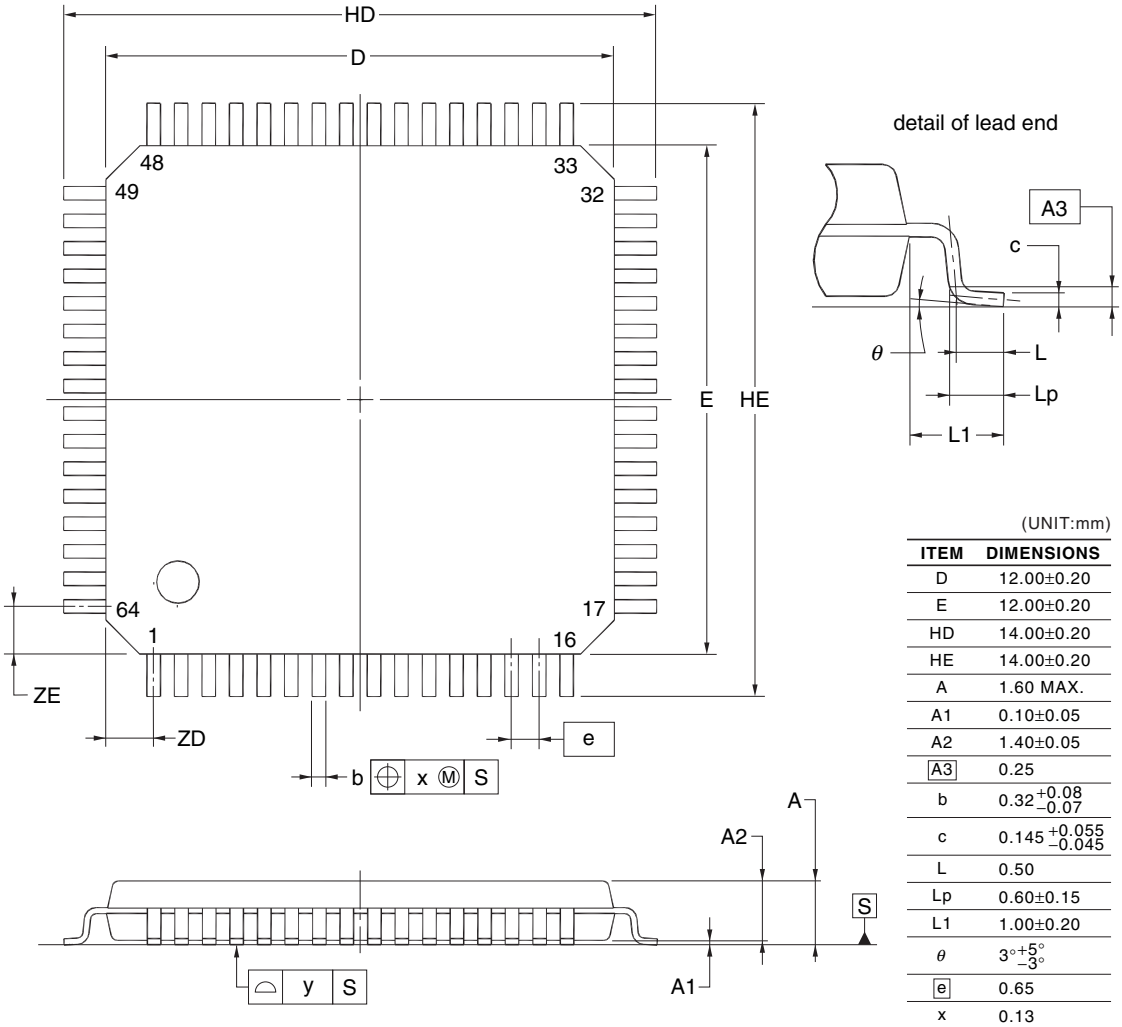

| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 4.45 | 4.50 | 4.55 | 4.45 | 4.50 | 4.55 |

## 4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFA, R5F104LHAFA, R5F104LJAFA
R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFA, R5F104LHDFA, R5F104LJDFA
R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
R5F104LKAFA, R5F104LLAFA
R5F104LKGFA, R5F104LLGFA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP64-12x12-0.65 | PLQP0064JA-A | P64GK-65-UET-2 | 0.51 |



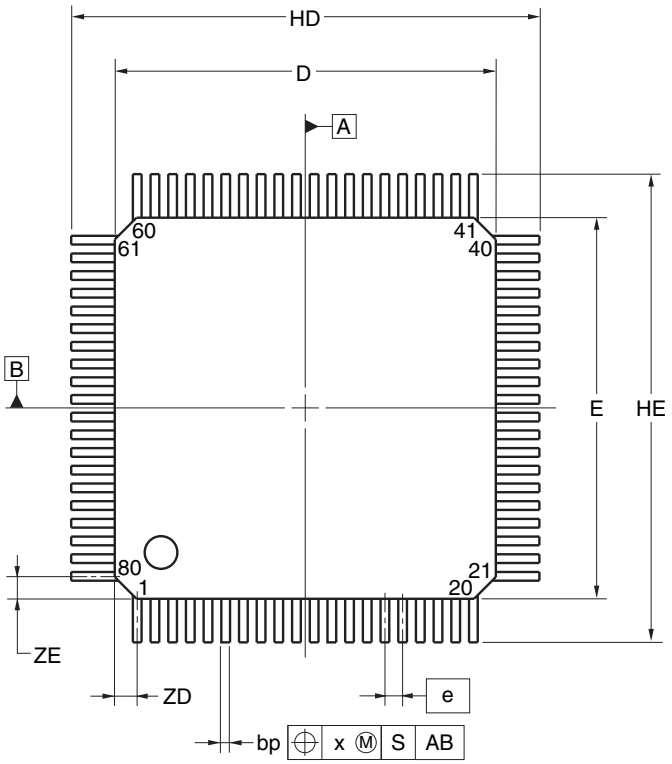

(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.32^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 1.125 |
| ZE | 1.125 |

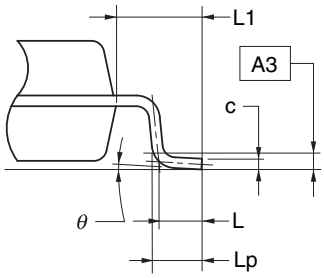
**NOTE**
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA
R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
R5F104MKAFA, R5F104MLAFA
R5F104MKGFA, R5F104MLGFA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JB-E | P80GC-65-UBT-2 | 0.69 |




detail of lead end




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.80 | 14.00 | 14.20 |
| E | 13.80 | 14.00 | 14.20 |
| HD | 17.00 | 17.20 | 17.40 |
| HE | 17.00 | 17.20 | 17.40 |
| A | — | — | 1.70 |
| A1 | 0.05 | 0.125 | 0.20 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | — | 0.25 | — |
| bp | 0.26 | 0.32 | 0.38 |
| c | 0.10 | 0.145 | 0.20 |
| L | — | 0.80 | — |
| Lp | 0.736 | 0.886 | 1.036 |
| L1 | 1.40 | 1.60 | 1.80 |
| θ | 0° | 3° | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| ZD | — | 0.825 | — |
| ZE | — | 0.825 | — |