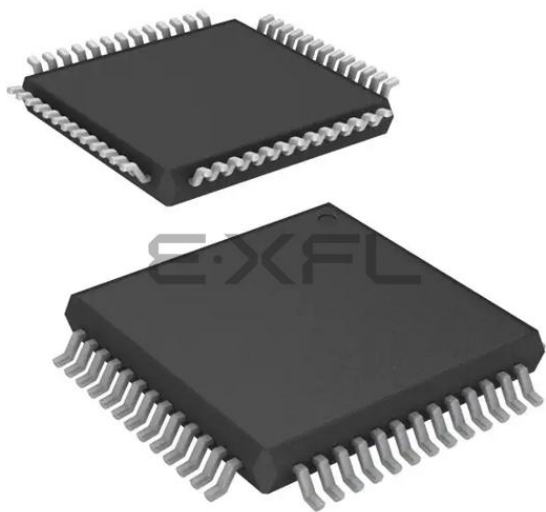




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104jggfa-30

(2/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	A	R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0 R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0
		D	R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0 R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0
		G	R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0 R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0
44 pins	44-pin plastic LQFP (10 × 10, 0.8 mm pitch)	A	R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0 R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0
		D	R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0 R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0
		G	R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0 R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

(4/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAFA#V0, R5F104LHAFA#V0, R5F104LJFAFA#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAFA#X0, R5F104LHAFA#X0, R5F104LJFAFA#X0 R5F104LKAFA#30, R5F104LLAFA#30 R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFFA#V0, R5F104LHDFFA#V0, R5F104LJDFFA#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFFA#X0, R5F104LHDFFA#X0, R5F104LJDFFA#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCA#U0, R5F104LDA#U0, R5F104LEA#U0, R5F104LFA#U0, R5F104LGA#U0, R5F104LHA#U0, R5F104LJA#U0 R5F104LCA#W0, R5F104LDA#W0, R5F104LEA#W0, R5F104LFA#W0, R5F104LGA#W0, R5F104LHA#W0, R5F104LJA#W0 R5F104LKA#U0, R5F104LLA#U0 R5F104LKA#W0, R5F104LLA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFLGA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFLGA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

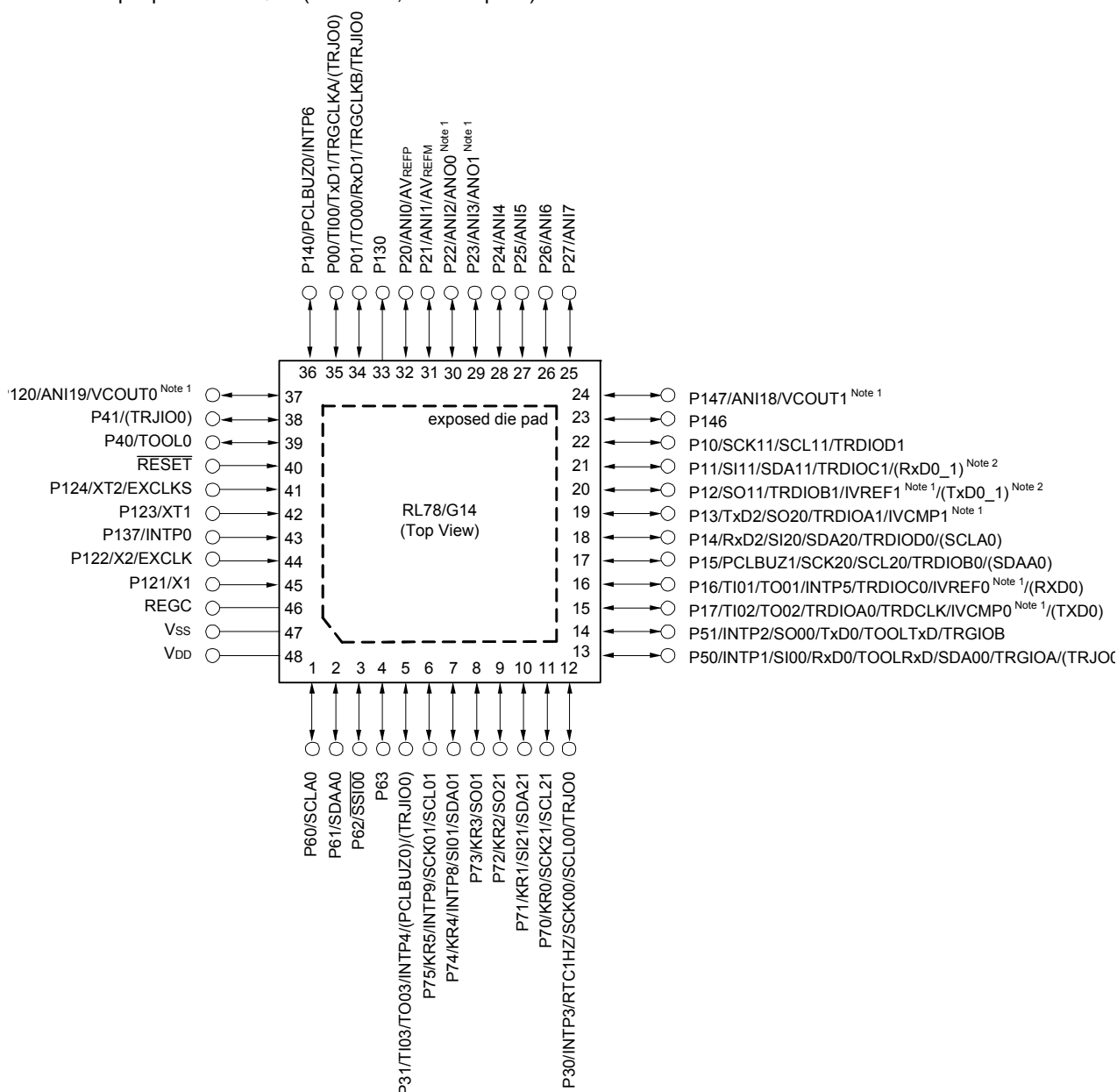
(5/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFA#V0, R5F104MJAFB#V0 R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFA#X0, R5F104MJAFB#X0 R5F104MKAFB#30, R5F104MLAFB#30 R5F104MKAFB#50, R5F104MLAFB#50
		D	R5F104MDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0 R5F104MDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0
		G	R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0 R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0 R5F104MKGFB#30, R5F104MLGFB#30 R5F104MKGFB#X0, R5F104MLGFB#50
	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	A	R5F104MFAFA#V0, R5F104MGFAFA#V0, R5F104MHAFA#V0, R5F104MJFAFA#V0 R5F104MFAFA#X0, R5F104MGFAFA#X0, R5F104MHAFA#X0, R5F104MJFAFA#X0 R5F104MKFAFA#30, R5F104MLFAFA#30 R5F104MKFAFA#50, R5F104MLFAFA#50
		D	R5F104MFDFA#V0, R5F104MGDFA#V0, R5F104MHDFB#V0, R5F104MJDFB#V0 R5F104MFDFA#X0, R5F104MGDFA#X0, R5F104MHDFB#X0, R5F104MJDFB#X0
		G	R5F104MFGFA#V0, R5F104MGGFA#V0, R5F104MHGFA#V0, R5F104MJGFA#V0 R5F104MFGFA#X0, R5F104MGGFA#X0, R5F104MHGFA#X0, R5F104MJGFA#X0 R5F104MKGFA#30, R5F104MLGFA#30 R5F104MKGFA#50, R5F104MLGFA#50
100 pins	100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F104PFAFB#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFB#V0 R5F104PFAFB#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFB#X0 R5F104PKAFB#30, R5F104PLAFB#30 R5F104PKAFB#50, R5F104PLAFB#50
		D	R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFB#V0 R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFB#X0
		G	R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0 R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0 R5F104PKGFB#30, R5F104PLGFB#30 R5F104PKGFB#50, R5F104PLGFB#50
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	A	R5F104PFAFA#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJFAFA#V0 R5F104PFAFA#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJFAFA#X0 R5F104PKFAFA#30, R5F104PLFAFA#30 R5F104PKFAFA#50, R5F104PLFAFA#50
		D	R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFB#V0 R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFB#X0
		G	R5F104PFGFA#V0, R5F104PGGFA#V0, R5F104PHGFA#V0, R5F104PJGFA#V0 R5F104PFGFA#X0, R5F104PGGFA#X0, R5F104PHGFA#X0, R5F104PJGFA#X0 R5F104PKGFA#30, R5F104PLGFA#30 R5F104PKGFA#50, R5F104PLGFA#50

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

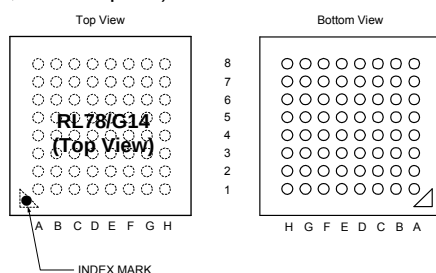
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

- 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)



	A	B	C	D	E	F	G	H	
8	EVDD0	EVSS0	P121/X1	P122/X2/ EXCLK	P137/INTP0	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ VCOUT0 Note 1	8
7	P60/SCLA0	VDD	VSS	REGC	RESET	P01/TO00/ TRGCLKB/ TRJIO0	P00/TIO0/ TRGCLKA/ (TRJIO0)	P140/ PCLBUZ0/ INTP6	7
6	P61/SDAA0	P62/SSI00	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/ SO10/TxD1	P141/ PCLBUZ1/ INTP7	6
5	P77/KR7/ INTP11/(TXD2)	P31/TIO3/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AVREFP	5
4	P75/KR5/ INTP9/ SCK01/ SCL01	P76/KR6/ INTP10/ (RxD2)	P52/(INTP1)	P54/(INTP3)	P16/TIO1/ TO01/INTP5/ TRDI0C0/ IVREF0 Note 1/ (SI00)/(RxD0)	P21/ANI1/ AVREFM	P22/ANI2/ ANO0 Note 1	P23/ANI3/ ANO1 Note 1	4
3	P70/KR0/ SCK21/ SCL21	P73/KR3/ SO01	P74/KR4/ INTP8/SI01/ SDA01	P17/TIO2/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note 1/ (SO00)/(TXD0)	P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0)	P12/SO11/ TRDIOB1/ IVREF1 Note 1/ (INTP5)/ (TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJIO0	P72/KR2/ SO21	P71/KR1/ SI21/SDA21	P06/(INTP11)/ (TRJIO0)	P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)	P11/SI11/ SDA11/ TRDI0C1/ (RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJIO0)	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P55/ (PCLBUZ1)/ (SCK00)/ (INTP4)	P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 Note 1	P10/SCK11/ SCL11/ TRDIOD1	P146	P147/ANI18/ VCOUT1 Note 1	1
	A	B	C	D	E	F	G	H	

Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)	
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits $\times$ 8 bits, 16 bits $\times$ 16 bits), Division (16 bits $\div$ 16 bits, 32 bits $\div$ 32 bits) • Multiplication and Accumulation (16 bits $\times$ 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	

Note In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	3.09	mA			
					VDD = 3.0 V		0.80	3.09				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	2.40				
					VDD = 3.0 V		0.49	2.40				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	2.40				
					VDD = 3.0 V		0.62	2.40				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	1.83				
					VDD = 3.0 V		0.4	1.83				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	1.38				
					VDD = 3.0 V		0.37	1.38				
				LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		260		710	μA	
						VDD = 2.0 V		260		710		
				LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		420		700	μA	
						VDD = 2.0 V		420		700		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	1.55	mA			
					Resonator connection		0.40	1.74				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28		1.55		
						Resonator connection		0.40		1.74		
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19		0.86		
						Resonator connection		0.25		0.93		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.19	0.86				
					Resonator connection		0.25	0.93				
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		95	550	μA		
						Resonator connection		140	590			
			fMX = 8 MHz Note 3, VDD = 2.0 V		Square wave input		95	550				
					Resonator connection		140	590				
			Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA			
					Resonator connection		0.44	0.76				
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57				
					Resonator connection		0.49	0.76				
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17				
					Resonator connection		0.59	1.36				
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97				
					Resonator connection		0.72	2.16				
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37				
					Resonator connection		1.16	3.56				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
					TA = +25°C					0.24	0.51	
					TA = +50°C					0.29	1.10	
					TA = +70°C					0.41	1.90	
					TA = +85°C					0.90	3.30	

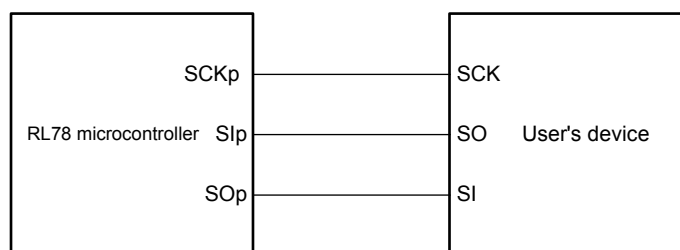
(Notes and Remarks are listed on the next page.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

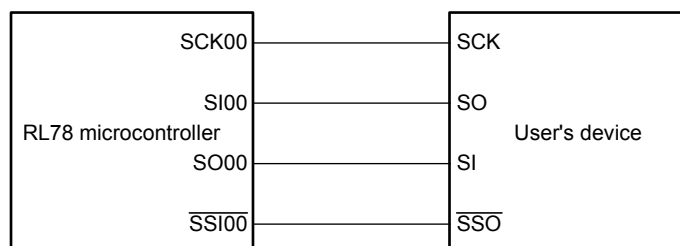
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SSI00 setup time	tSSIK	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
SSI00 hold time	tKSSI	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400	ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400	ns

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

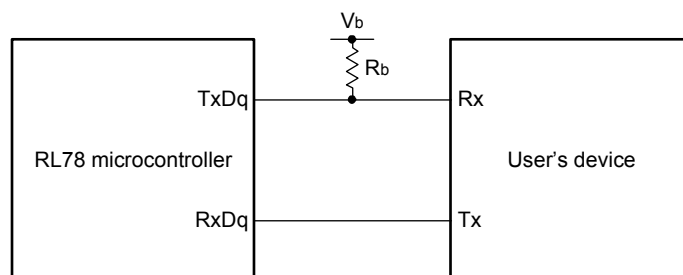
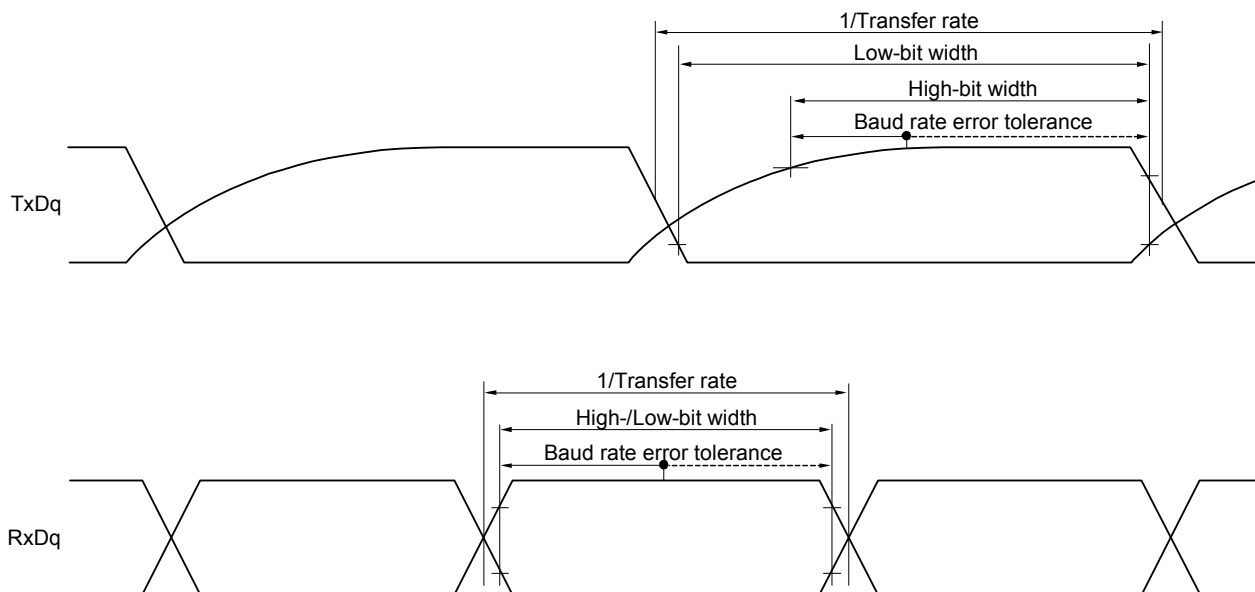
CSI mode connection diagram (during communication at same potential)

CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,

C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
Data hold time (transmission)	tHD:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The value must also be equal to or less than fMCK/4.**Note 2.** Use it with EVDD0 ≥ Vb.**Note 3.** Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(4) Peripheral Functions (Common to all products)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fIL = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

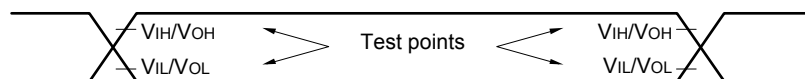
(TA = -40 to +105°C, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	$2\text{ MHz} < f_{\text{CLK}} \leq 32\text{ MHz}$	1			μs
			$f_{\text{CLK}} \leq 2\text{ MHz}$	$1/f_{\text{CLK}} + 1$			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		$2.5/f_{\text{CLK}}$			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	1			μs
		INTP1 to INTP11	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250			ns
$\overline{\text{RESET}}$ low-level width	tRSL			10			μs

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$f_{MCK}/12$ Note 2	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when $FRQSEL4 = 1$.

Note 2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

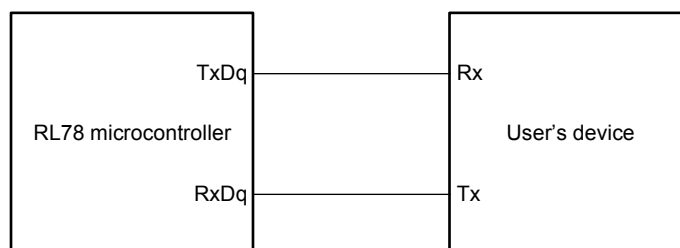
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

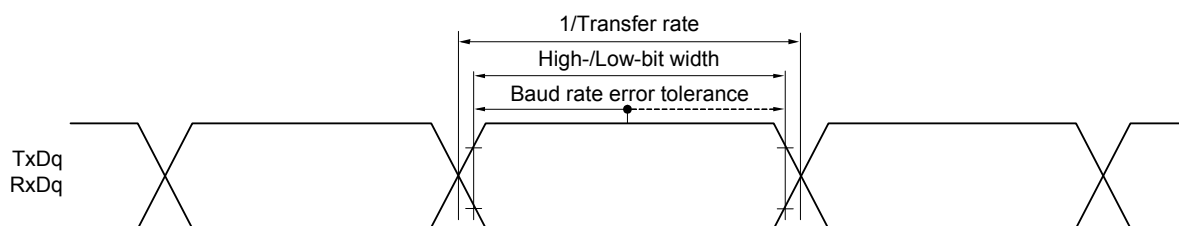
16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

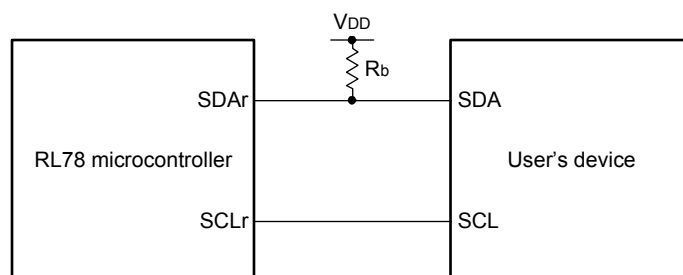
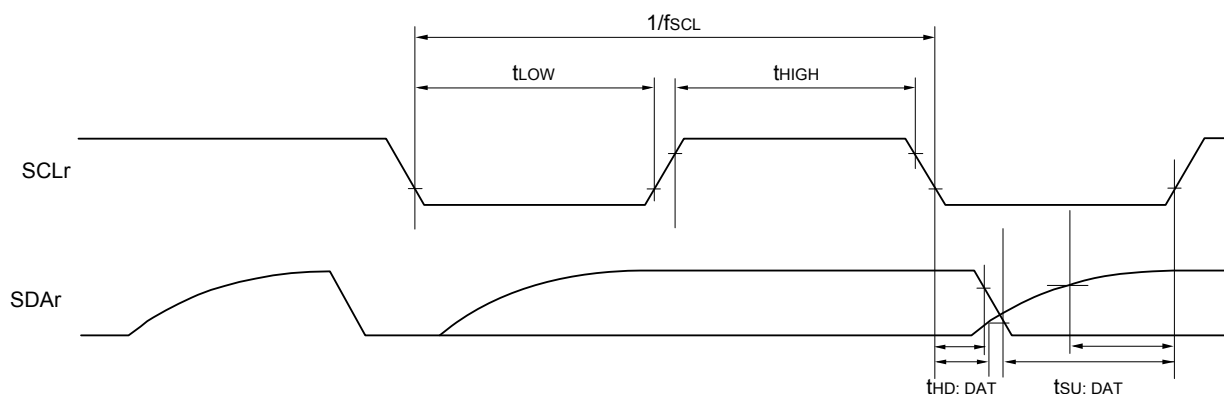


Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

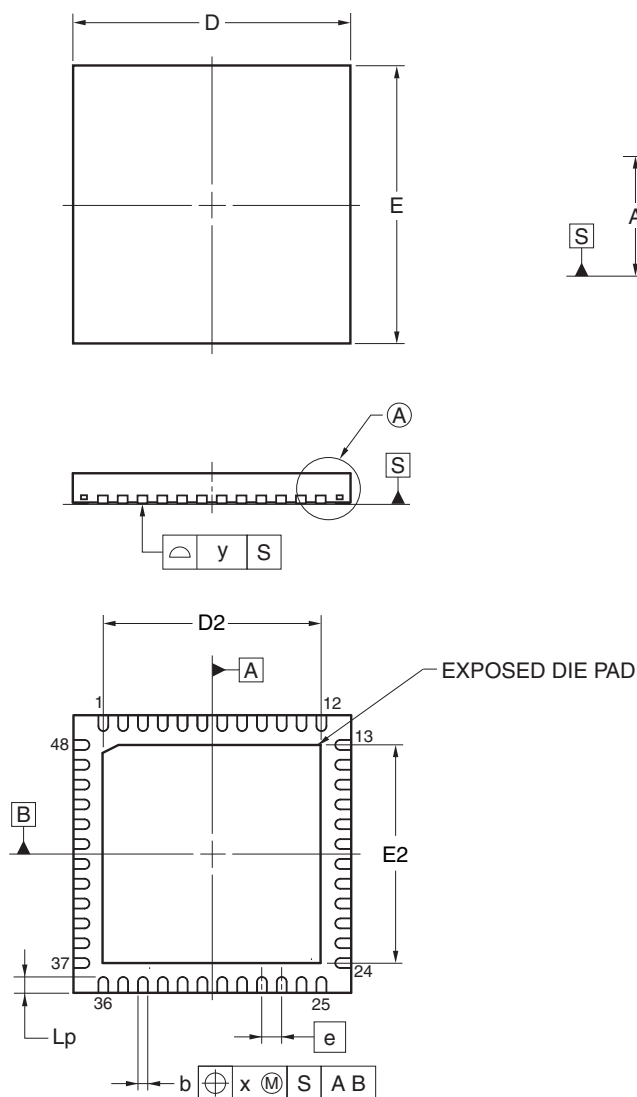
Remark 1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA,
 R5F104GHANA, R5F104GJANA
 R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA,
 R5F104GHDNA, R5F104GJDNA
 R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,
 R5F104GHGNA, R5F104GJGNA
 R5F104GKANA, R5F104GLANA
 R5F104GKGNA, R5F104GLGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

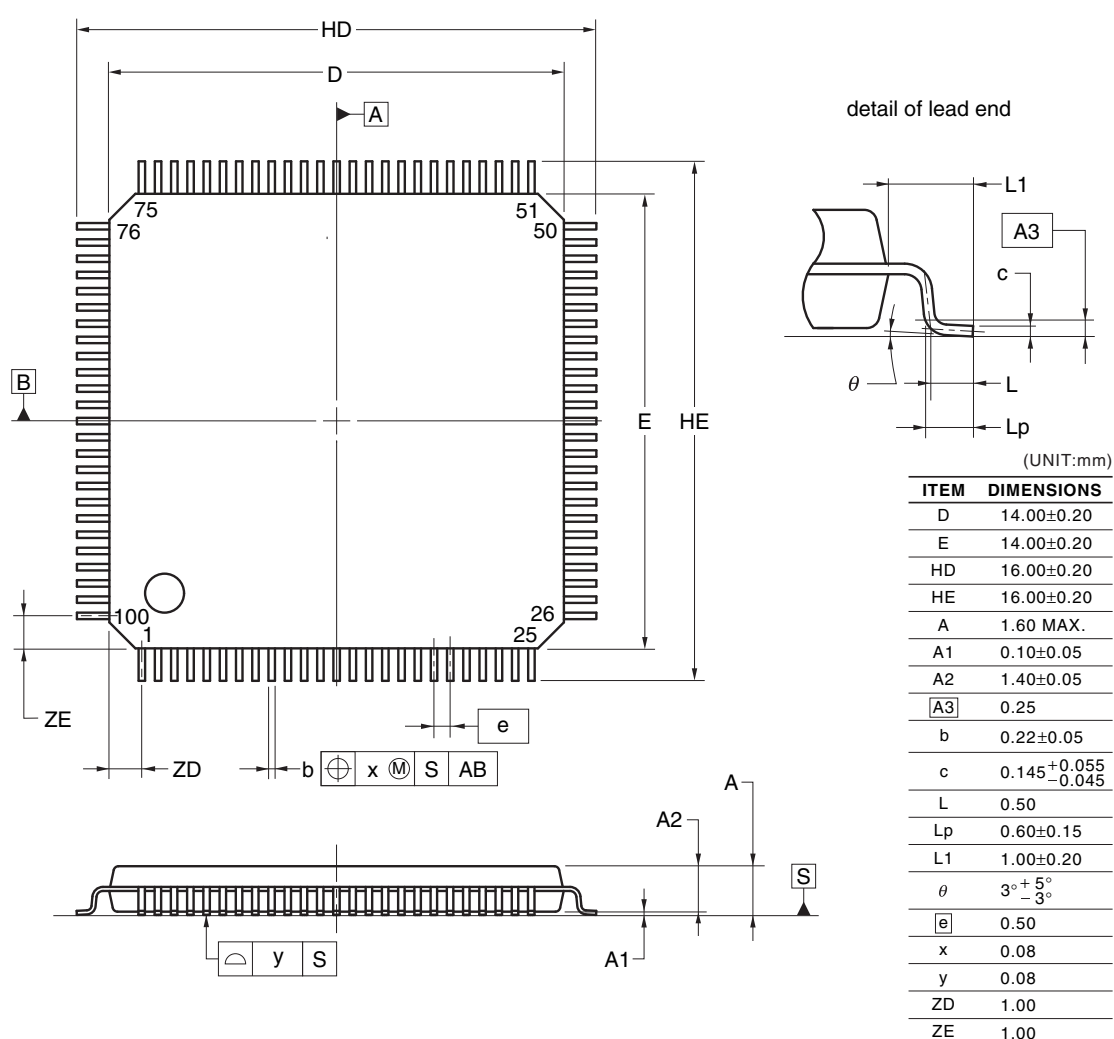
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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4.10 100-pin products

R5F104PFAFB, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB
 R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
 R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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