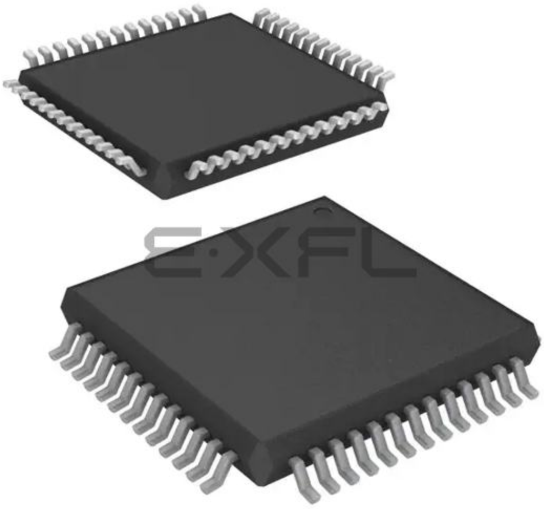
# Renesas Electronics America Inc - R5F104JJGFA#V0 Datasheet



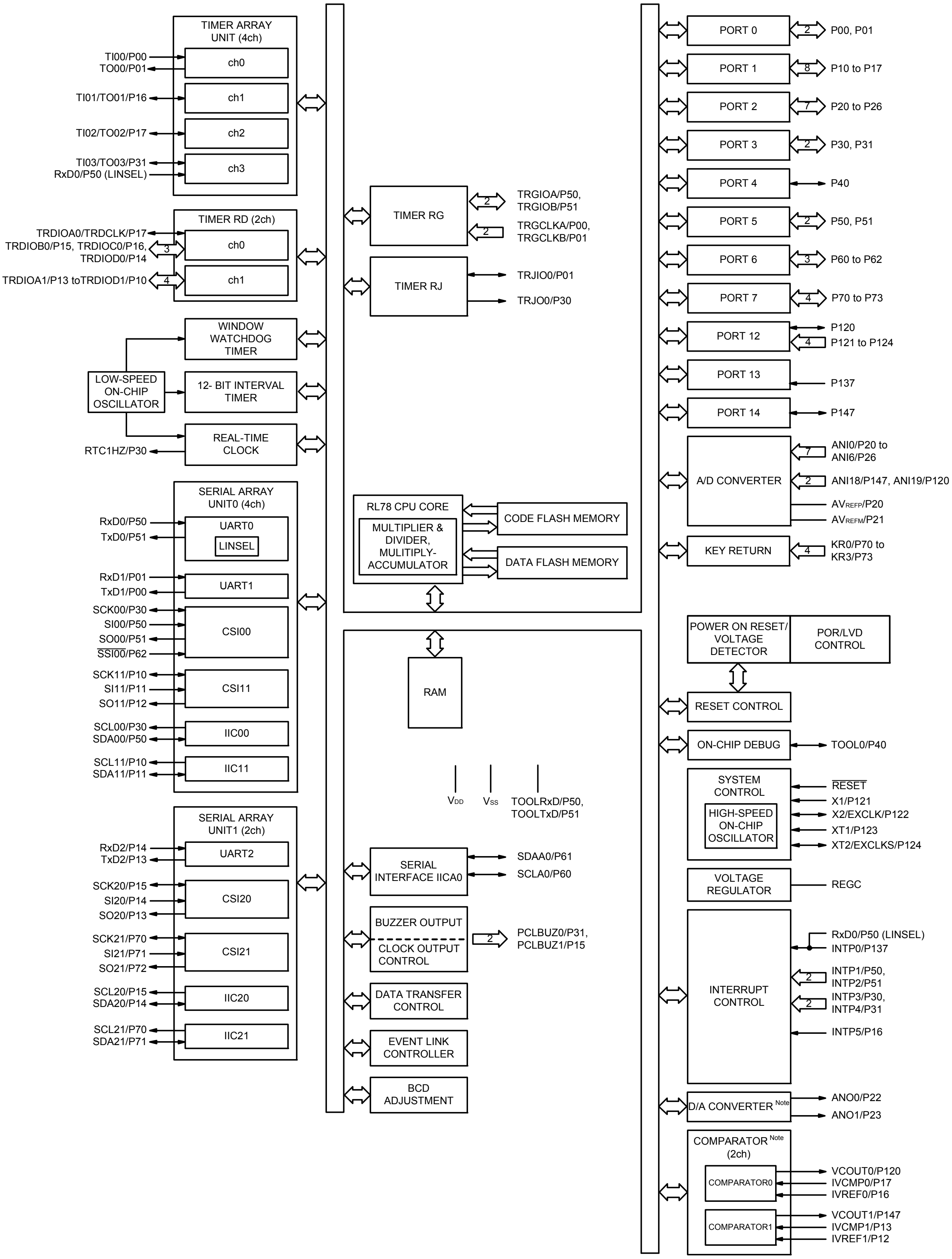
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104jjgfa-v0 |

### 1.5.4 40-pin products



**Note** Mounted on the 96 KB or more code flash memory products.

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax<br>(x = A, C to E) | R5F104Bx<br>(x = A, C to E) | R5F104Cx<br>(x = A, C to E) | R5F104Ex<br>(x = A, C to E) |
| Clock output/buzzer output | | 2 | 2 | 2 | 2 |
| | | [30-pin, 32-pin, 36-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>[40-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| 8/10-bit resolution A/D converter | | 8 channels | 8 channels | 8 channels | 9 channels |
| Serial interface | | [30-pin, 32-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I$^2$C: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified I$^2$C: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified I$^2$C: 1 channel<br>[36-pin, 40-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I$^2$C: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified I$^2$C: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified I$^2$C: 2 channels | | | |
| | I$^2$C bus | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 28 sources | | | 29 sources |
| Event link controller (ELC) | | Event input: 19<br>Event trigger output: 7 | | | Event input: 20<br>Event trigger output: 7 |
| Vectored interrupt sources | Internal | 24 | 24 | 24 | 24 |
| | External | 6 | 6 | 6 | 7 |
| Key interrupt | | — | — | — | 4 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | | | |
| On-chip debug function | | Provided | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = –40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = –40 to +105°C) | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\text{ V} \le V_{DD} \le 5.5\text{ V}$@1 MHz to 32 MHz
$2.4\text{ V} \le V_{DD} \le 5.5\text{ V}$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\text{ V} \le V_{DD} \le 5.5\text{ V}$@1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\text{ V} \le V_{DD} \le 5.5\text{ V}$@1 MHz to 4 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

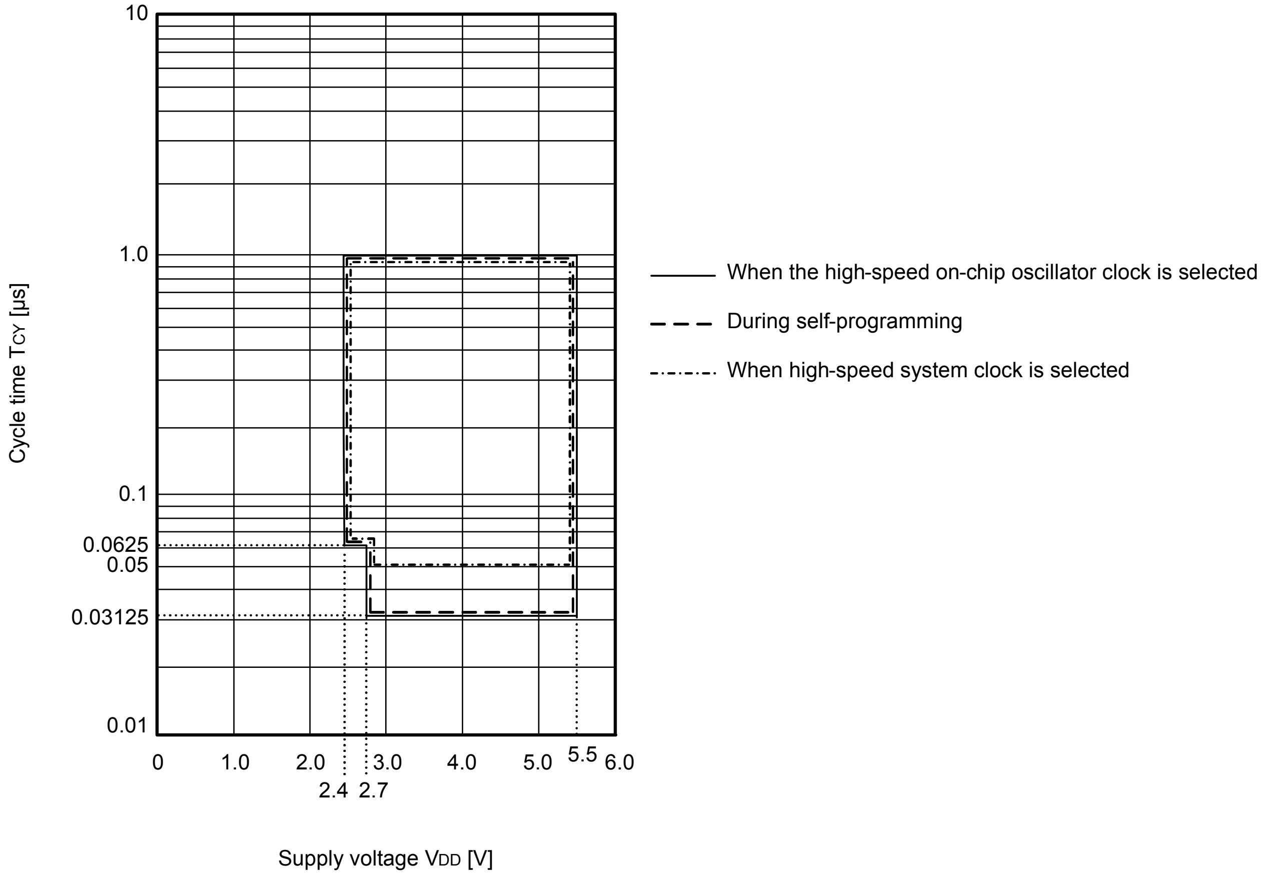
**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

Minimum Instruction Execution Time during Main System Clock Operation

$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution** **Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (3/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution** **Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### (3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI20 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**Note 4.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

### ($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)(2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz,<br>$f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 4.36 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 4.36 | |
| | | | | $f_{HOCO}$ = 32 MHz,<br>$f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 3.67 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 3.67 | |
| | | | | $f_{HOCO}$ = 48 MHz,<br>$f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.42 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.42 | |
| | | | | $f_{HOCO}$ = 24 MHz,<br>$f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.85 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.85 | |
| | | | | $f_{HOCO}$ = 16 MHz,<br>$f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 2.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 2.08 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3,<br>$V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 2.45 | mA |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 20 MHz Note 3,<br>$V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 2.45 | |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3,<br>$V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | | $f_{MX}$ = 10 MHz Note 3,<br>$V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | µA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = +50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = +70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5,<br>$T_A$ = +105°C | Square wave input | | 3.20 | 17.10 | |
| | | | | | Resonator connection | | 3.40 | 17.50 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | µA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 3.10 | 17.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator).
The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User’s Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency
**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency
**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

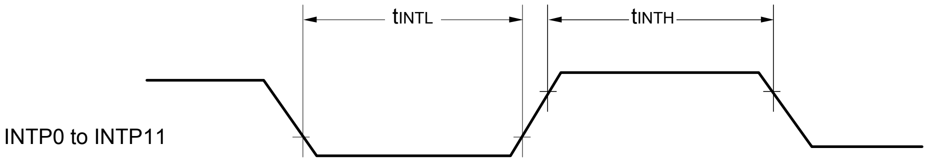
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03, TI10 to TI13 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |

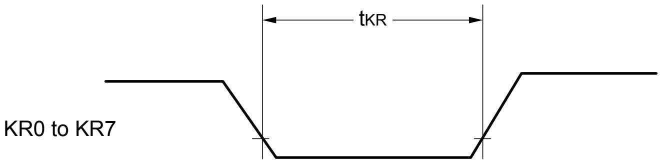
**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

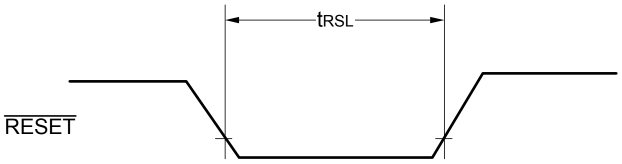
Interrupt Request Input Timing



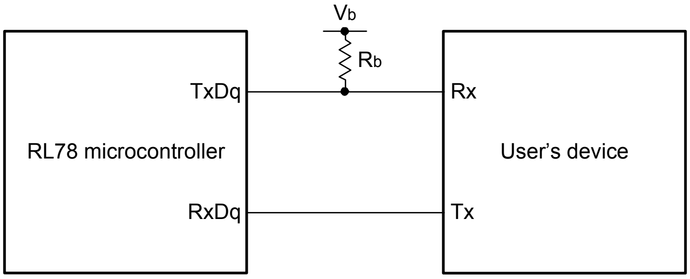
Key Interrupt Input Timing



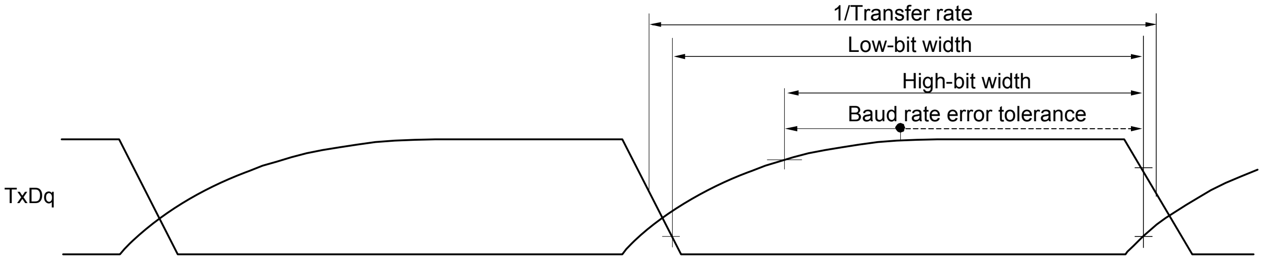
$\overline{\text{RESET}}$ Input Timing

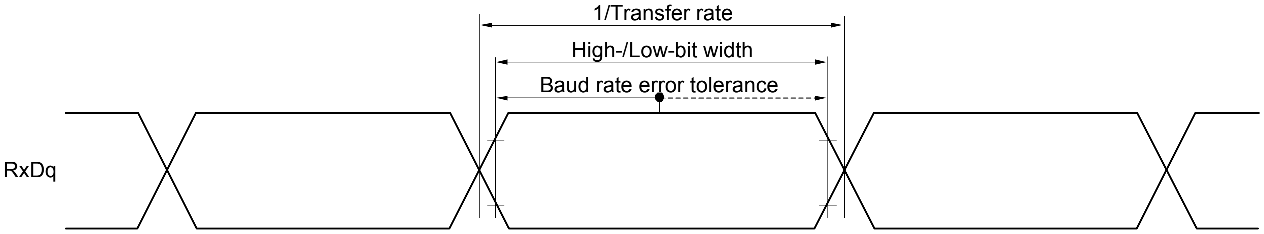


**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**





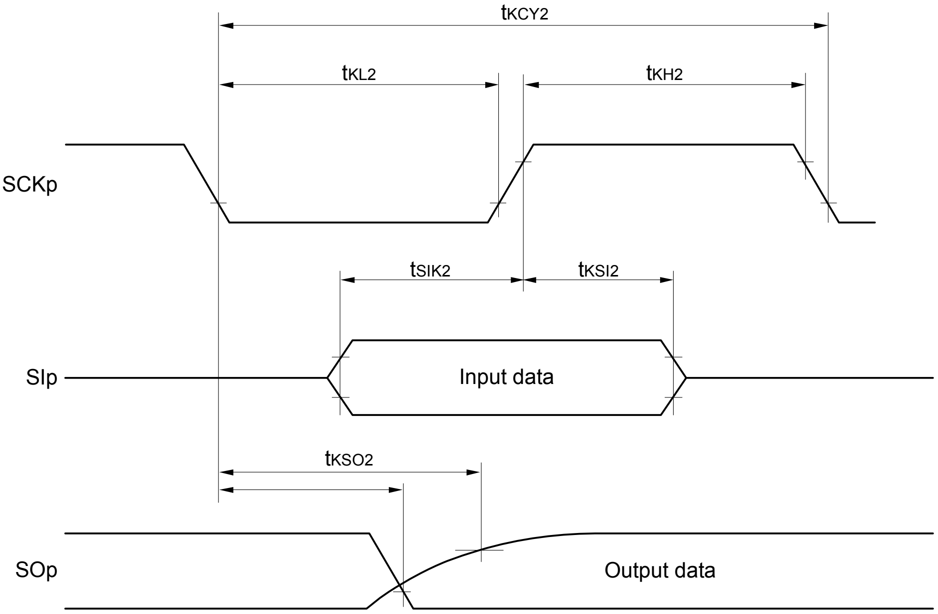
**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

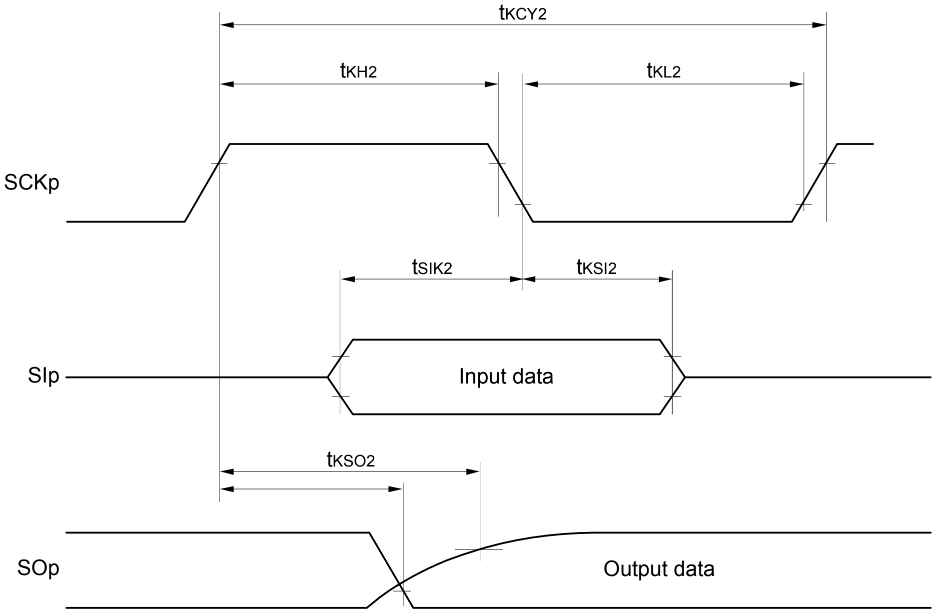
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V,**
**$V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin: ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI20 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $EV_{DD0}$ ≤ $AV_{REFP}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

### 3.6.6 LVD circuit characteristics

**(1) Reset Mode and Interrupt Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.90 | 4.06 | 4.22 | V |
| | | | Falling edge | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Rising edge | 3.60 | 3.75 | 3.90 | V |
| | | | Falling edge | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Rising edge | 3.01 | 3.13 | 3.25 | V |
| | | | Falling edge | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Rising edge | 2.90 | 3.02 | 3.14 | V |
| | | | Falling edge | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Rising edge | 2.81 | 2.92 | 3.03 | V |
| | | | Falling edge | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Rising edge | 2.70 | 2.81 | 2.92 | V |
| | | | Falling edge | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Rising edge | 2.61 | 2.71 | 2.81 | V |
| | | | Falling edge | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Rising edge | 2.51 | 2.61 | 2.71 | V |
| | | | Falling edge | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

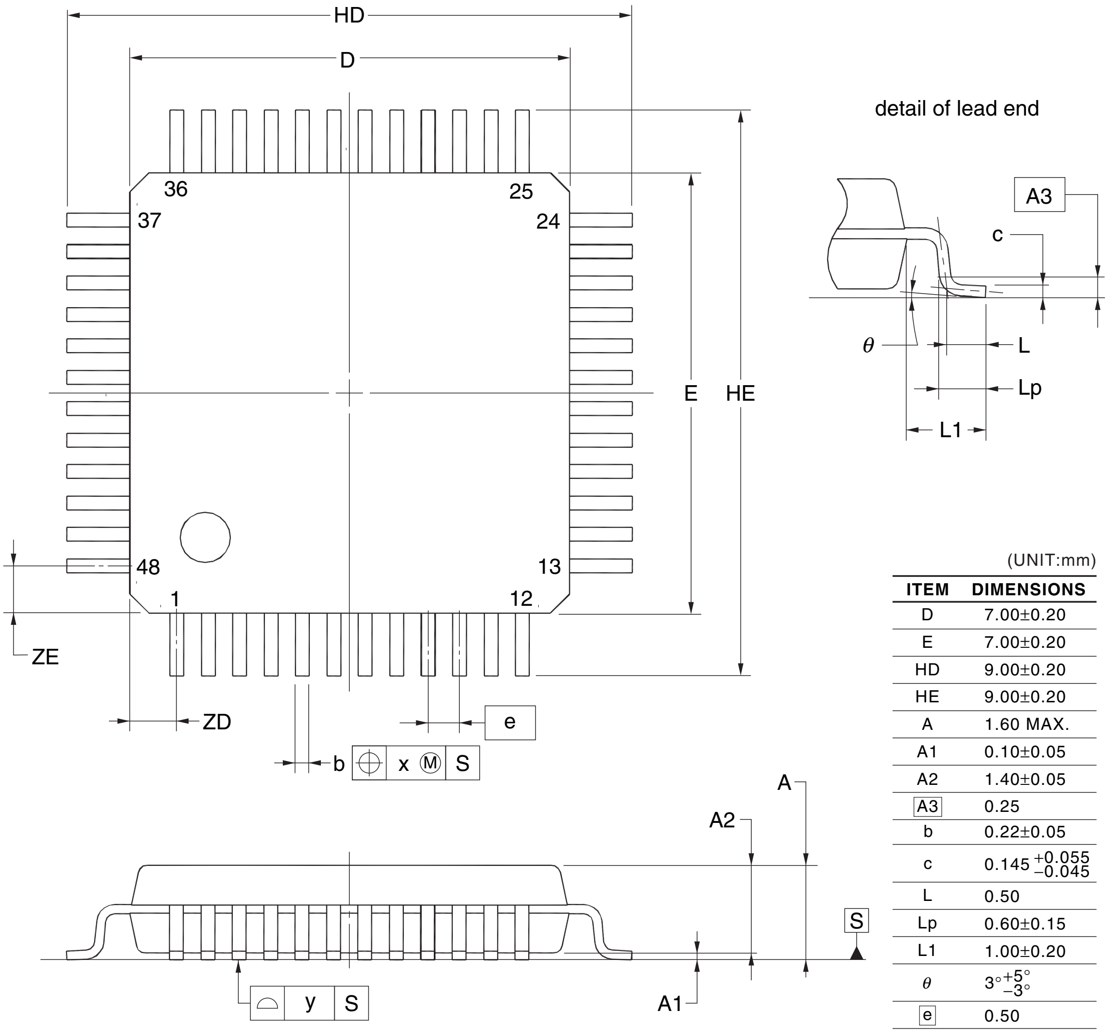
## 4.6 48-pin products

R5F104GAAFB, R5F104GCAFB, R5F104GDAFB, R5F104GEAFB, R5F104GFAFB, R5F104GGAFB, R5F104GHAFB, R5F104GJAFB

R5F104GADFB, R5F104GCDFB, R5F104GDDFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB, R5F104GHDFB, R5F104GJDFB

R5F104GAGFB, R5F104GCGFB, R5F104GDGFB, R5F104GEGFB, R5F104GFGFB, R5F104GGGFB, R5F104GHGFB, R5F104GJGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16 |



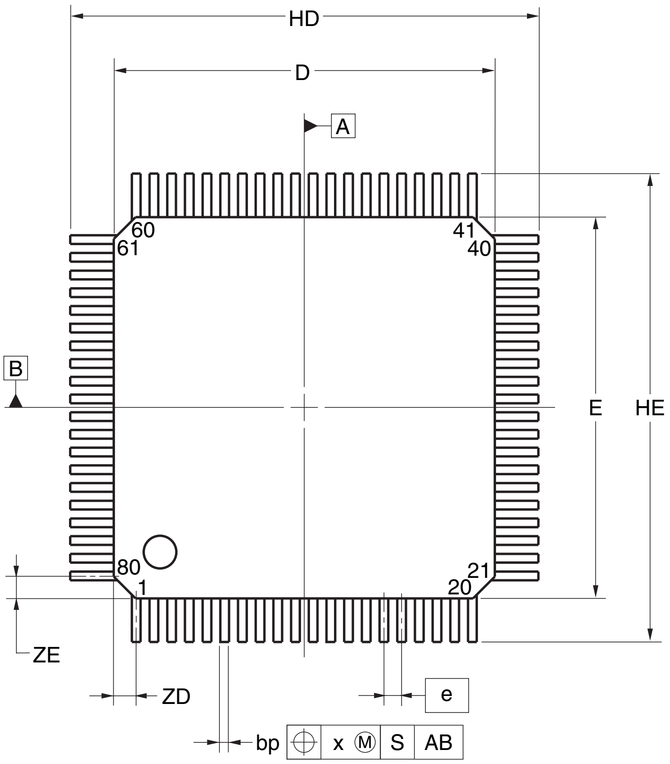
(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.20 |
| E | 7.00±0.20 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| $\theta$ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

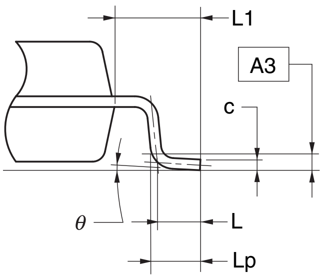
**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA
R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
R5F104MKAFA, R5F104MLAFA
R5F104MKGFA, R5F104MLGFA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JB-E | P80GC-65-UBT-2 | 0.69 |



detail of lead end



| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.80 | 14.00 | 14.20 |
| E | 13.80 | 14.00 | 14.20 |
| HD | 17.00 | 17.20 | 17.40 |
| HE | 17.00 | 17.20 | 17.40 |
| A | — | — | 1.70 |
| A1 | 0.05 | 0.125 | 0.20 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | — | 0.25 | — |
| bp | 0.26 | 0.32 | 0.38 |
| c | 0.10 | 0.145 | 0.20 |
| L | — | 0.80 | — |
| Lp | 0.736 | 0.886 | 1.036 |
| L1 | 1.40 | 1.60 | 1.80 |
| θ | 0° | 3° | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| ZD | — | 0.825 | — |
| ZE | — | 0.825 | — |