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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

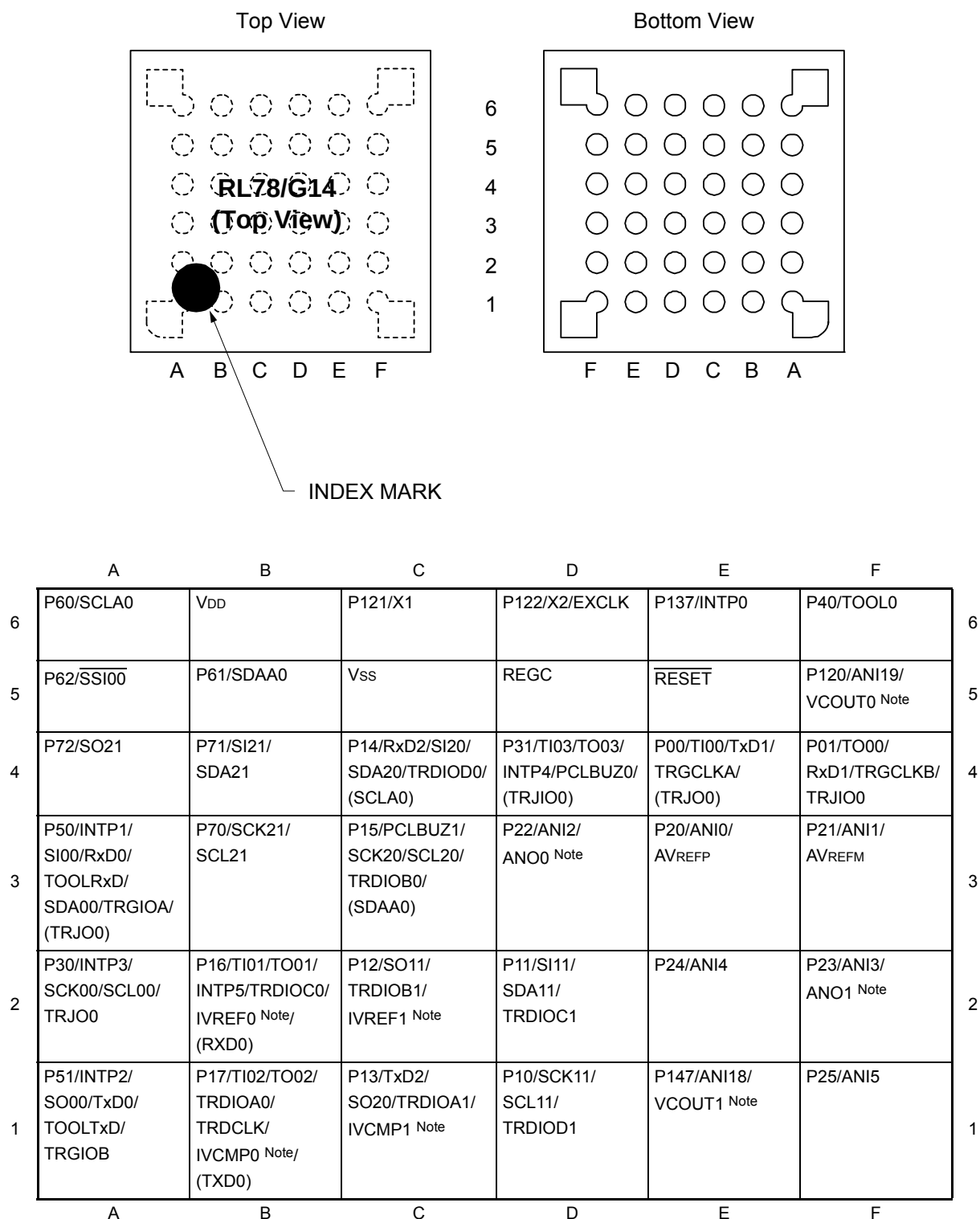
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104lddfb-x0

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

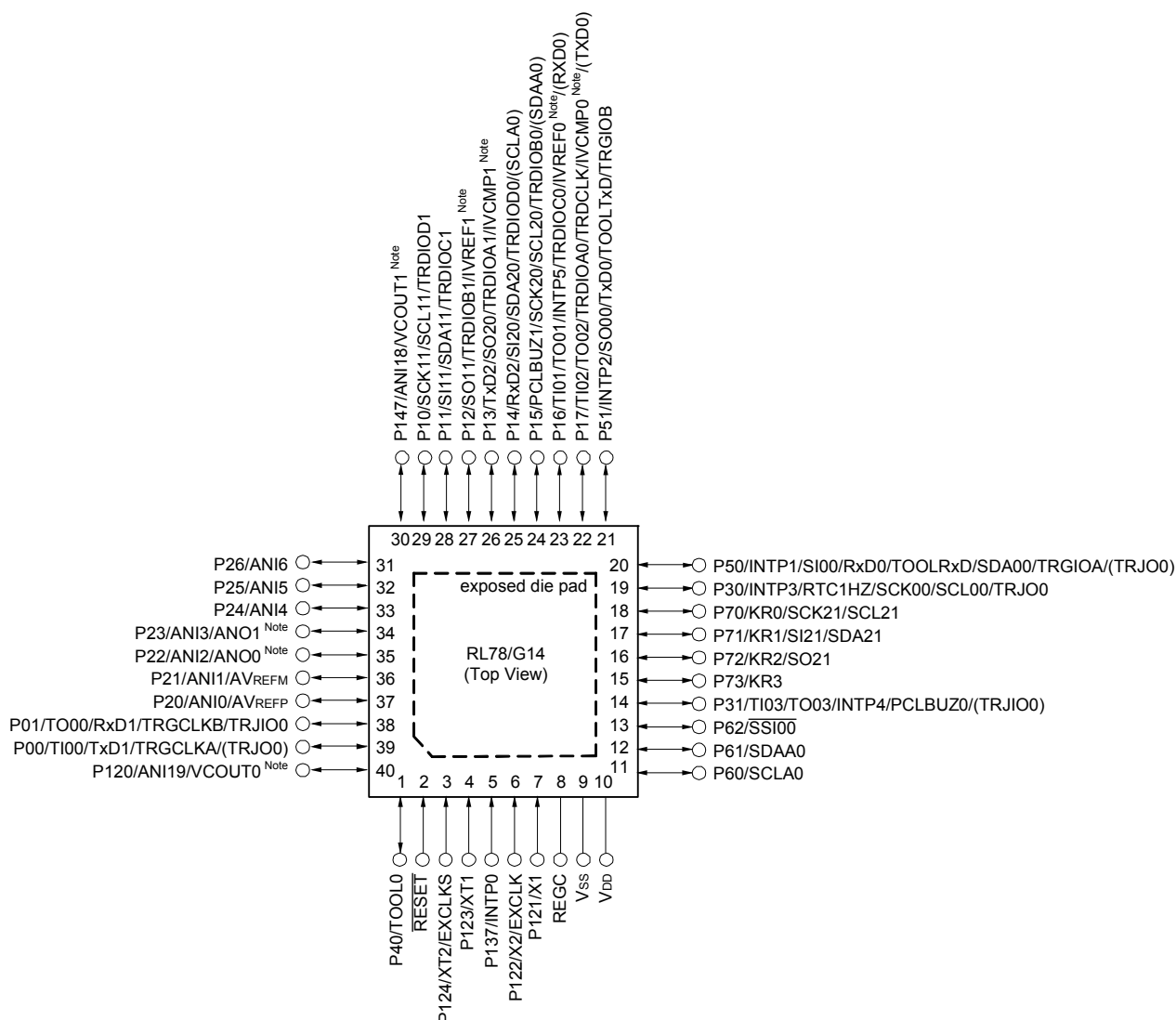
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

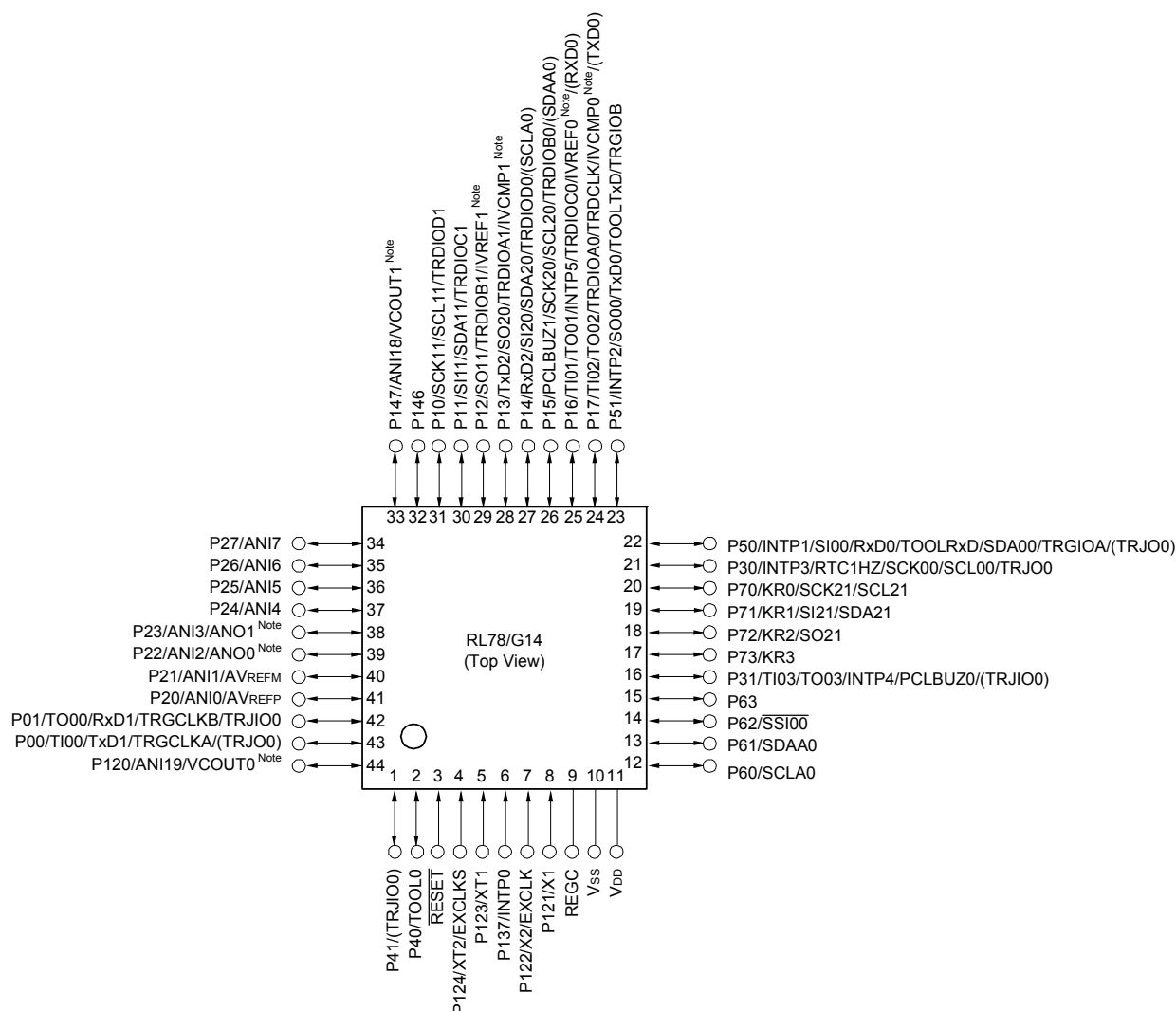
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.5 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

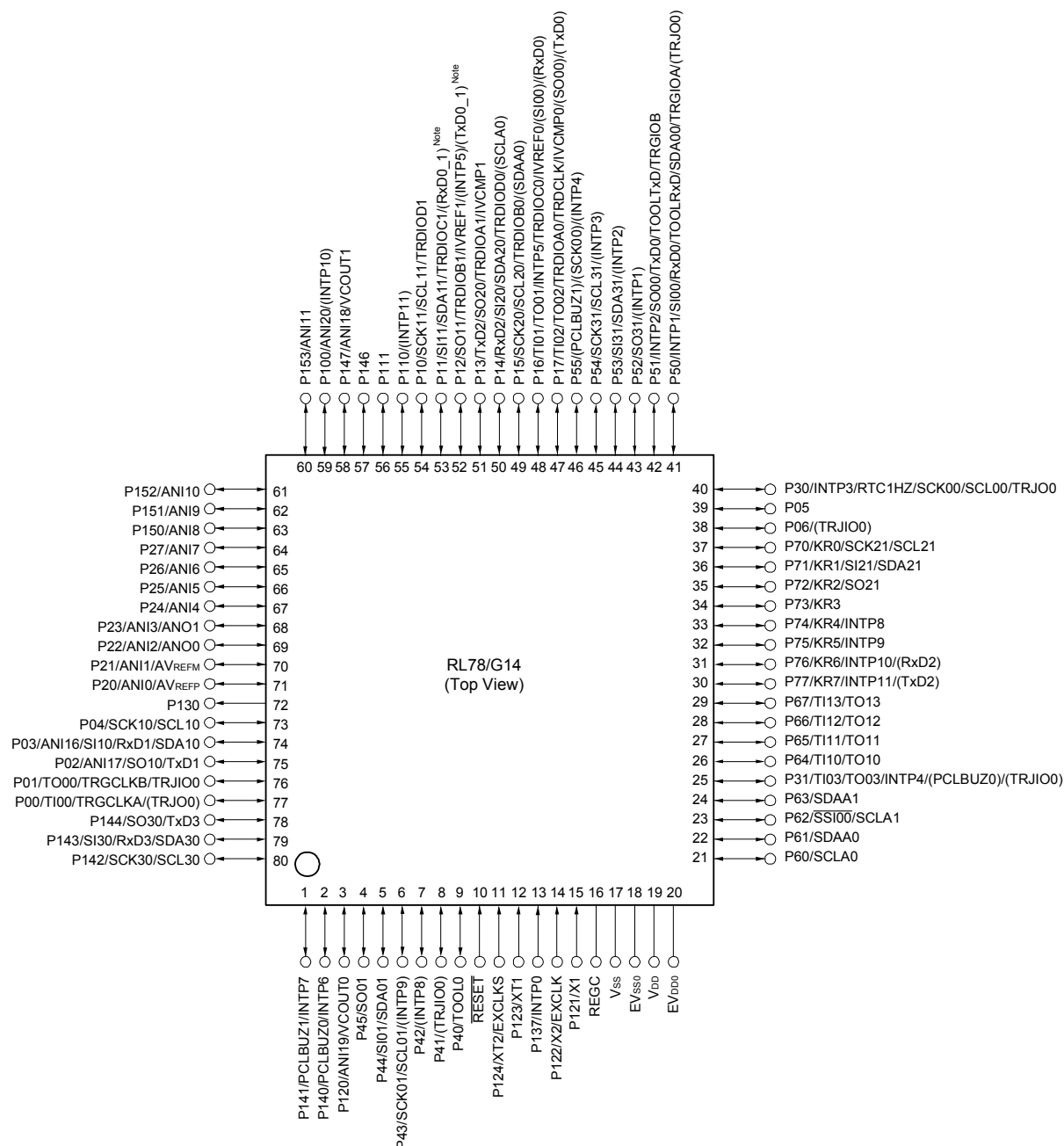
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	16 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note	2.5 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)

(Note is listed on the next page.)

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Code flash memory (KB)		96 to 128	96 to 128	96 to 128	96 to 192
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 16 Note	12 to 16 Note	12 to 16 Note	12 to 20 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
General-purpose register		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)			
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)			
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)			
		—			30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits $\times$ 8 bits, 16 bits $\times$ 16 bits), Division (16 bits $\div$ 16 bits, 32 bits $\div$ 32 bits) • Multiplication and Accumulation (16 bits $\times$ 16 bits $\div$ 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)

(Note is listed on the next page.)

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Code flash memory (KB)		16 to 64	16 to 64	32 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	4 to 5.5 Note	4 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)			

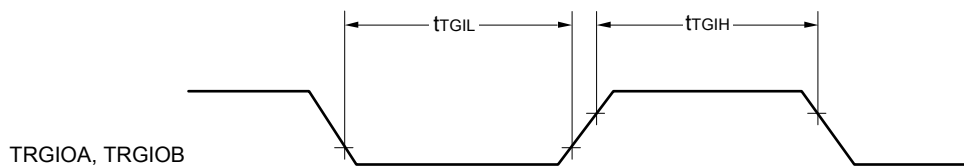
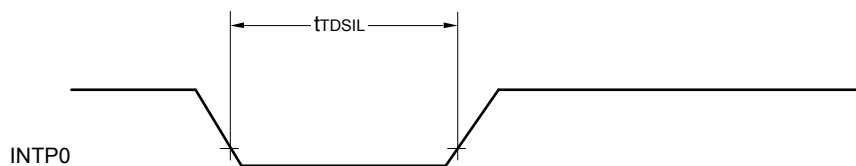
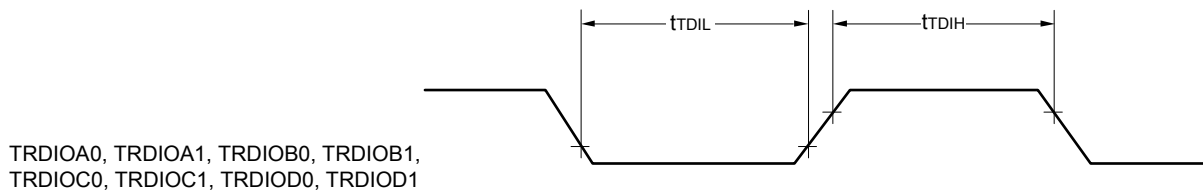
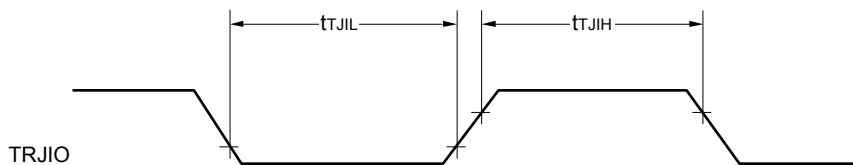
(Note is listed on the next page.)

(2/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Clock output/buzzer output		2	2	2	2
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		10 channels	10 channels	12 channels	12 channels
Serial interface		[44-pin products] - CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [48-pin, 52-pin products] - CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [64-pin products] - CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels			
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		29 sources	30 sources		31 sources
Event link controller (ELC)		Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt		4	6	8	8
Reset		- Reset by $\overline{\text{RESET}}$ pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access			
Power-on-reset circuit		- Power-on-reset: 1.51 ±0.04 V (T_A = -40 to +85°C) 1.51 ±0.06 V (T_A = -40 to +105°C) - Power-down-reset: 1.50 ±0.04 V (T_A = -40 to +85°C) 1.50 ±0.06 V (T_A = -40 to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)			
Operating ambient temperature		T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

- Note 1.** Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|-------------------------------------|
| HS (high-speed main) mode: | 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ VDD ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ VDD ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK}	4.0 V ≤ EVDD0 ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EVDD0 ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 7		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 10		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EVDD0 ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		33		110		110		ns
Slp hold time (from SCKp↑) Note 2	t _{SI1}	2.7 V ≤ EVDD0 ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t _{SO1}	C = 20 pF Note 4			10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00))

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8 \text{ V} \leq EV_{DD0} < 3.3 \text{ V}$ and $1.6 \text{ V} \leq V_b \leq 2.0 \text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V <i>Note</i> , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns

Note Use it with EVDD0 ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

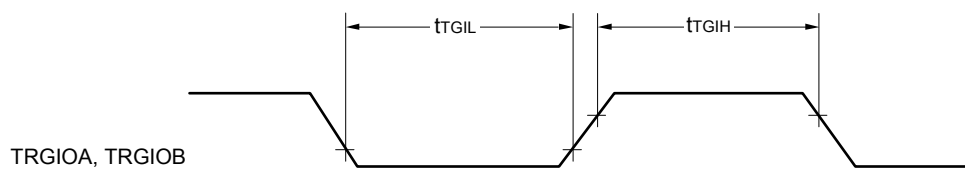
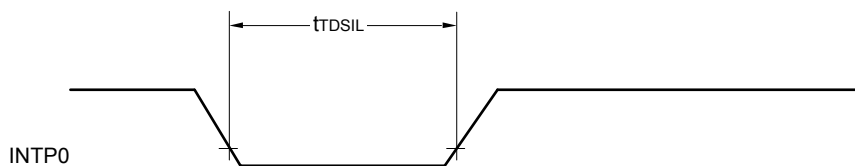
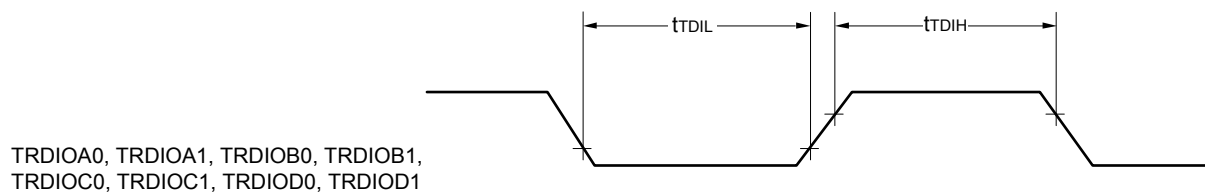
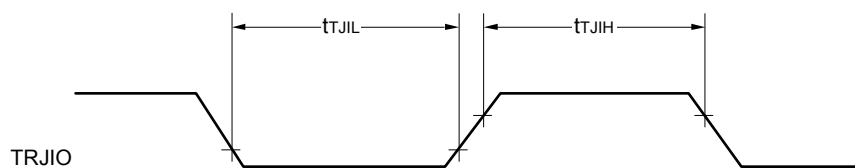
(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

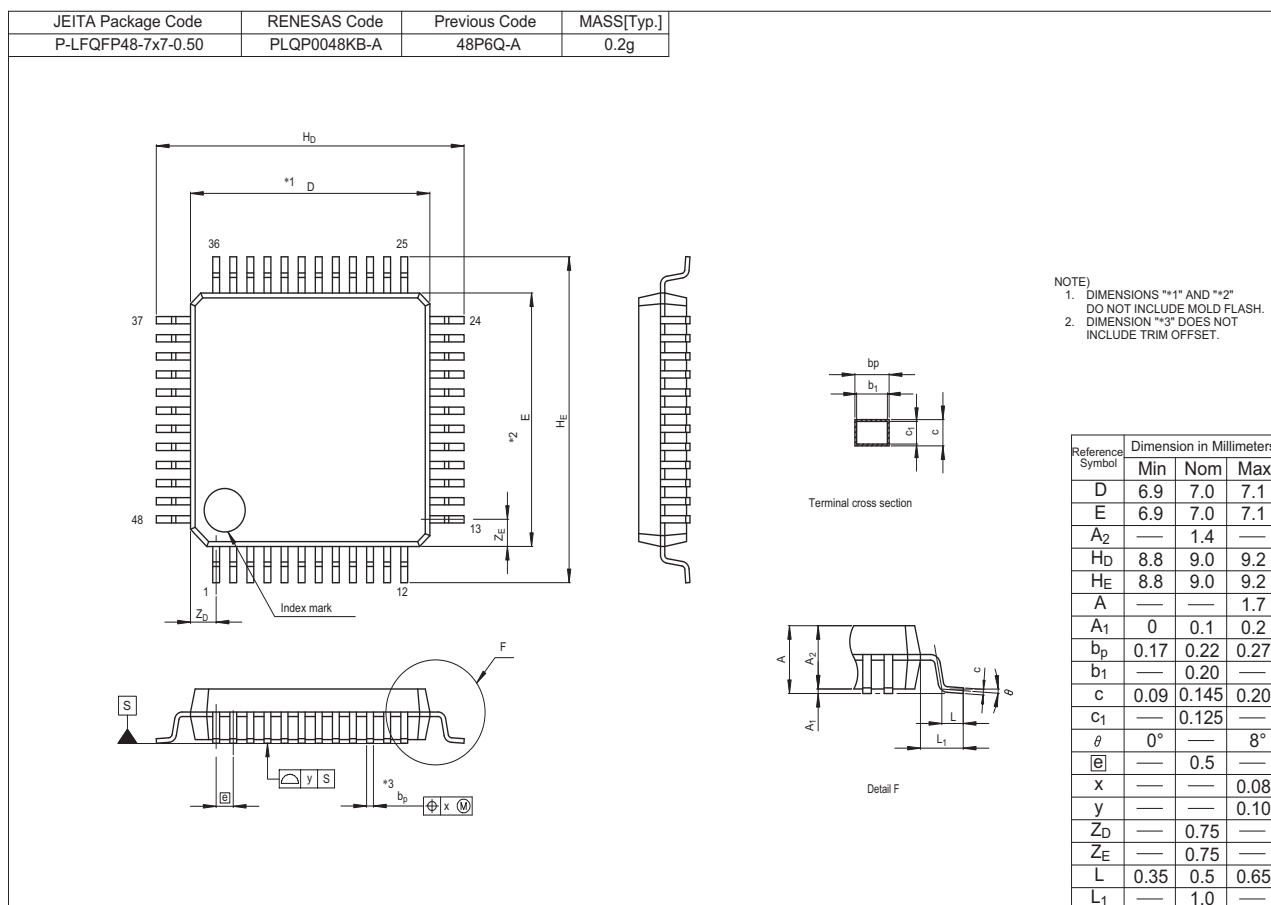
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	4.86	mA
					VDD = 3.0 V		0.79	4.86	
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	4.17	
					VDD = 3.0 V		0.49	4.17	
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.82	
					VDD = 3.0 V		0.62	3.82	
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	3.25	
					VDD = 3.0 V		0.4	3.25	
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	2.28	
					VDD = 3.0 V		0.38	2.28	
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	2.65	mA
					Resonator connection		0.40	2.77	
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30	2.65	
					Resonator connection		0.40	2.77	
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
	IDD3 Note 6	STOP mode Note 8	Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA
					Resonator connection		0.47	0.85	
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66	
					Resonator connection		0.53	0.85	
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35	
					Resonator connection		0.56	2.54	
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08	
					Resonator connection		0.80	4.27	
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09	
					Resonator connection		1.74	8.28	
				fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		6.00	51.00	
					Resonator connection		6.00	51.00	
				TA = -40°C			0.19	0.57	μA
				TA = +25°C			0.25	0.57	
				TA = +50°C			0.33	2.26	
				TA = +70°C			0.52	3.99	
				TA = +85°C			1.46	8.00	
				TA = +105°C			5.50	50.00	

(Notes and Remarks are listed on the next page.)



R5F104GKAFB, R5F104GLAFB

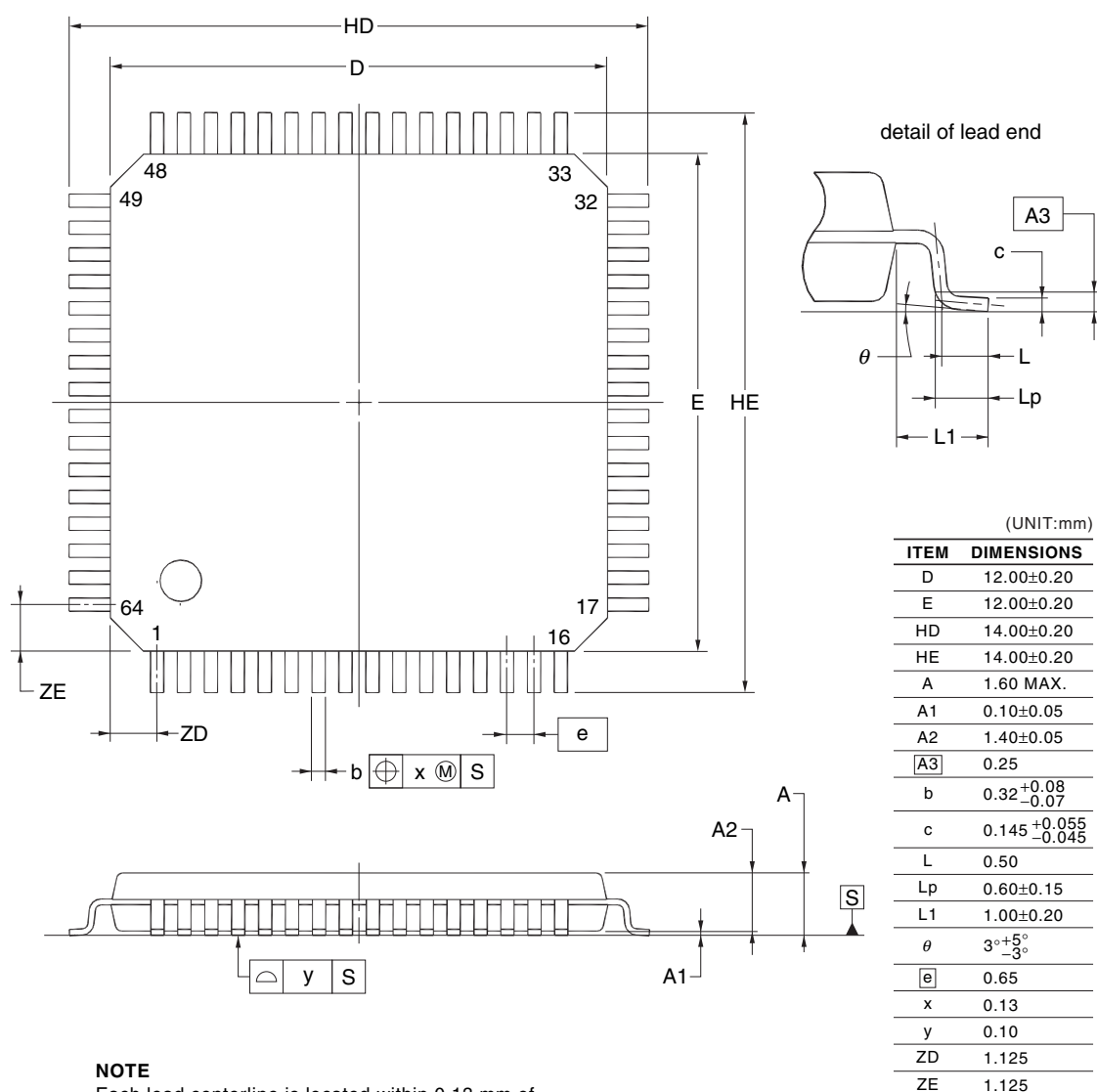
R5F104GKGFB, R5F104GLGFB



4.8 64-pin products

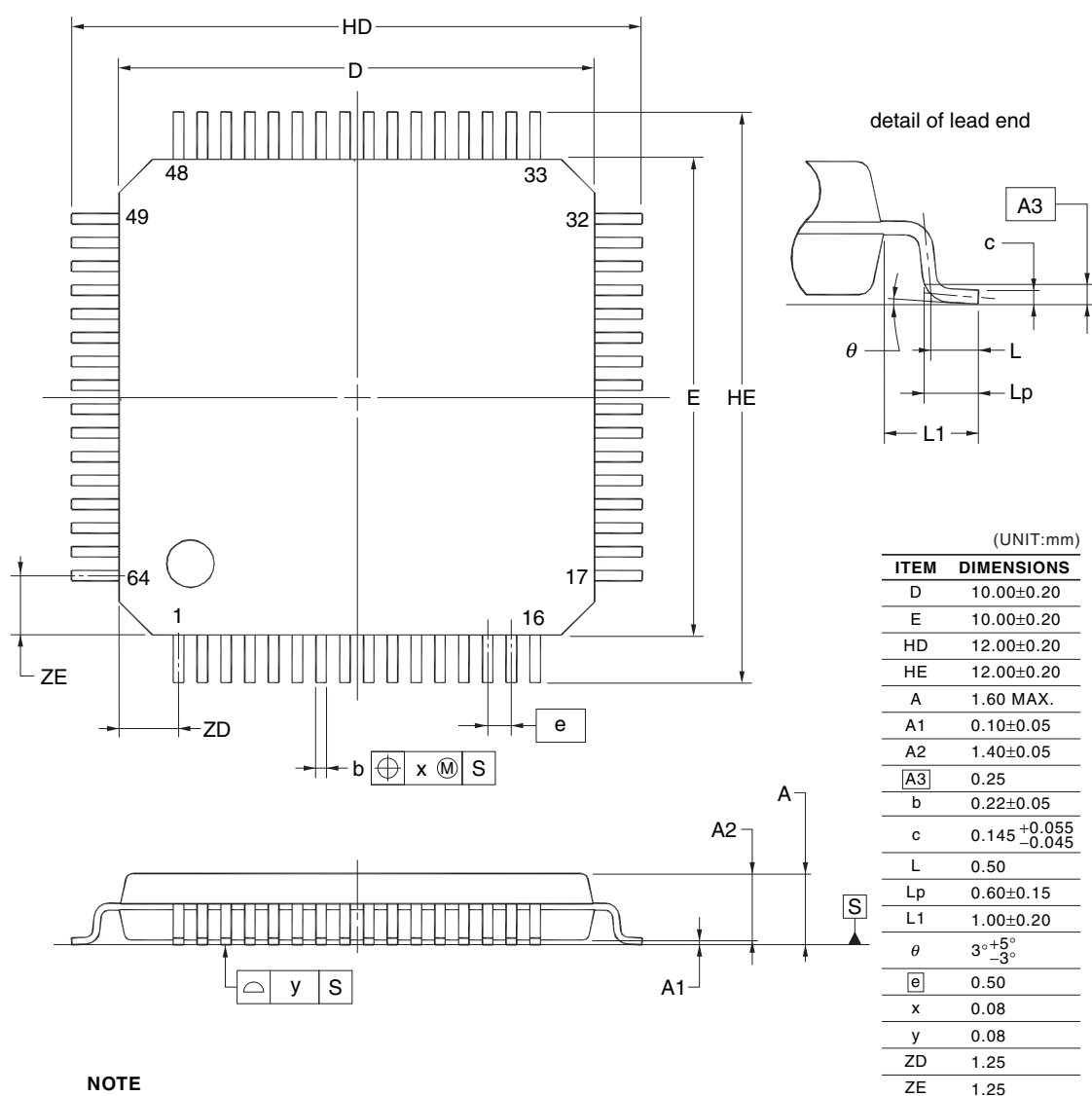
R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFa, R5F104LHAFA, R5F104LJAFA
 R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFa, R5F104LHDFa, R5F104LJDFa
 R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
 R5F104LKAFA, R5F104LLAFA
 R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB,
 R5F104LJAFB
 R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LFDFB, R5F104LGDFB, R5F104LHDFB,
 R5F104LJDFB
 R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB,
 R5F104LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

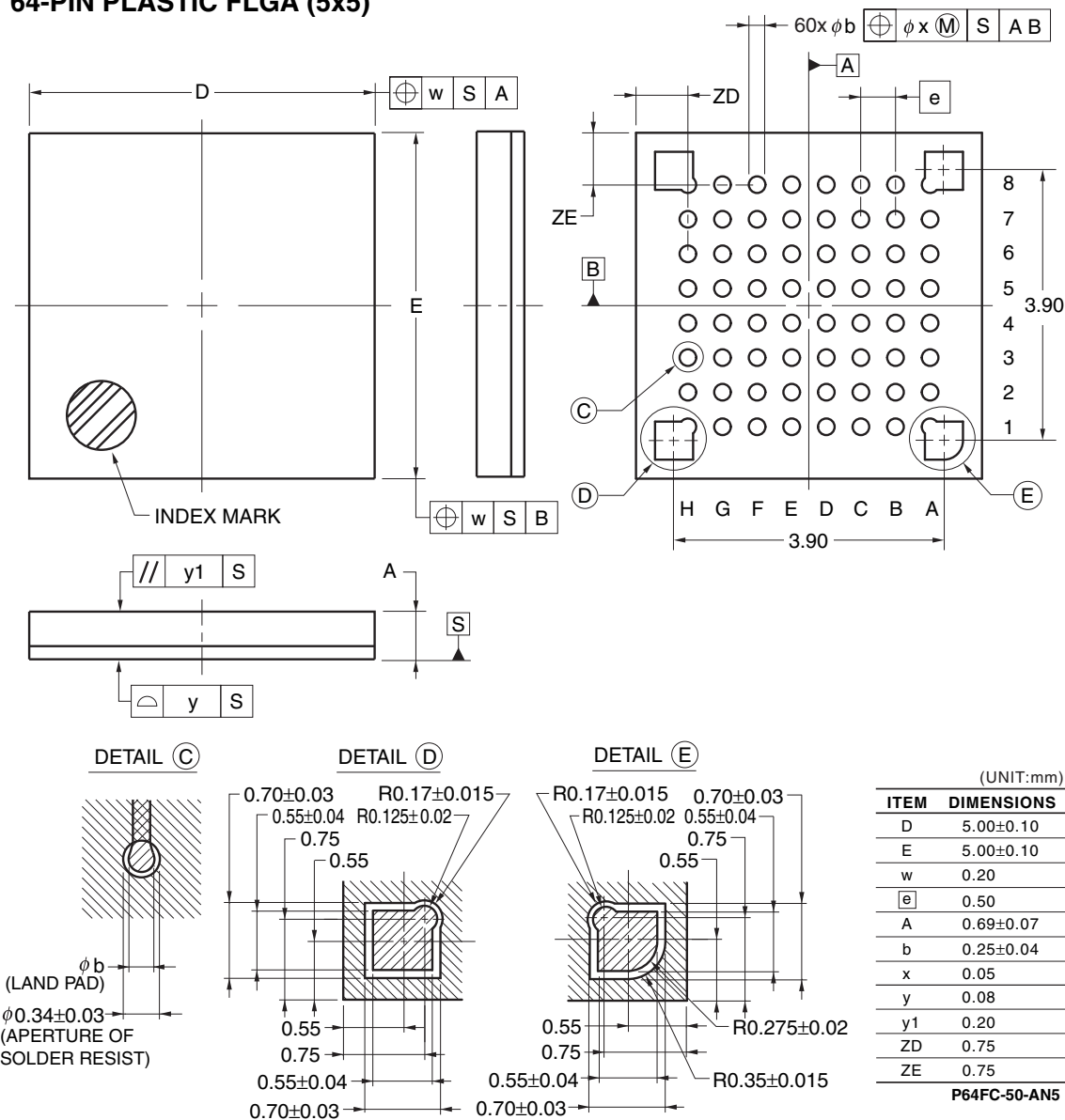


NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104LKGLA, R5F104LLGLA

64-PIN PLASTIC FLGA (5x5)



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REVISION HISTORY	RL78/G14 Datasheet
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Rev.	Date	Description	
		Page	Summary
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145 p.197	Modification of specifications in 3.3.2 Supply current characteristics Modification of part number in 4.7 52-pin products
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics

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