# Renesas Electronics America Inc - R5F104LEAFB#30 Datasheet

**Welcome to E-XFL.COM**

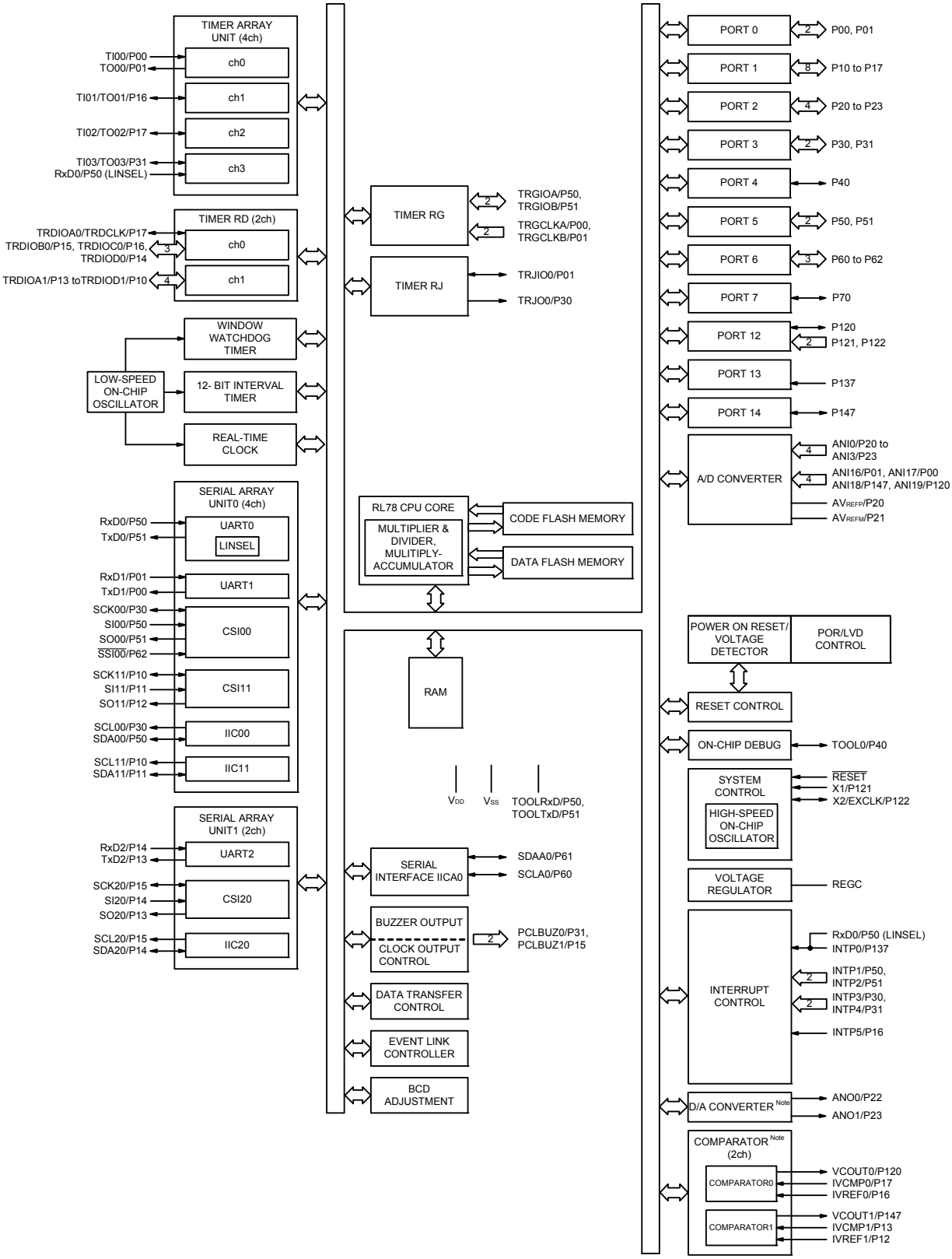
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

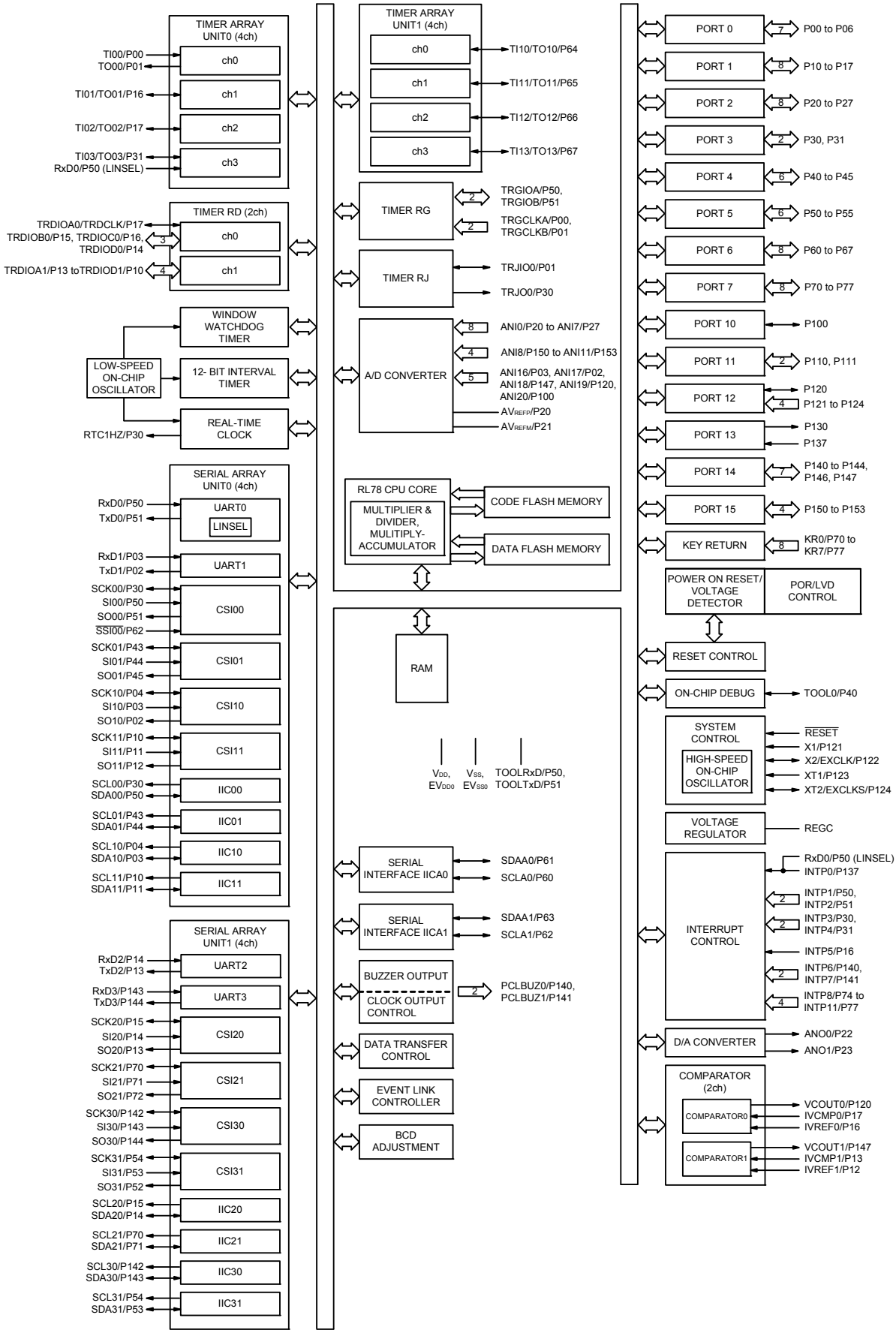
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 5.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104leafb-30 |

## 1.5.2 32-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.9 80-pin products



[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = F, G) | R5F104Bx (x = F, G) | R5F104Cx (x = F, G) | R5F104Ex (x = F to H) |
| Code flash memory (KB) | | 96 to 128 | 96 to 128 | 96 to 128 | 96 to 192 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 16 Note | 12 to 16 Note | 12 to 16 Note | 12 to 20 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | — | | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | — | | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 26 | 28 | 32 | 36 |
| | CMOS I/O | 21 | 22 | 26 | 28 |
| | CMOS input | 3 | 3 | 3 | 5 |
| | CMOS output | — | — | — | — |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 3 | 3 | 3 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |

(**Note** is listed on the next page.)

## 2.3.2 Supply current characteristics

### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.1 | 8.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.1 | 8.7 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.1 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.1 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 6.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 6.9 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.3 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.6 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 2.0 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.8 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | mA |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

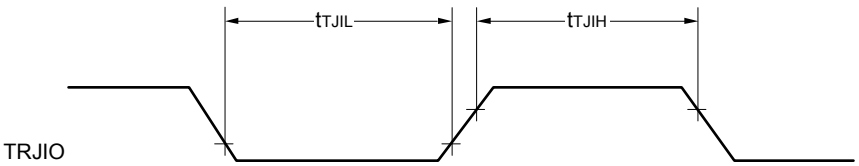
**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

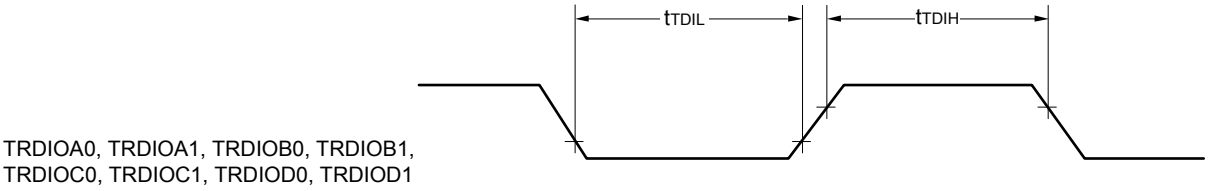
**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

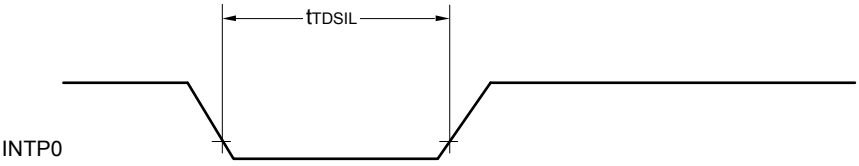
**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

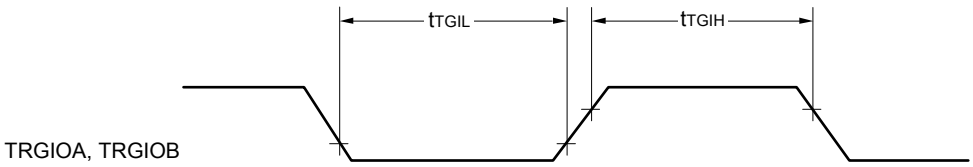
**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C


tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1


tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

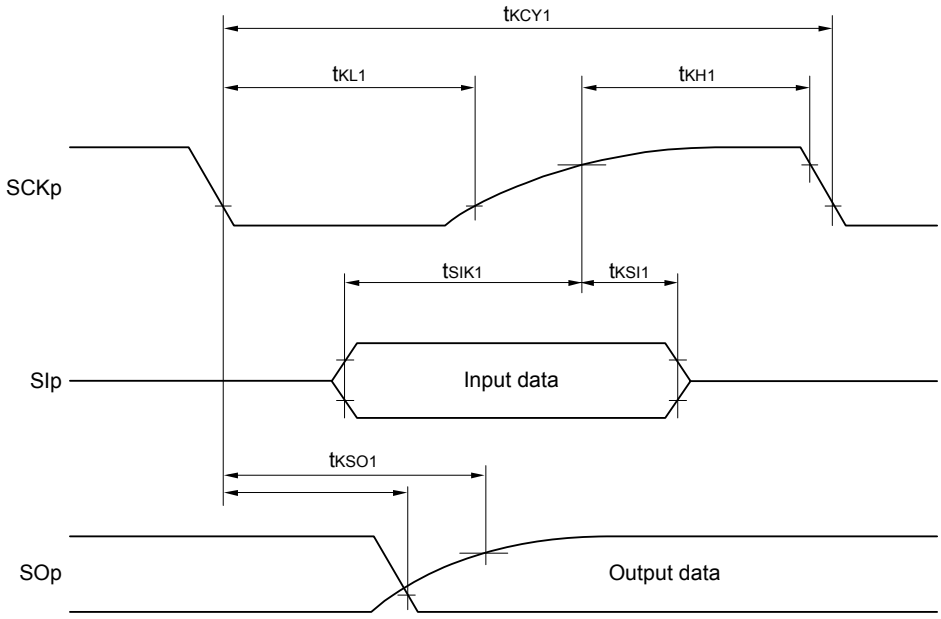
| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | 1150 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |

**Note** Use it with $EV_{DD0} \geq V_b$.

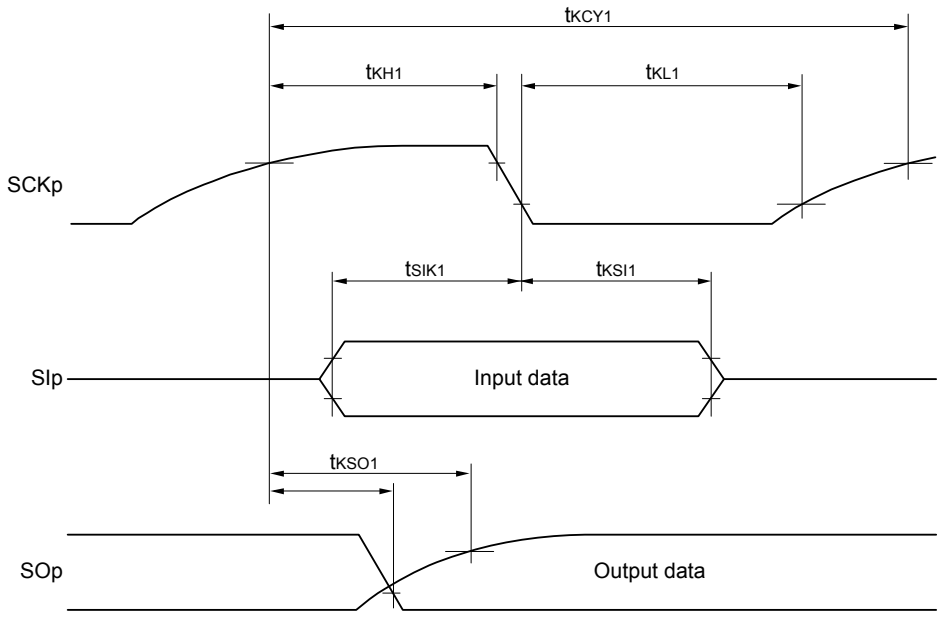
**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

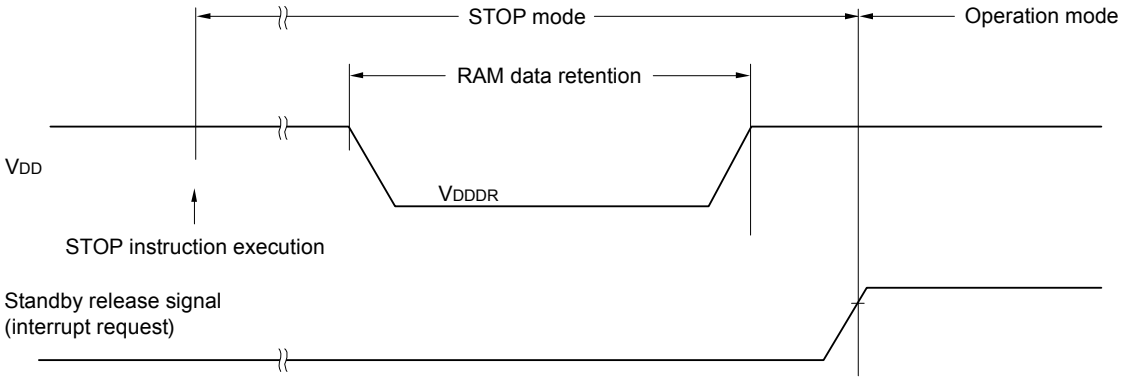
**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

## 2.7 RAM Data Retention Characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites<br>Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years<br>$T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites<br>Notes 1, 2, 3 | | Retained for 1 year<br>$T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years<br>$T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years<br>$T_A$ = 85°C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0}$ = $EV_{DD1}$ | -0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0}$ = $EV_{SS1}$ | -0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8 and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI20 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | -0.3 to $V_{DD}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.4 | 10.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.4 | 10.9 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.0 | 10.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.0 | 10.3 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.2 | 8.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 8.2 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.8 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.8 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.0 | 5.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.0 | 5.6 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 6.6 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.7 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 6.6 | |
| | | | | | | Resonator connection | | 3.6 | 6.7 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.9 | |
| | | | | | | Resonator connection | | 2.2 | 4.0 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.9 | |
| | | | | | | Resonator connection | | 2.2 | 4.0 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.9 | 7.1 | µA |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.1 | |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.1 | 8.8 | |
| | | | | | | Resonator connection | | 5.1 | 8.8 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 13.0 | 58.0 | |
| | | | | | | Resonator connection | | 13.0 | 58.0 | |

(**Notes** and **Remarks** are listed on the next page.)

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note 2 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 1.3 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 150 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI20 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 3 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 3 | | | V |

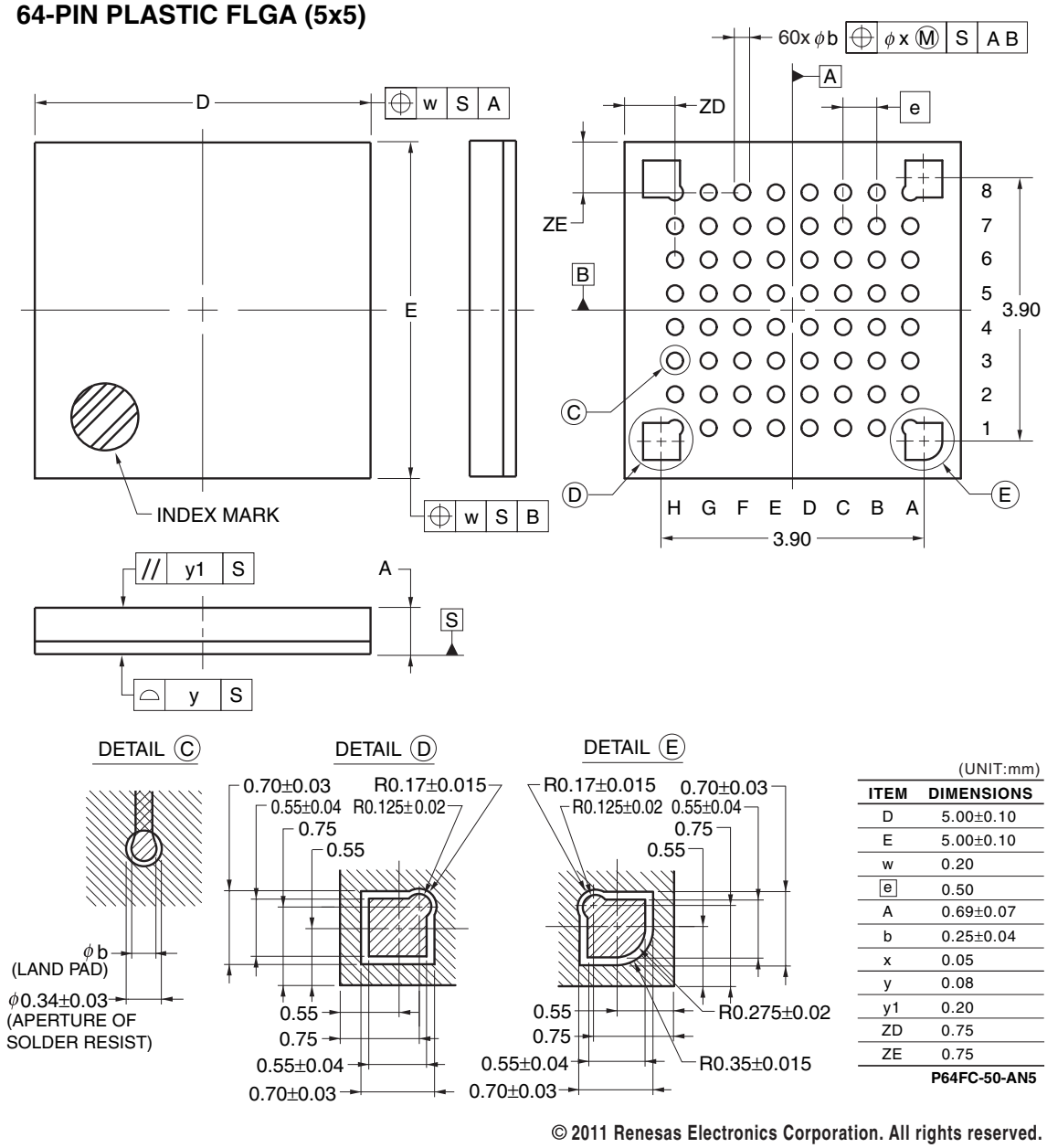
**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
R5F104LKALA, R5F104LLALA
R5F104LCGLA,R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
R5F104LKGLA, R5F104LLGLA

## 64-PIN PLASTIC FLGA (5x5)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 5.00±0.10 |
| E | 5.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.25±0.04 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

P64FC-50-AN5

| REVISION HISTORY | RL78/G14 Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 3.20 | Jan 05, 2015 | p.135, 137, 139, 141, 143, 145 | Modification of specifications in 3.3.2 Supply current characteristics |
| | | p.197 | Modification of part number in 4.7 52-pin products |
| 3.30 | Aug 12, 2016 | p.143, 145 | Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics |