Renesas Electronics America Inc - R5F104LEAFP#X0 Datasheet

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104leafp-x0

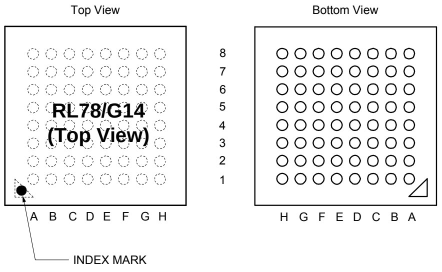
(2/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	A	R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0 R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0
		D	R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0 R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0
		G	R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0 R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0
44 pins	44-pin plastic LQFP (10 × 10, 0.8 mm pitch)	A	R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0 R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0
		D	R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0 R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0
		G	R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0 R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

- 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)



	A	B	C	D	E	F	G	H	
8	EVDD0	EVSS0	P121/X1	P122/X2/EXCLK	P137/INTP0	P123/XT1	P124/XT2/EXCLKS	P120/ANI19/VCOUT0 Note 1	8
7	P60/SCLA0	VDD	VSS	REGC	$\overline{\text{RESET}}$	P01/TO00/TRGCLKB/TRJIO0	P00/TI00/TRGCLKA/(TRJO0)	P140/PCLBUZ0/INTP6	7
6	P61/SDAA0	P62/$\overline{\text{SSI00}}$	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/SO10/TxD1	P141/PCLBUZ1/INTP7	6
5	P77/KR7/INTP11/(TXD2)	P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/SI10/RxD1/SDA10	P04/SCK10/SCL10	P130	P20/ANI0/AVREFP	5
4	P75/KR5/INTP9/SCK01/SCL01	P76/KR6/INTP10/(RXD2)	P52/(INTP1)	P54/(INTP3)	P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 Note 1/(SI00)/(RXD0)	P21/ANI1/AVREFM	P22/ANI2/ANO0 Note 1	P23/ANI3/ANO1 Note 1	4
3	P70/KR0/SCK21/SCL21	P73/KR3/SO01	P74/KR4/INTP8/SI01/SDA01	P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 Note 1/(SO00)/(TXD0)	P15/SCK20/SCL20/TRDIOB0/(SDAA0)	P12/SO11/TRDIOB1/IVREF1 Note 1/(INTP5)/(TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0	P72/KR2/SO21	P71/KR1/SI21/SDA21	P06/(INTP11)/(TRJIO0)	P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)	P11/SI11/SDA11/TRDIOC1/(RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)	P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB	P55/(PCLBUZ1)/(SCK00)/(INTP4)	P13/TxD2/SO20/TRDIOA1/IVCMP1 Note 1	P10/SCK11/SCL11/TRDIOD1	P146	P147/ANI18/VCOUT1 Note 1	1
	A	B	C	D	E	F	G	H	

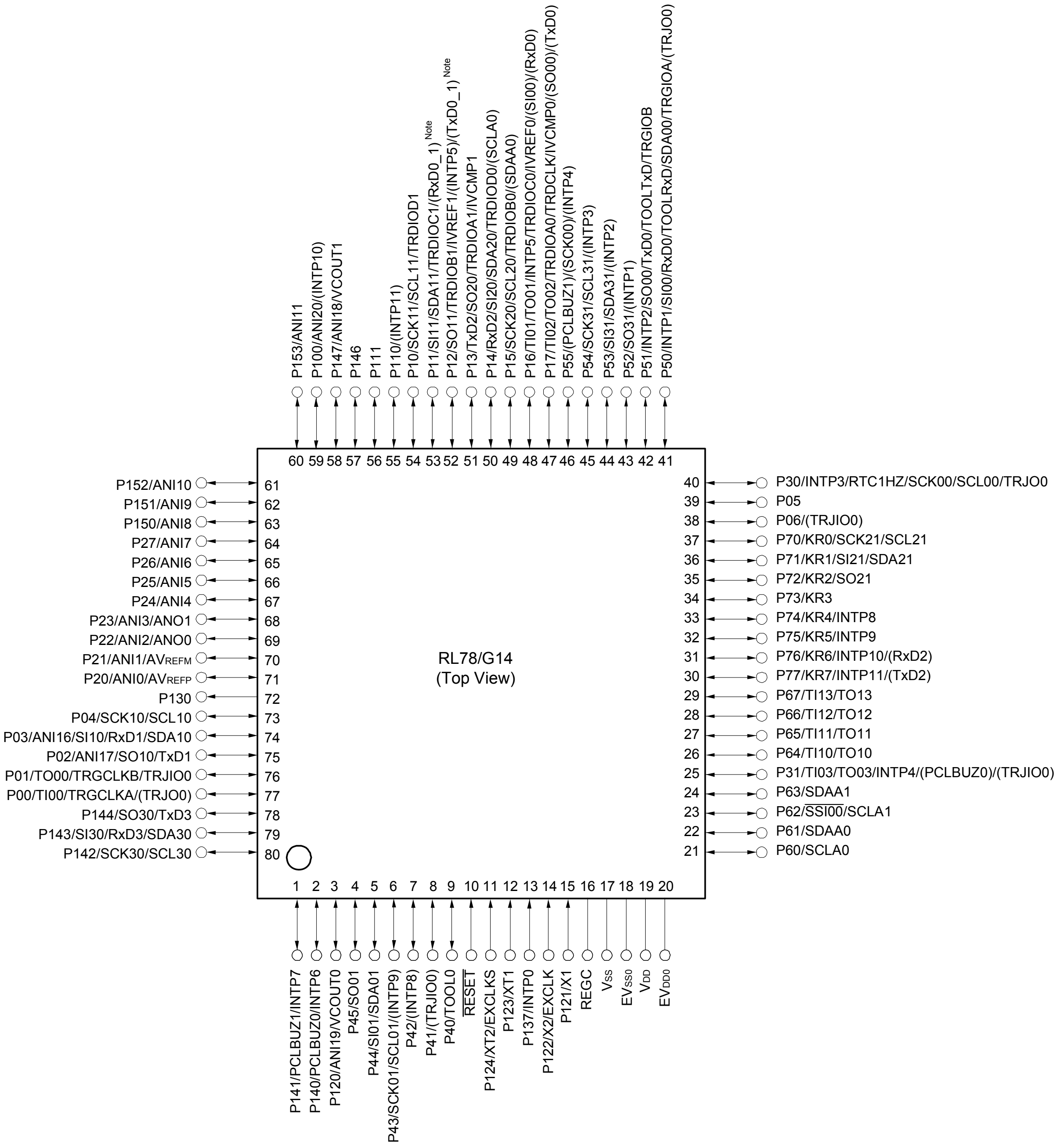
Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.
Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.
Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

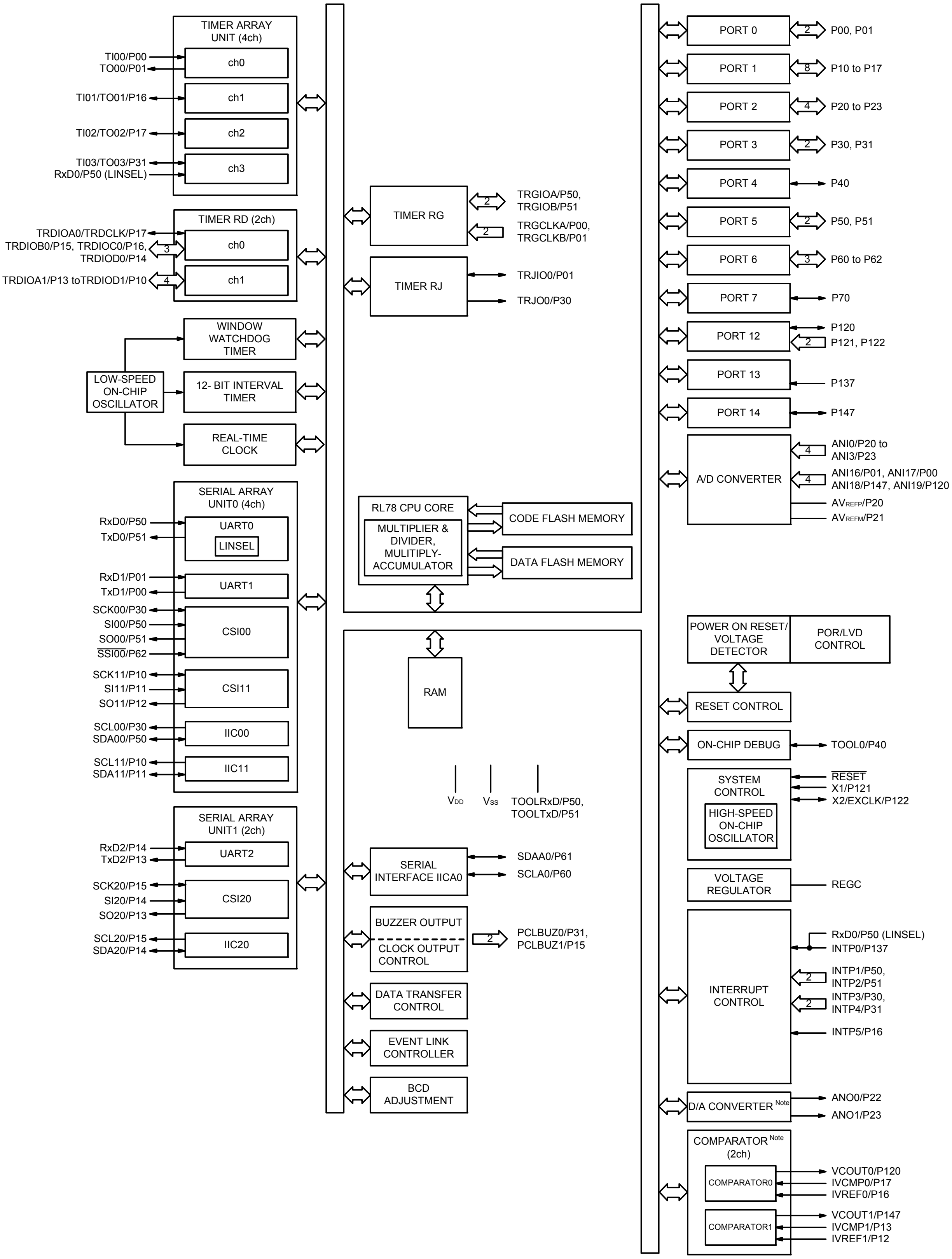
Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.

(T_A = -40 to +85°C, 1.6 V $\leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			1.8 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V $\leq EV_{DD0} <$ 1.8 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27, P150 to P156	1.6 V $\leq V_{DD} \leq$ 5.5 V, I_{OH2} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P156	1.6 V $\leq V_{DD} \leq$ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V $\leq EV_{DD0} \leq$ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 32 MHz
$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 4 MHz

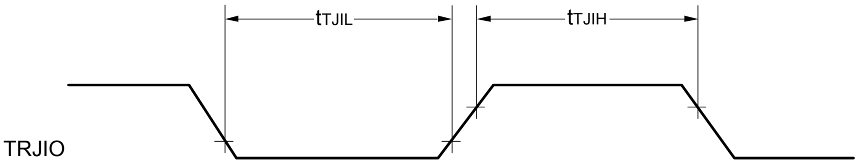
Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

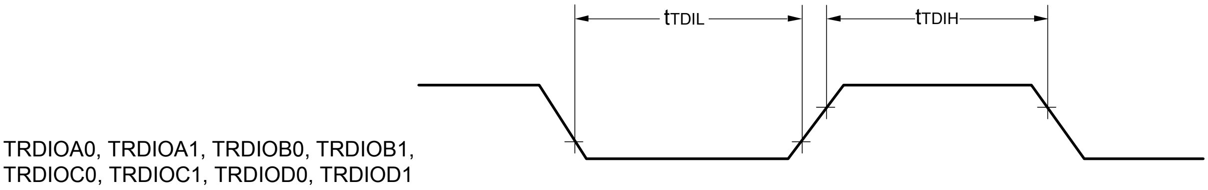
Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

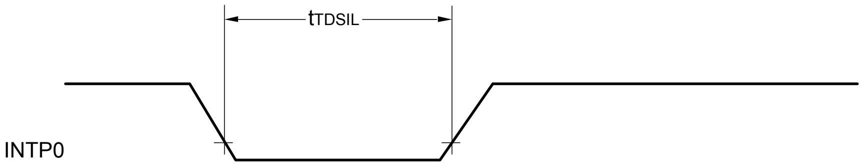
Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

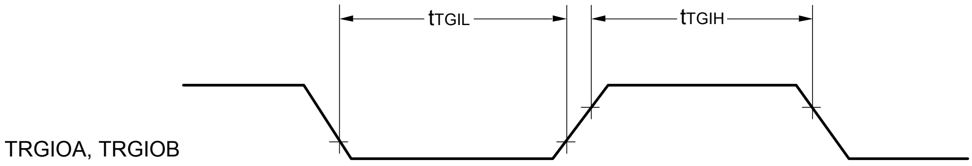
Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C


t_{TJIL}
t_{TJIH}
TRJIO


t_{TDIL}
t_{TDIH}
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1


t_{TDSIL}
INTP0


t_{TGIL}
t_{TGIH}
TRGIOA, TRGIOB

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

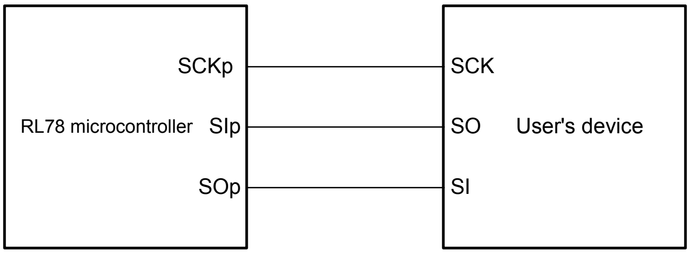
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SSI00}}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		400		400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		ns
$\overline{\text{SSI00}}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		400		400		ns

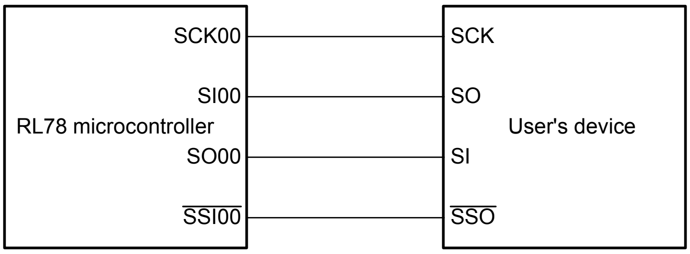
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-)= AVREFM
ANI0 to ANI14	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI20	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		—

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	1.8 V ≤ AVREFP ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 4		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	µs
			1.6 V ≤ VDD ≤ 5.5 V	57		95	µs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD Note 3	1.8 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 4			±0.50	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD Note 3	1.8 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	1.8 V ≤ AVREFP ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	1.8 V ≤ AVREFP ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 4			±2.0	LSB
Analog input voltage	VAIN	ANI2 to ANI14		0		AVREFP	V
		Internal reference voltage (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VBGR Note 5			V
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VTMPS25 Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. Values when the conversion time is set to 57 µs (min.) and 95 µs (max.).

Note 5. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5		1.2	±8.5	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	µs
			1.6 V ≤ VDD ≤ 5.5 V	57		95	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AVREFP and EVDD0	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EVDD0 ≤ AVREFP ≤ VDD, the MAX. values are as follows.

Overall error:	Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
Zero-scale error/Full-scale error:	Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
Integral linearity error/ Differential linearity error:	Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. When AVREFP < EVDD0 ≤ VDD, the MAX. values are as follows.

Overall error:	Add ±4.0 LSB to the MAX. value when AVREFP = VDD.
Zero-scale error/Full-scale error:	Add ±0.20%FSR to the MAX. value when AVREFP = VDD.
Integral linearity error/ Differential linearity error:	Add ±2.0 LSB to the MAX. value when AVREFP = VDD.

Note 5. When the conversion time is set to 57 µs (min.) and 95 µs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V [Note 3]		1.2	±10.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V [Note 3]			±0.85	%FSR
Full-scale error [Notes 1, 2]	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V [Note 3]			±0.85	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V [Note 3]			±6.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V [Note 3]			±2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} [Note 4]			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 4. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		V_{LVD12}	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		V_{LVD13}	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105°C)

This chapter describes the following electrical specifications.
Target products G: Industrial applications T_A = -40 to +105°C
R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

Caution 4. Please contact Renesas Electronics sales office for derating of operation under T_A = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G14 is used in the range of T_A = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)**.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

3.2.2 On-chip oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
		+85 to +105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(4) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 2.4 V ≤ $EV_{DD0} = EV_{DD1} \le V_{DD} \le$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		µA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		µA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		µA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		µA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, $AV_{REFP} = V_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, $AV_{REFP} = V_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		µA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		µA
D/A converter operating current	I_{DAC} Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	I_{CMP} Notes 1, 12, 13	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		µA
			Comparator high-speed mode		6.5		µA
			Comparator low-speed mode		1.7		µA
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		µA
			Comparator high-speed mode		4.0		µA
			Comparator low-speed mode		1.3		µA
LVD operating current	I_{LVD} Notes 1, 7				0.08		µA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, $AV_{REFP} = V_{DD}$ = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 24		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 36		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

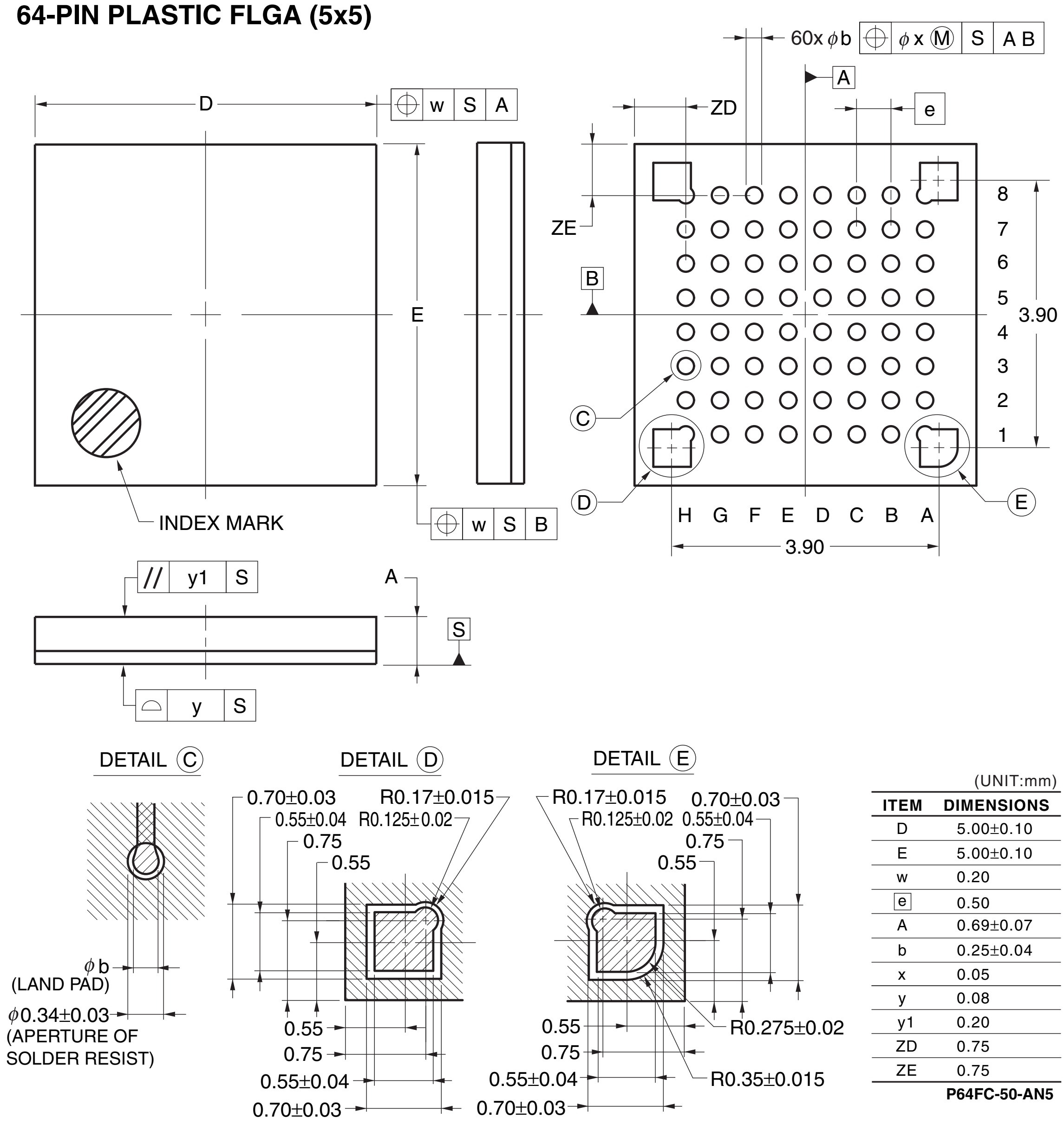
Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
R5F104LKALA, R5F104LLALA
R5F104LCGLA,R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
R5F104LKGLA, R5F104LLGLA

64-PIN PLASTIC FLGA (5x5)



(UNIT:mm)

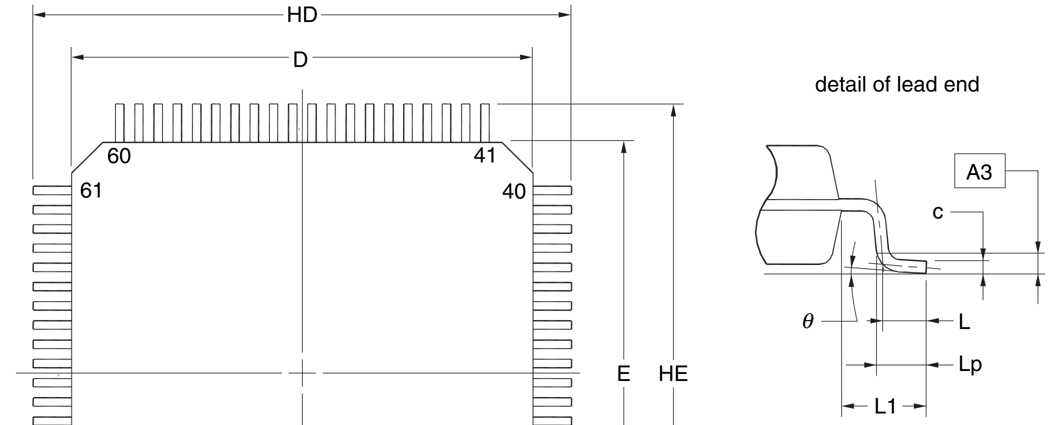
ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5

4.9 80-pin products

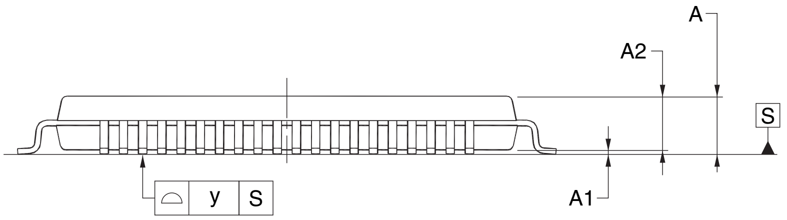
R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
R5F104MFDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

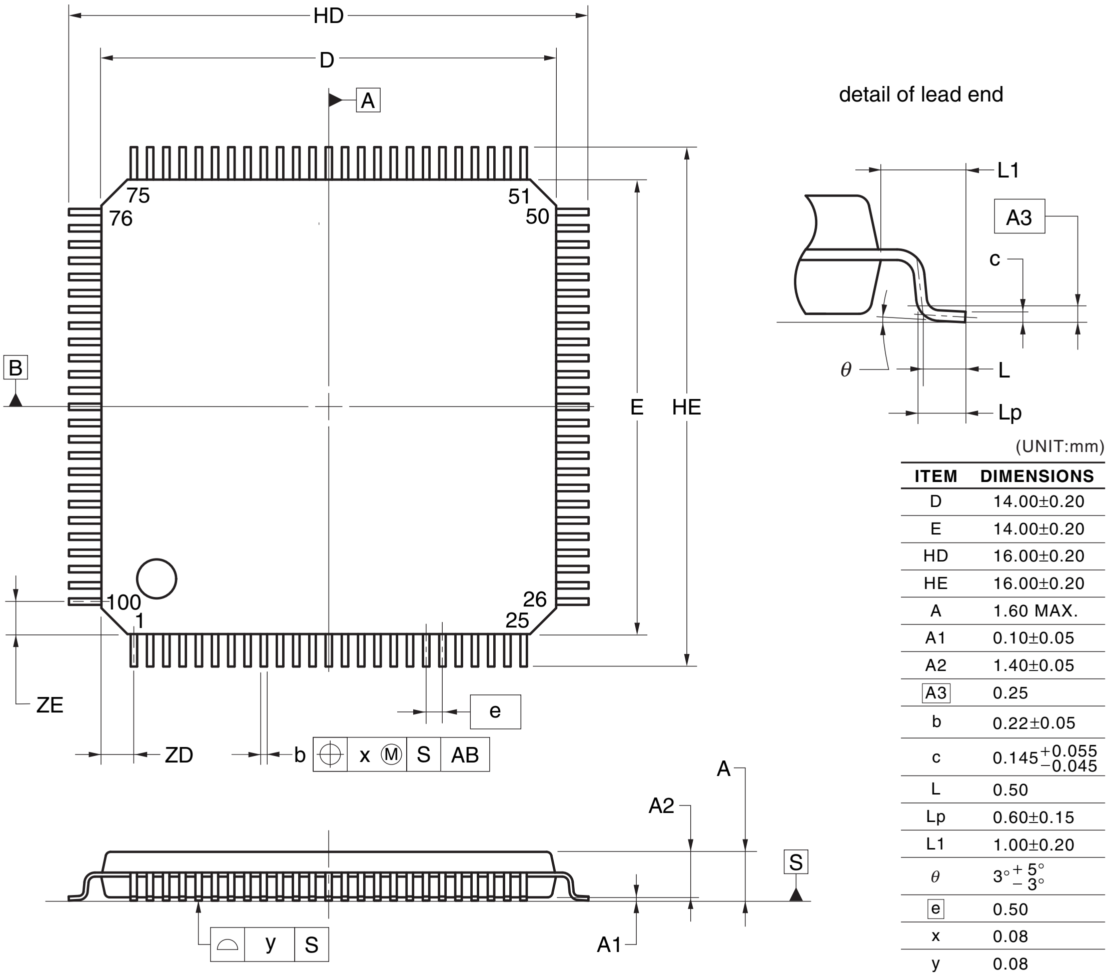


NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4.10 100-pin products

R5F104PFAFB, R5F104PGAFB, R5F104PHAFB, R5F104PJAFB
R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.