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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

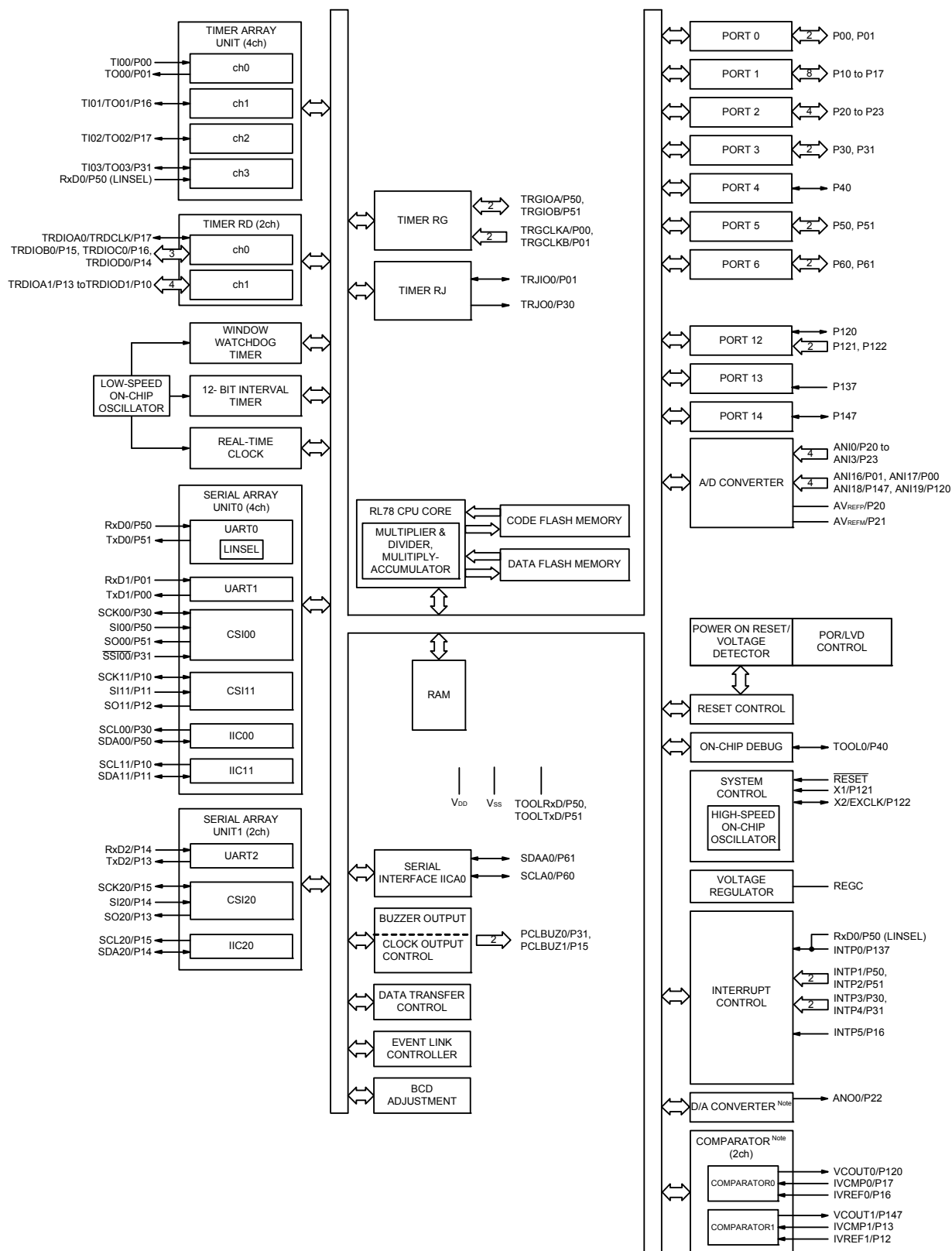
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ledfb-30

1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		SCK00, SCK01, SCK10,:	Serial clock input/output
ANO0, ANO1:	Analog output	SCK11, SCK20, SCK21,	
AVREFM:	A/D converter reference potential (– side) input	SCK30, SCK31	
AVREFP:	A/D converter reference potential (+ side) input	SCLA0, SCLA1,:	Serial clock input/output
EVDD0, EVDD1:	Power supply for port	SCL00, SCL01, SCL10, SCL11,:	Serial clock output
EVSS0, EVSS1:	Ground for port	SCL20, SCL21, SCL30,	
EXCLK:	External clock input (main system clock)	SCL31	
EXCLKS:	External clock input (subsystem clock)	SDAA0, SDAA1, SDA00,:	Serial data input/output
INTP0 to INTP11:	External interrupt input	SDA01, SDA10, SDA11,	
IVCMP0, IVCMP1:	Comparator input	SDA20, SDA21, SDA30,	
IVREF0, IVREF1:	Comparator reference input	SDA31	
KR0 to KR7:	Key return	SI00, SI01, SI10, SI11,:	Serial data input
P00 to P06:	Port 0	SI20, SI21, SI30, SI31	
P10 to P17:	Port 1	SO00, SO01, SO10,:	Serial data output
P20 to P27:	Port 2	SO11, SO20, SO21,	
P30, P31:	Port 3	SO30, SO31	
P40 to P47:	Port 4	$\overline{\text{SSI00}}$:	Serial interface chip select input
P50 to P57:	Port 5	TI00 to TI03,:	Timer input
P60 to P67:	Port 6	TI10 to TI13	
P70 to P77:	Port 7	TO00 to TO03,:	Timer output
P80 to P87:	Port 8	TO10 to TO13, TRJ00	
P100 to P102:	Port 10	TOOL0:	Data input/output for tool
P110, P111:	Port 11	TOOLRxD, TOOLTxD:	Data input/output for external device
P120 to P124:	Port 12	TRDCLK, TRGCLKA,:	Timer external input clock
P130, P137:	Port 13	TRGCLKB	
P140 to P147:	Port 14	TRDIOA0, TRDIOB0,:	Timer input/output
P150 to P156:	Port 15	TRDIOC0, TRDIOD0,	
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	TRDIOA1, TRDIOB1,	
REGC:	Regulator capacitance	TRDIOC1, TRDIOD1,	
$\overline{\text{RESET}}$:	Reset	TRGIOA, TRGIOB, TRJIO0	
RTC1HZ:	Real-time clock correction clock (1 Hz) output	TxD0 to TxD3:	Transmit data
		VCOUT0, VCOUT1:	Comparator output
		VDD:	Power supply
		VSS:	Ground
		X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

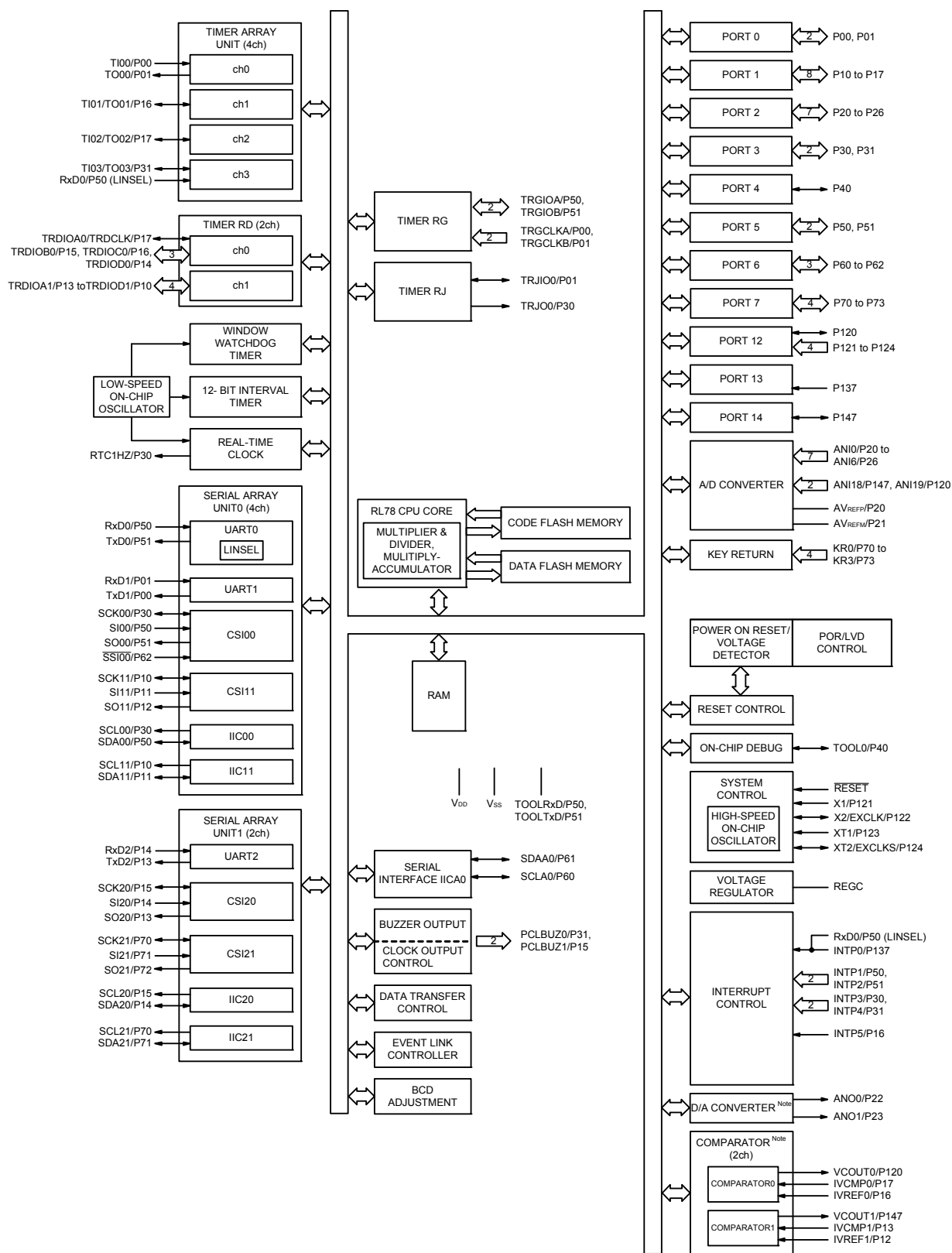
1.5 Block Diagram

1.5.1 30-pin products



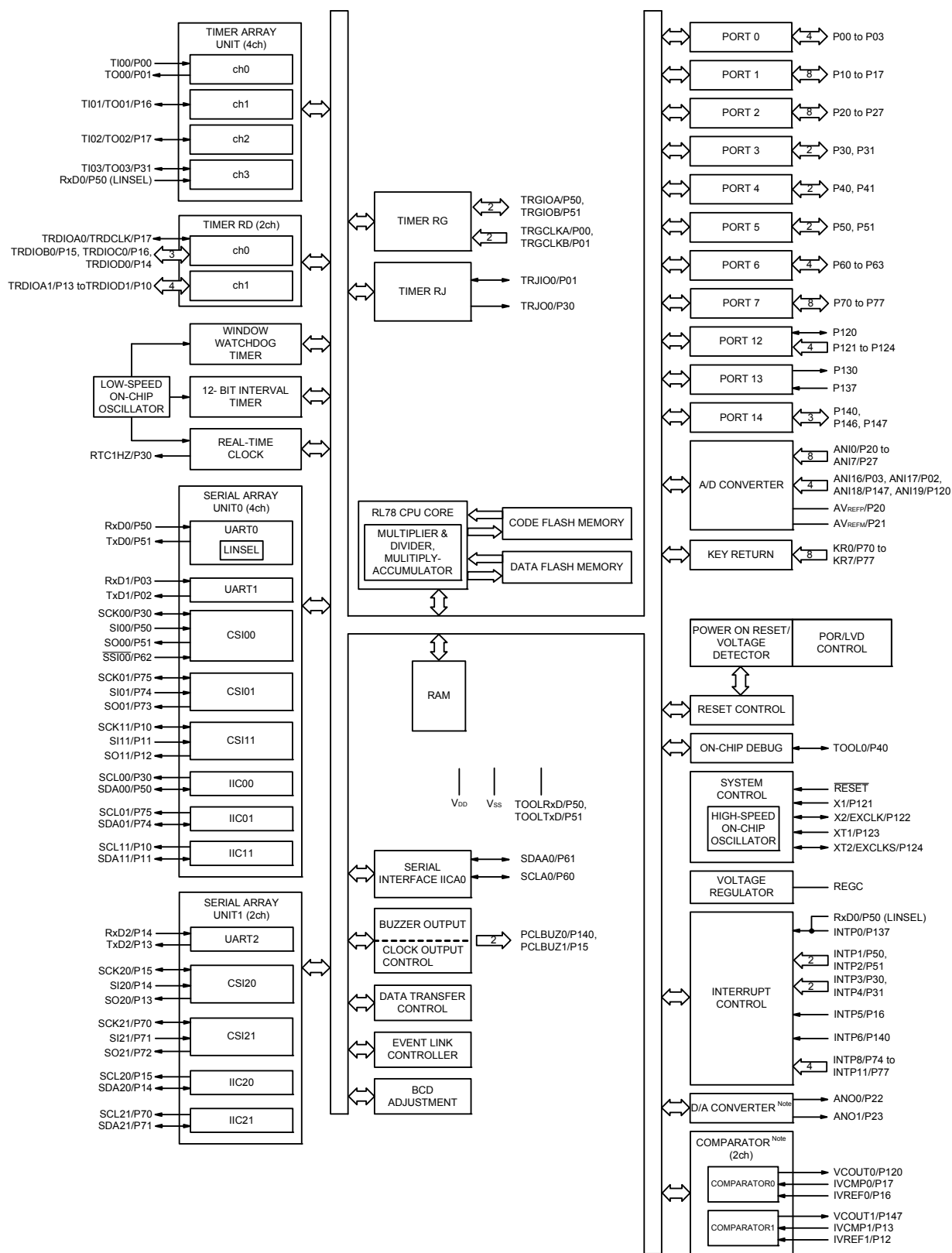
Note Mounted on the 96 KB or more code flash memory products.

1.5.4 40-pin products



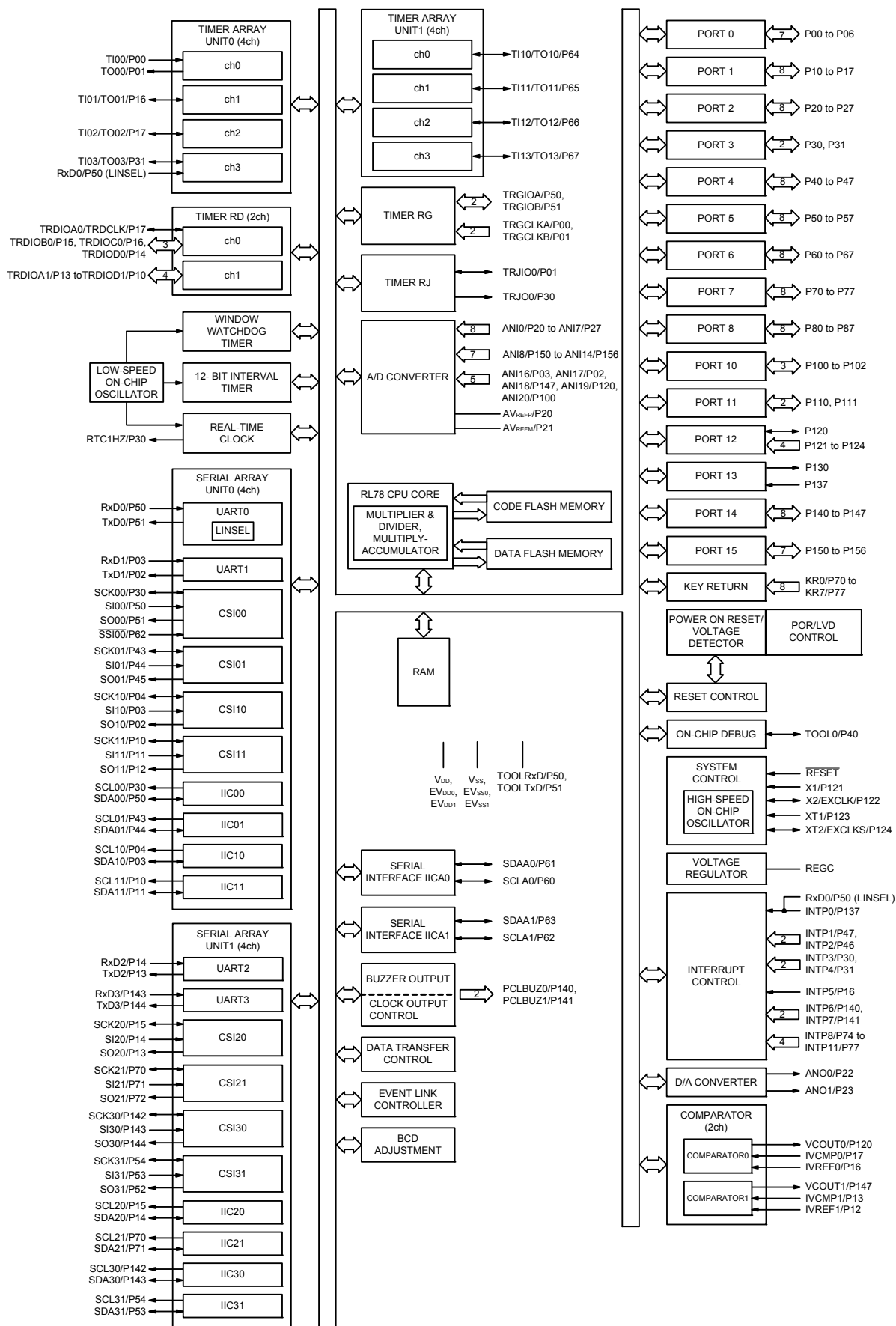
Note Mounted on the 96 KB or more code flash memory products.

1.5.7 52-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.5.10 100-pin products



Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)****(2/3)**

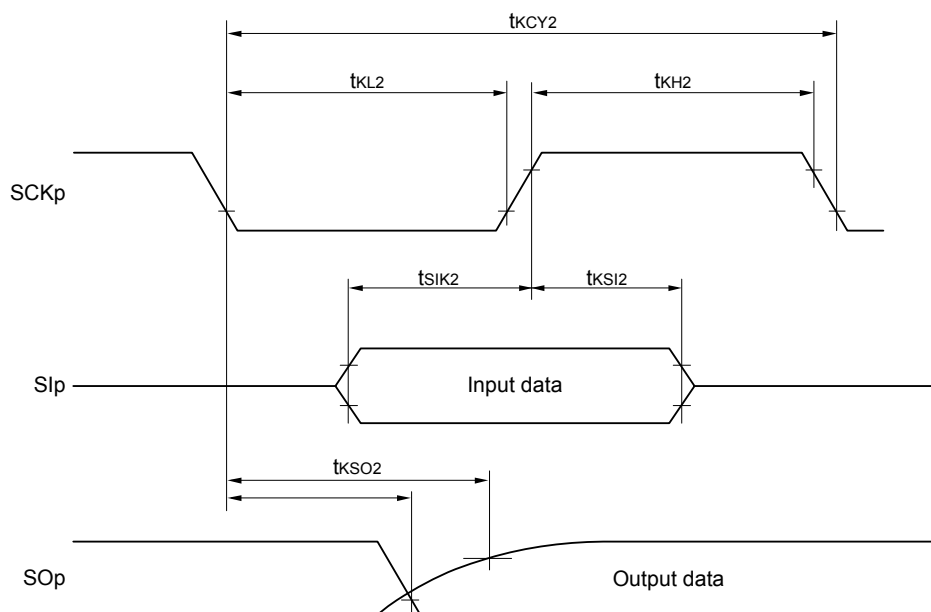
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	t _{KSI1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

Note 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1.**Note 2.** Use it with EV_{DD0} ≥ V_b.

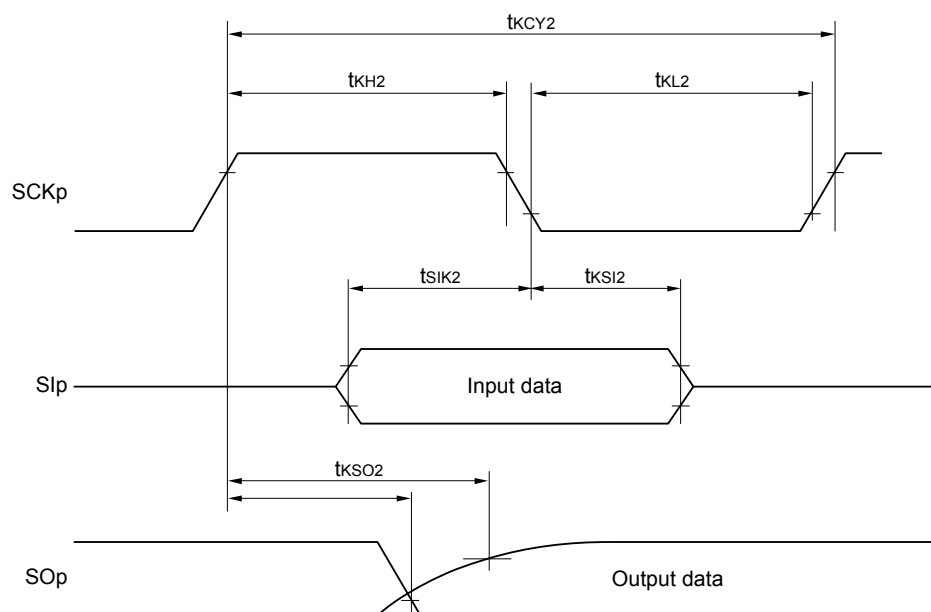
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ EVDD0 ≤ 5.5 V		-60.0	mA
	IOH2	Per pin for P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ VDD ≤ 5.5 V		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
 <Example> Where n = 80% and IOH = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{DD0}				1 μA
	ILI _{H2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{DD}				1 μA
	ILI _{H3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{DD}	In input port or external clock input			1 μA
				In resonator connection			10 μA
Input leakage current, low	ILI _{L1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0}				-1 μA
	ILI _{L2}	P20 to P27, P137, P150 to P156, <u>RESET</u>	V _I = V _{SS}				-1 μA
	ILI _{L3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{SS}	In input port or external clock input			-1 μA
				In resonator connection			-10 μA
On-chip pull-up resistance	R _U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100 kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	4.86	mA	
					VDD = 3.0 V		0.79	4.86		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	4.17		
					VDD = 3.0 V		0.49	4.17		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.82		
					VDD = 3.0 V		0.62	3.82		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	3.25		
					VDD = 3.0 V		0.4	3.25		
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	2.28		
					VDD = 3.0 V		0.38	2.28		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	2.65	mA	
					Resonator connection		0.40	2.77		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30	2.65		
					Resonator connection		0.40	2.77		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	1.36		
					Resonator connection		0.25	1.46		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	1.36		
					Resonator connection		0.25	1.46		
		Subsystem clock operation		fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA	
					Resonator connection		0.47	0.85		
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66		
					Resonator connection		0.53	0.85		
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35		
					Resonator connection		0.56	2.54		
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08		
					Resonator connection		0.80	4.27		
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09		
					Resonator connection		1.74	8.28		
				fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		6.00	51.00		
					Resonator connection		6.00	51.00		
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19	0.57	μA
			TA = +25°C					0.25	0.57	
			TA = +50°C					0.33	2.26	
			TA = +70°C					0.52	3.99	
			TA = +85°C					1.46	8.00	
			TA = +105°C					5.50	50.00	

(Notes and Remarks are listed on the next page.)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V	2.6 Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V	1.2 Note 4	Mbps
			2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V	0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using fmCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} $\geq 4/f_{\text{CLK}}$	4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω	600		ns
			2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω	1000		ns
			2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω	2300		ns
SCKp high-level width	t _{KH1}	4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω		t _{KCY1} /2 - 150		ns
		2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω		t _{KCY1} /2 - 340		ns
		2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω		t _{KCY1} /2 - 916		ns
SCKp low-level width	t _{KL1}	4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω		t _{KCY1} /2 - 24		ns
		2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω		t _{KCY1} /2 - 36		ns
		2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω		t _{KCY1} /2 - 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +105°C, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

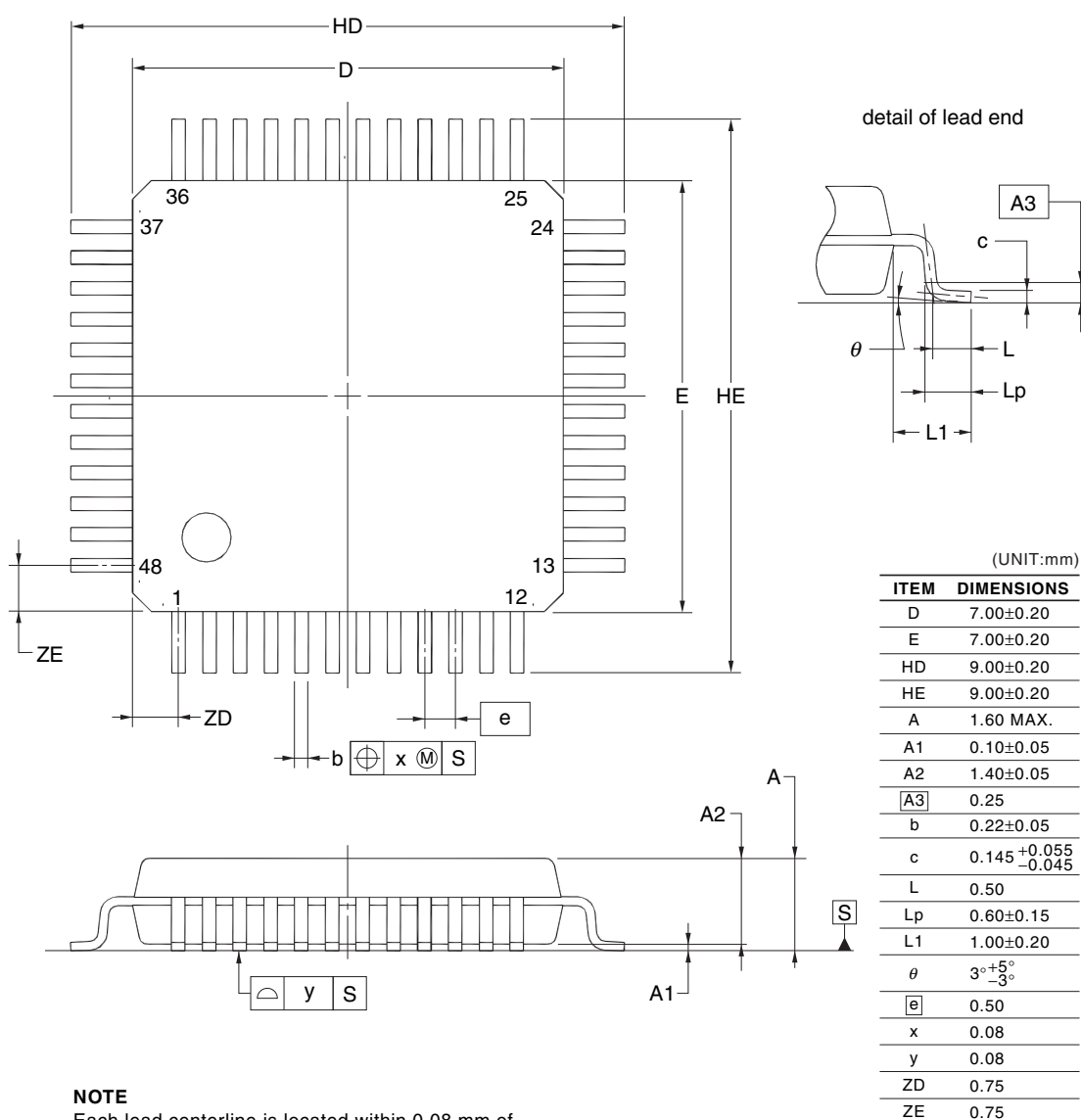
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time Note 1	tkCY2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	$24\text{ MHz} < \text{fMCK}$	$28/\text{fMCK}$	ns
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	$24/\text{fMCK}$	ns
			$8\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	$20/\text{fMCK}$	ns
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	$16/\text{fMCK}$	ns
			$\text{fMCK} \leq 4\text{ MHz}$	$12/\text{fMCK}$	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	$24\text{ MHz} < \text{fMCK}$	$40/\text{fMCK}$	ns
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	$32/\text{fMCK}$	ns
			$16\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	$28/\text{fMCK}$	ns
			$8\text{ MHz} < \text{fMCK} \leq 16\text{ MHz}$	$24/\text{fMCK}$	ns
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	$16/\text{fMCK}$	ns
			$\text{fMCK} \leq 4\text{ MHz}$	$12/\text{fMCK}$	ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$	$24\text{ MHz} < \text{fMCK}$	$96/\text{fMCK}$	ns
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	$72/\text{fMCK}$	ns
			$16\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	$64/\text{fMCK}$	ns
			$8\text{ MHz} < \text{fMCK} \leq 16\text{ MHz}$	$52/\text{fMCK}$	ns
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	$32/\text{fMCK}$	ns
			$\text{fMCK} \leq 4\text{ MHz}$	$20/\text{fMCK}$	ns
SCKp high-/low-level width	tkH2, tkL2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	tkCY2/2 - 24		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	tkCY2/2 - 36		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$	tkCY2/2 - 100		ns
Slp setup time (to SCKp↑) Note 2	tsIK2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	$1/\text{fMCK} + 40$		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	$1/\text{fMCK} + 40$		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$	$1/\text{fMCK} + 60$		ns
Slp hold time (from SCKp↑) Note 3	tsIS2		$1/\text{fMCK} + 62$		ns
Delay time from SCKp↓ to SOp output Note 4	tkSO2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			$2/\text{fMCK} + 240$
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			$2/\text{fMCK} + 428$
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_v = 5.5\text{ k}\Omega$			$2/\text{fMCK} + 1146$

(Notes, Caution, and Remarks are listed on the next page.)

4.6 48-pin products

R5F104GAAFB, R5F104GCAFB, R5F104GDAFB, R5F104GEAFB, R5F104GFAFB, R5F104GGAFB,
 R5F104GHAFB, R5F104GJAFB
 R5F104GADFB, R5F104GCDFB, R5F104GDDFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB,
 R5F104GHDFB, R5F104JDFB
 R5F104GAGFB, R5F104GCGFB, R5F104GDGFB, R5F104GEGFB, R5F104GFGFB, R5F104GGGFB,
 R5F104GHGFB, R5F104GJGFB

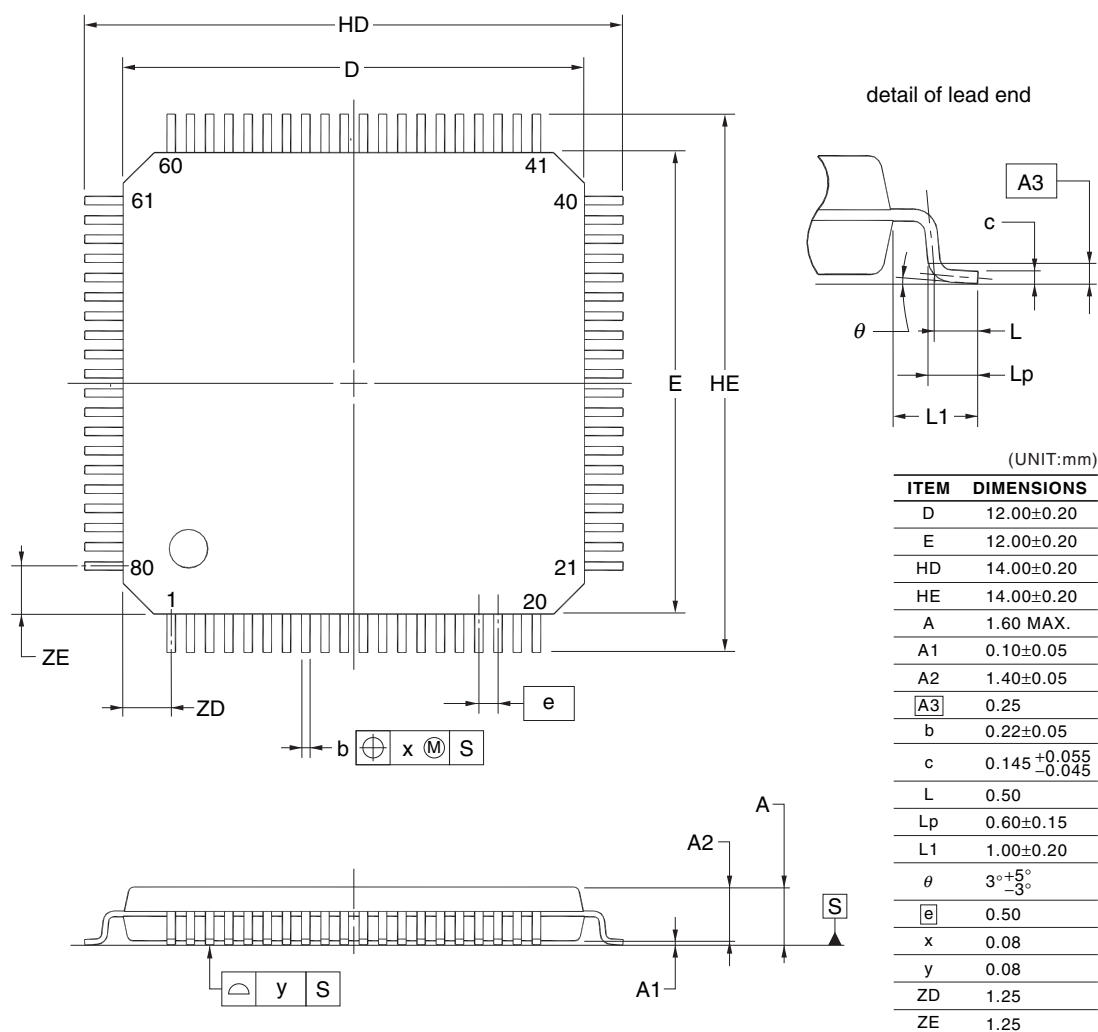
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



4.9 80-pin products

R5F104MFAFB, R5F104MGAFB, R5F104MHA FB, R5F104MJAFB
 R5F104MDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
 R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

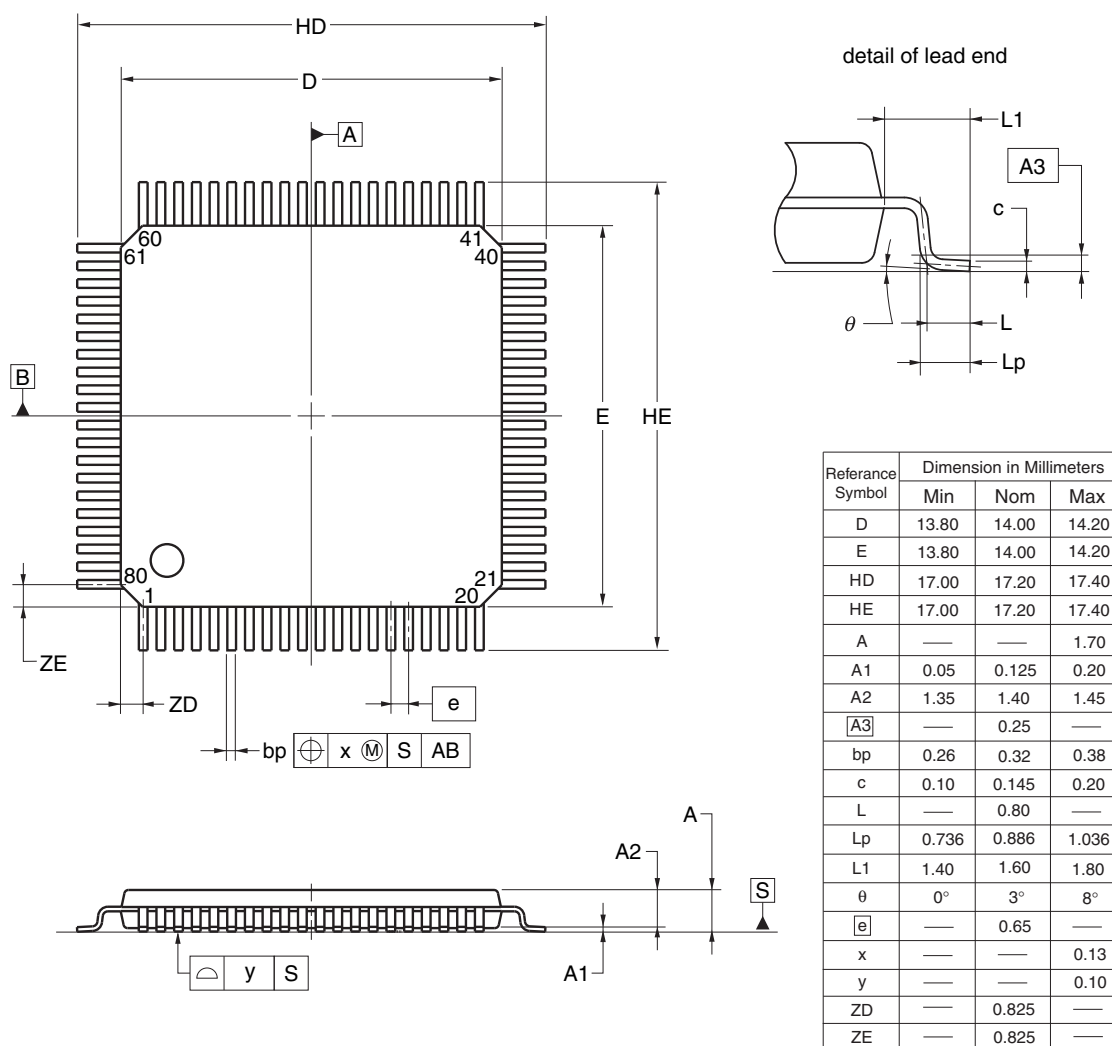


NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

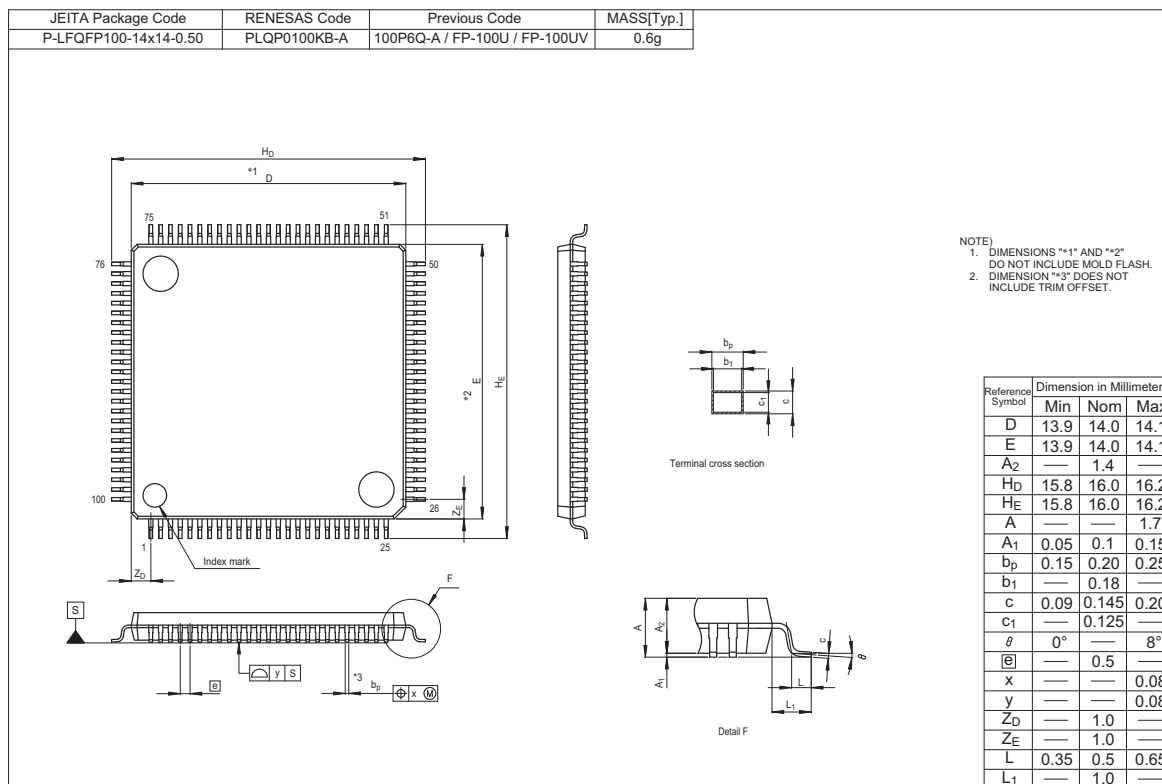
R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJFAFA
 R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
 R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
 R5F104MKAFA, R5F104MLAFA
 R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



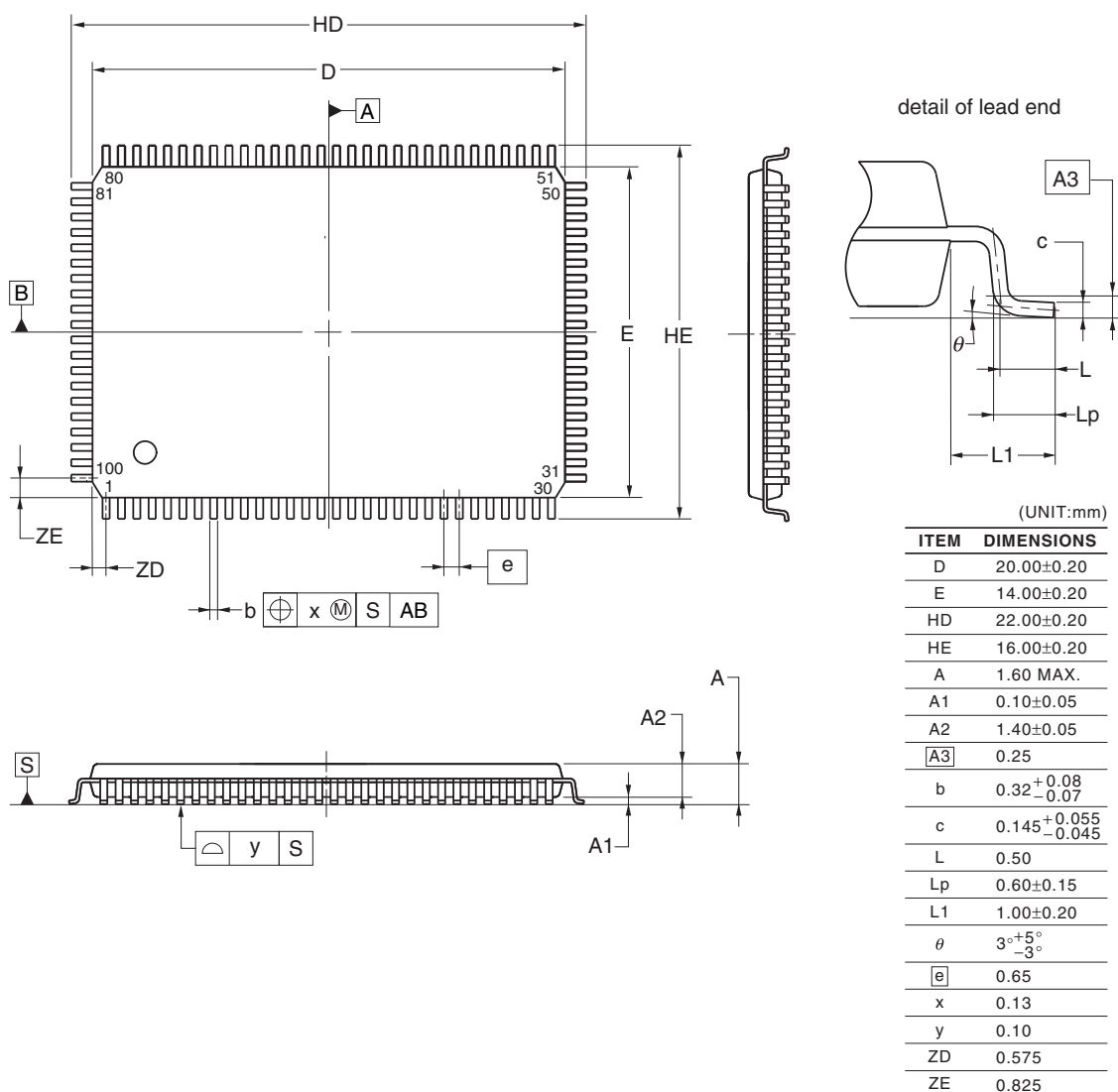
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R5F104PKAFB, R5F104PLAFB
R5F104PKGFB, R5F104PLGFB



R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJFAFA
 R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFA
 R5F104PFGFA, R5F104PGGFA, R5F104PHGFA, R5F104PJGFA
 R5F104PKAFA, R5F104PLAFA
 R5F104PKGFA, R5F104PLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



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