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What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
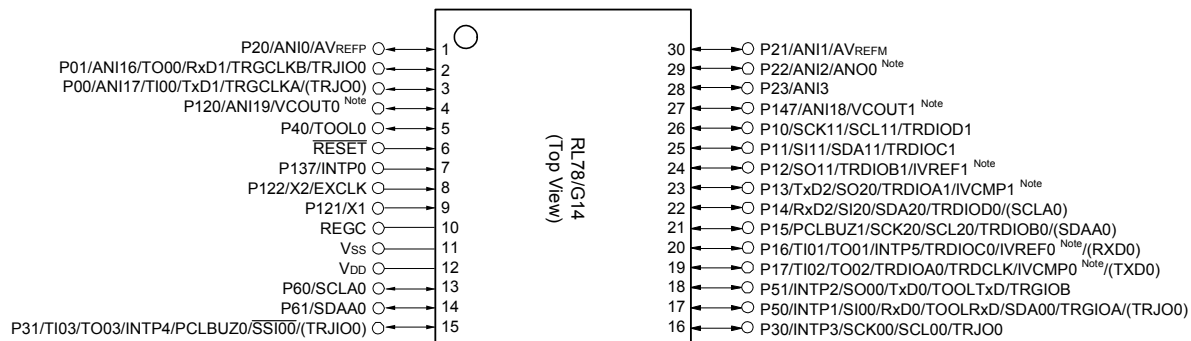
Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104lgafp-v0

1.3   Pin Configuration (Top View)

1.3.1   30-pin products

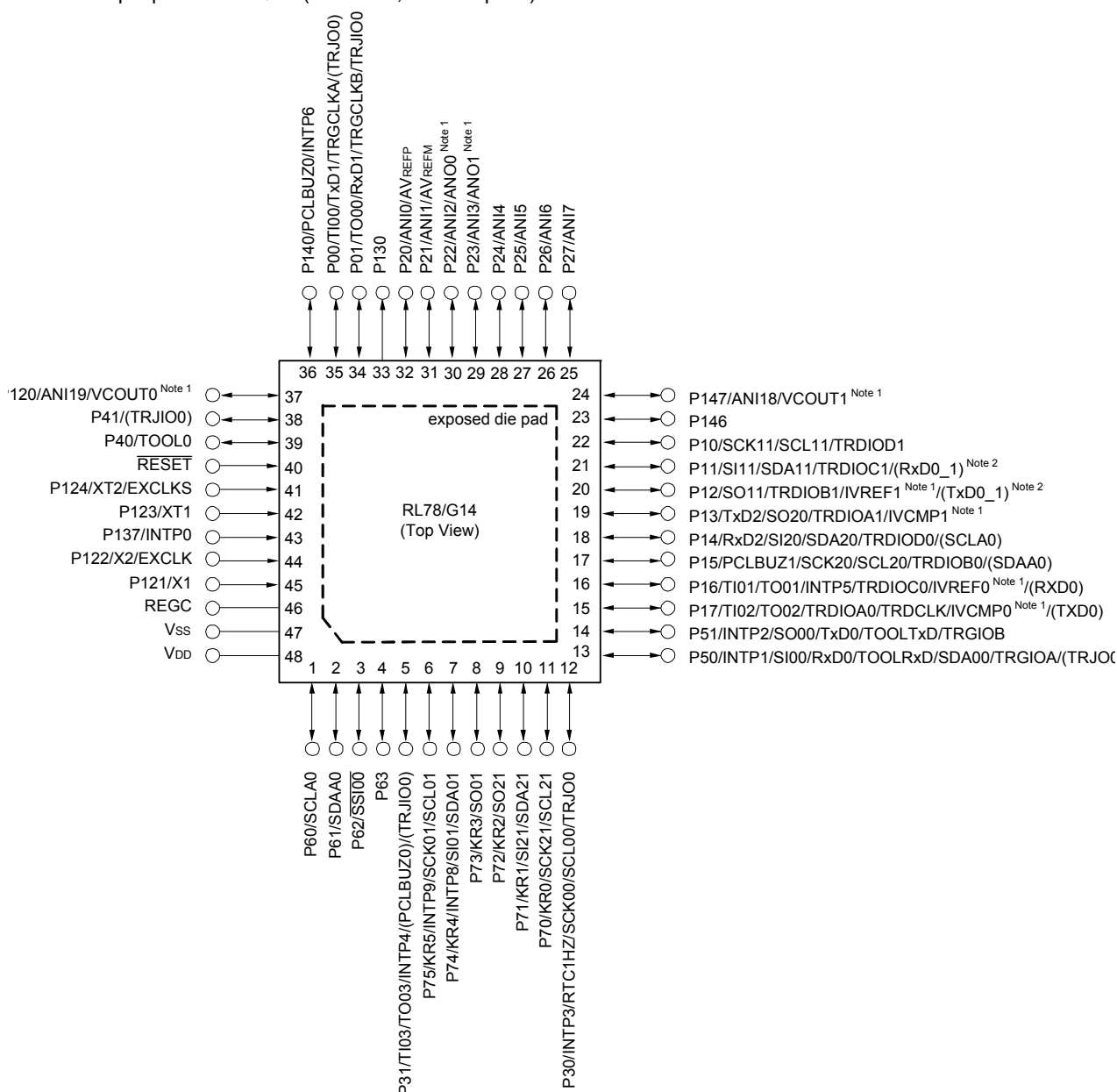• 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

Pin	Left signal	Pin	Right signal
1	P20/ANI0/AV$_{REFP}$	30	P21/ANI1/AV$_{REFM}$
2	P01/ANI16/TO00/RxD1/TRGCLKB/TRJIO0	29	P22/ANI2/ANO0 [Note]
3	P00/ANI17/TI00/TxD1/TRGCLKA/(TRJO0)	28	P23/ANI3
4	P120/ANI19/VCOUT0 [Note]	27	P147/ANI18/VCOUT1 [Note]
5	P40/TOOL0	26	P10/SCK11/SCL11/TRDIOD1
6	RESET	25	P11/SI11/SDA11/TRDIOC1
7	P137/INTP0	24	P12/SO11/TRDIOB1/IVREF1 [Note]
8	P122/X2/EXCLK	23	P13/TxD2/SO20/TRDIOA1/IVCMP1 [Note]
9	P121/X1	22	P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
10	REGC	21	P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
11	V$_{SS}$	20	P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 [Note]/(RXD0)
12	V$_{DD}$	19	P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 [Note]/(TXD0)
13	P60/SCLA0	18	P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
14	P61/SDAA0	17	P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)
15	P31/TI03/TO03/INTP4/PCLBUZ0/SSI00/(TRJIO0)	16	P30/INTP3/SCK00/SCL00/TRJO0

RL78/G14
(Top View)

Note   Mounted on the 96 KB or more code flash memory products.

Caution   **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1.   For pin identification, see **1.4 Pin Identification**.

Remark 2.   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Top pins (36 to 25):
- 36 P140/PCLBUZ0/INTP6
- 35 P00/TI00/TxD1/TRGCLKA/(TRJO0)
- 34 P01/TO00/RxD1/TRGCLKB/TRJIO0
- 33 P130
- 32 P20/ANI0/AVREFP
- 31 P21/ANI1/AVREFM
- 30 P22/ANI2/ANO0 Note 1
- 29 P23/ANI3/ANO1 Note 1
- 28 P24/ANI4
- 27 P25/ANI5
- 26 P26/ANI6
- 25 P27/ANI7

Left pins (37 to 48):
- 37 P120/ANI19/VCOUT0 Note 1
- 38 P41/(TRJIO0)
- 39 P40/TOOL0
- 40 RESET
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 Vss
- 48 VDD

Center: exposed die pad — RL78/G14 (Top View)

Right pins (24 to 13):
- 24 P147/ANI18/VCOUT1 Note 1
- 23 P146
- 22 P10/SCK11/SCL11/TRDIOD1
- 21 P11/SI11/SDA11/TRDIOC1/(RxD0_1) Note 2
- 20 P12/SO11/TRDIOB1/IVREF1 Note 1/(TxD0_1) Note 2
- 19 P13/TxD2/SO20/TRDIOA1/IVCMP1 Note 1
- 18 P14/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)
- 17 P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
- 16 P16/TI01/TO01/INTP5/TRDIOC0/IVREF0 Note 1/(RXD0)
- 15 P17/TI02/TO02/TRDIOA0/TRDCLK/IVCMP0 Note 1/(TXD0)
- 14 P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB
- 13 P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)

Bottom pins (1 to 12):
- 1 P60/SCLA0
- 2 P61/SDAA0
- 3 P62/SSI00
- 4 P63
- 5 P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)
- 6 P75/KR5/INTP9/SCK01/SCL01
- 7 P74/KR4/INTP8/SI01/SDA01
- 8 P73/KR3/SO01
- 9 P72/KR2/SO21
- 10 P71/KR1/SI21/SDA21
- 11 P70/KR0/SCK21/SCL21
- 12 P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0

Note 1. Mounted on the 96 KB or more code flash memory products.
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).
Remark 3. It is recommended to connect an exposed die pad to Vss.

1.5   Block Diagram

1.5.1   30-pin products
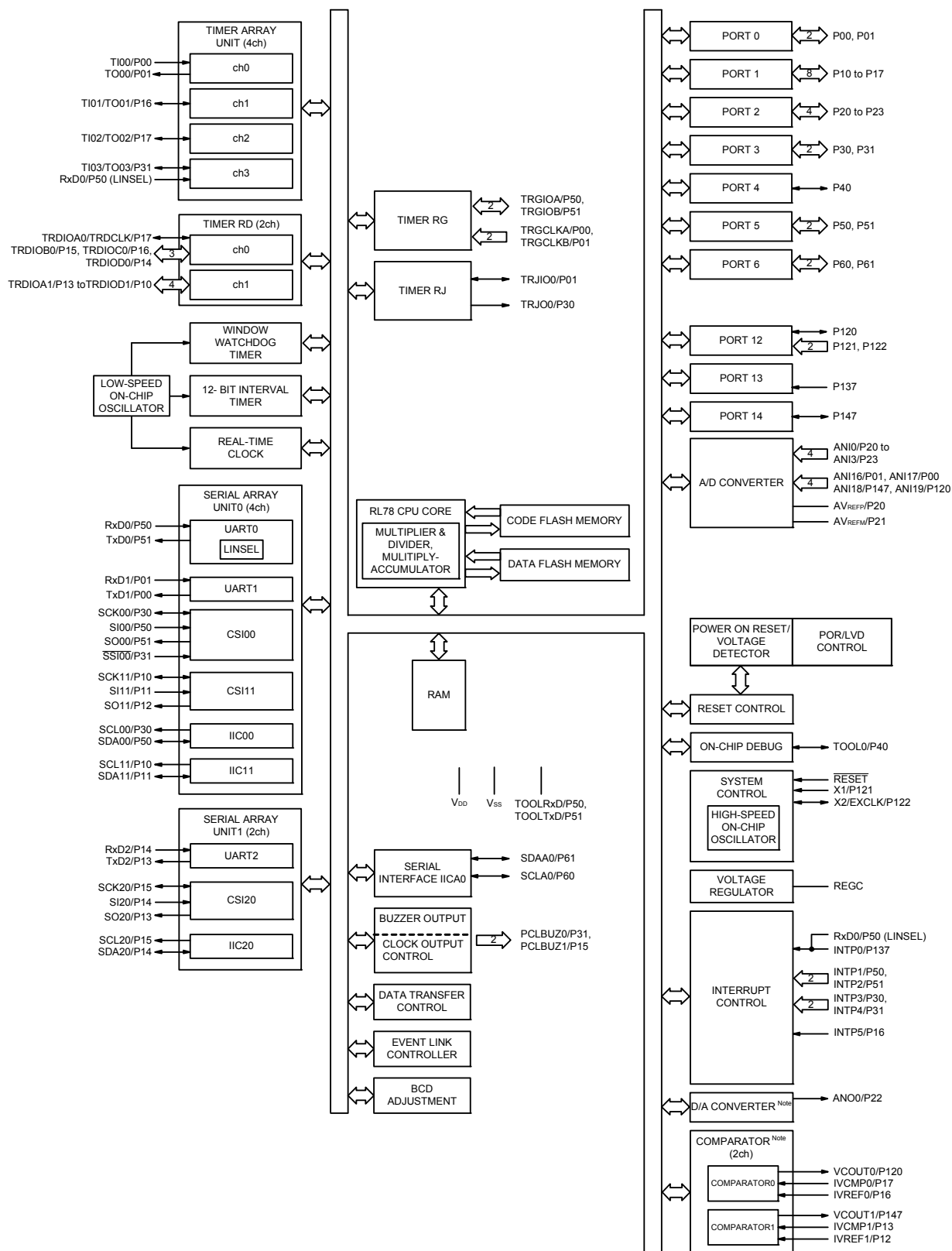
Note   Mounted on the 96 KB or more code flash memory products.
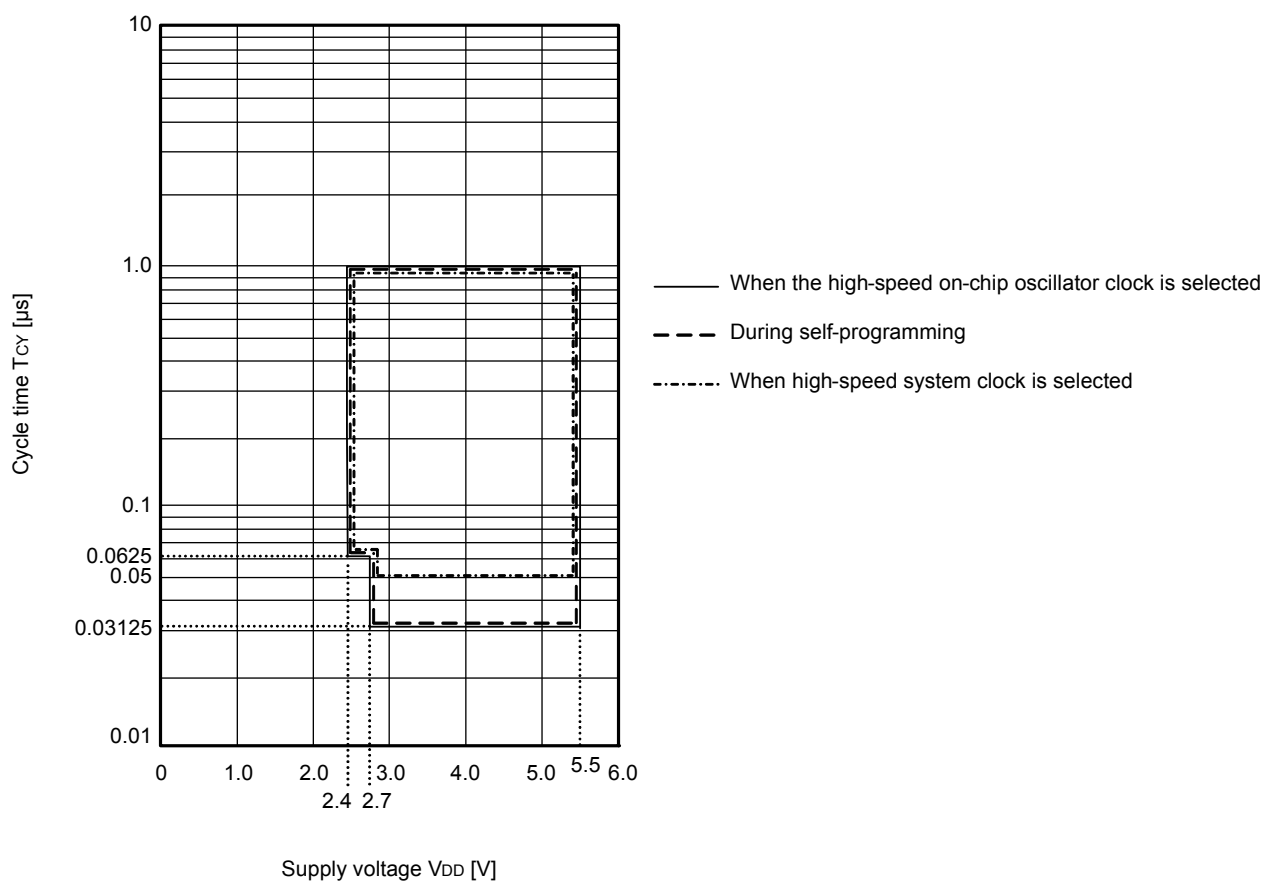
Absolute Maximum Ratings (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			-65 to +150	°C

Caution　**Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark　Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

                             2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

When the high-speed on-chip oscillator clock is selected

During self-programming

When high-speed system clock is selected

Supply voltage V$_{DD}$ [V]

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T$_A$ = -40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)   **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

    * This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ EV$_{DD0}$ < 4.0 V and 2.3 V ≤ V$_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

    * This value is the theoretical value of the relative difference between the transmission and reception sides

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200		1150		1150		ns
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t_{KCY1}/2 - 120		t_{KCY1}/2 - 120		t_{KCY1}/2 - 120		ns
SCKp low-level width	t_{KL1}	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t_{KCY1}/2 - 7		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		479		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 1]	t_{KSO1}	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60		60	ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130		130	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)
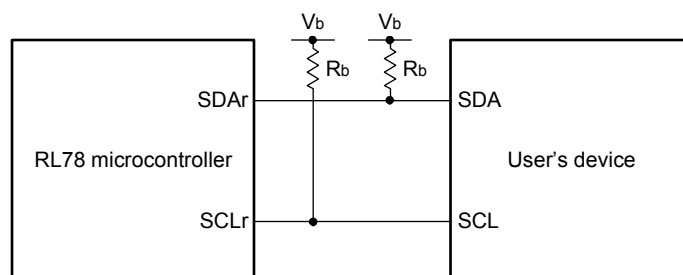
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output [Note 1]	t_{KSO1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use it with EV_{DD0} $\geq$ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

Simplified I²C mode connection diagram (during communication at different potential)

Simplified I²C mode serial transfer timing (during communication at different potential)
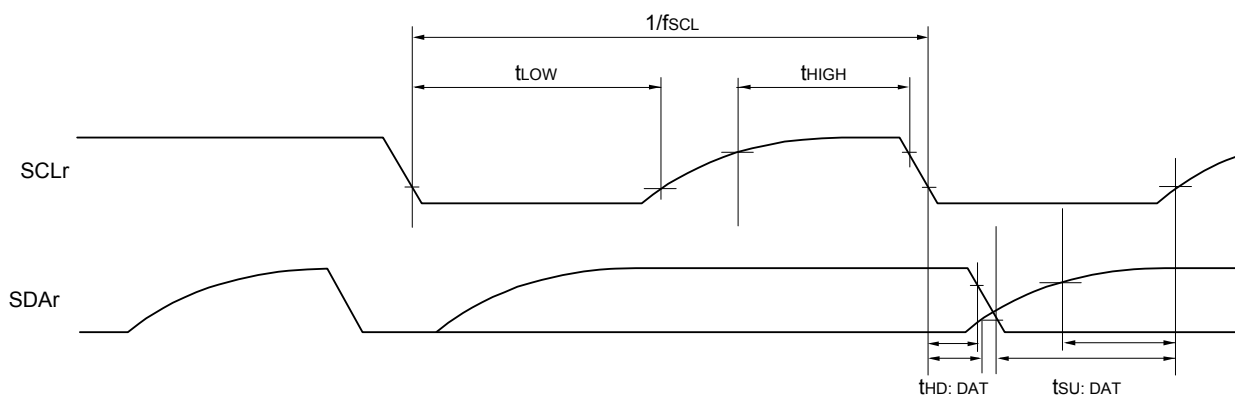
Remark 1. R$_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

(3) I^{2}C fast mode plus

(T$_A$ = -40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode plus: f$_{CLK}$ ≥ 10 MHz	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	1000	—		—		kHz
Setup time of restart condition	t$_{SU: STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Hold time Note 1	t$_{HD: STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Data setup time (reception)	t$_{SU: DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		50		—		—		ns
Data hold time (transmission) Note 2	t$_{HD: DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	0.45	—		—		μs
Setup time of stop condition	t$_{SU: STO}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Bus-free time	t$_{BUF}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of t$_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Note 3. The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C$_b$ = 120 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
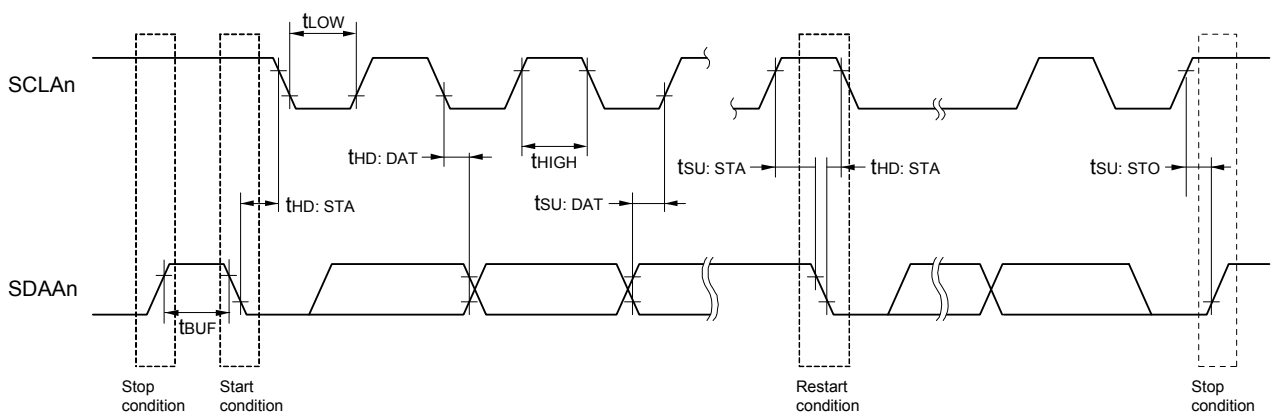
Remark n = 0, 1

**(4)   When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-)
= AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20**

**(T$_A$ = -40 to +85°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 1.6 V $\leq$ EV$_{DD}$ = EV$_{DD1}$ $\leq$ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage
(+) = V$_{BGR}$ [Note 3], Reference voltage (-) = AV$_{REFM}$ = 0 V [Note 4], HS (high-speed main) mode)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±0.60	% FSR
Integral linearity error [Note 1]	ILE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3.   Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.
Note 4.   When reference voltage (-) = V$_{SS}$, the MAX. values are as follows.
 Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV$_{REFM}$.
 Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.
 Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.

(2)   During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	250		ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V	500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 - 24		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 - 36		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 - 76		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		66		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		66		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI1}$			38		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO1}$	C = 30 pF [Note 4]			50	ns

Note 1.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4.   C is the load capacitance of the SCKp and SOp output lines.

Caution   **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

Note 5. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ EV$_{DD0}$ < 3.3 V and 1.6 V ≤ V$_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met.

Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 30- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)　　　　　　**(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 2		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 2		ns
		4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 Note 2		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note 2		ns
		2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Note 1.　The value must also be equal to or less than f_{MCK}/4.

Note 2.　Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution　**Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-)= AV_{REFM}
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI20	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP},
Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output volt- age (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Full-scale error [Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14		0		AV_{REFP}	V
		Internal reference voltage output (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{BGR} [Note 4]		V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{TMPS25} [Note 4]		V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
  Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
  Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
  Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Note 4. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(4)   When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 1.6 V $\leq$ EV$_{DD}$ = EV$_{DD1}$ $\leq$ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V,
Reference voltage (+) = V$_{BGR}$ Note 3, Reference voltage (-) = AV$_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E$_{ZS}$	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ Note 3	V

Note 1.   Excludes quantization error (±1/2 LSB).
Note 2.   This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3.   Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.
Note 4.   When reference voltage (-) = V$_{SS}$, the MAX. values are as follows.
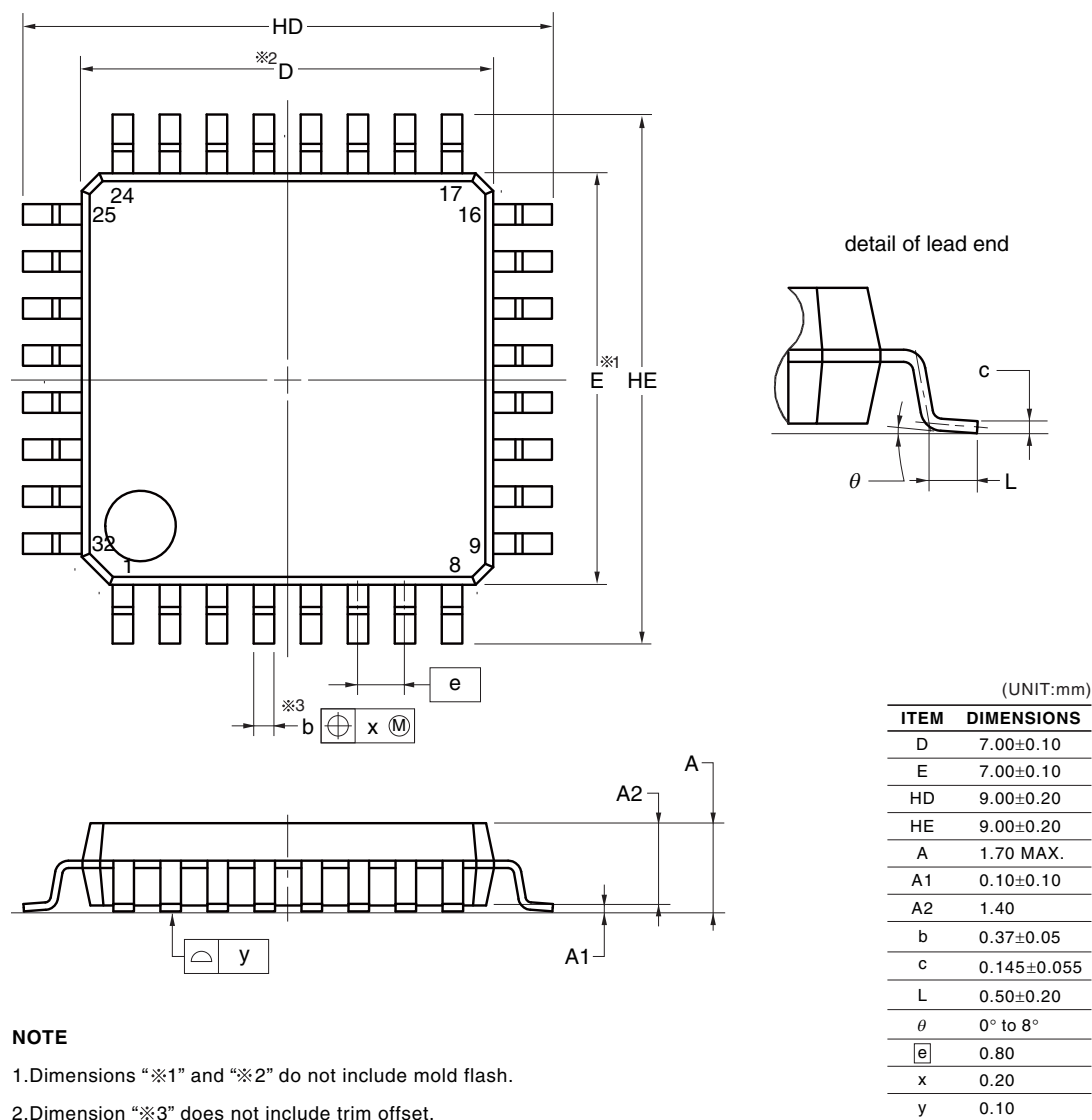   Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV$_{REFM}$.
   Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.
   Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV$_{REFM}$.

R5F104BAAFP, R5F104BCAFP, R5F104BDAFP, R5F104BEAFP, R5F104BFAFP, R5F104BGAFP
R5F104BADFP, R5F104BCDFP, R5F104BDDFP, R5F104BEDFP, R5F104BFDFP, R5F104BGDFP
R5F104BAGFP, R5F104BCGFP, R5F104BDGFP, R5F104BEGFP, R5F104BFGFP, R5F104BGGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2

detail of lead end

	(UNIT:mm)
ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

4.6   48-pin products

R5F104GAAFB, R5F104GCAFB, R5F104GDAFB, R5F104GEAFB, R5F104GFAFB, R5F104GGAFB,
R5F104GHAFB, R5F104GJAFB
R5F104GADFB, R5F104GCDFB, R5F104GDDFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB,
R5F104GHDFB, R5F104GJDFB
R5F104GAGFB, R5F104GCGFB, R5F104GDGFB, R5F104GEGFB, R5F104GFGFB, R5F104GGGFB,
R5F104GHGFB, R5F104GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 {}^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° {}^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.
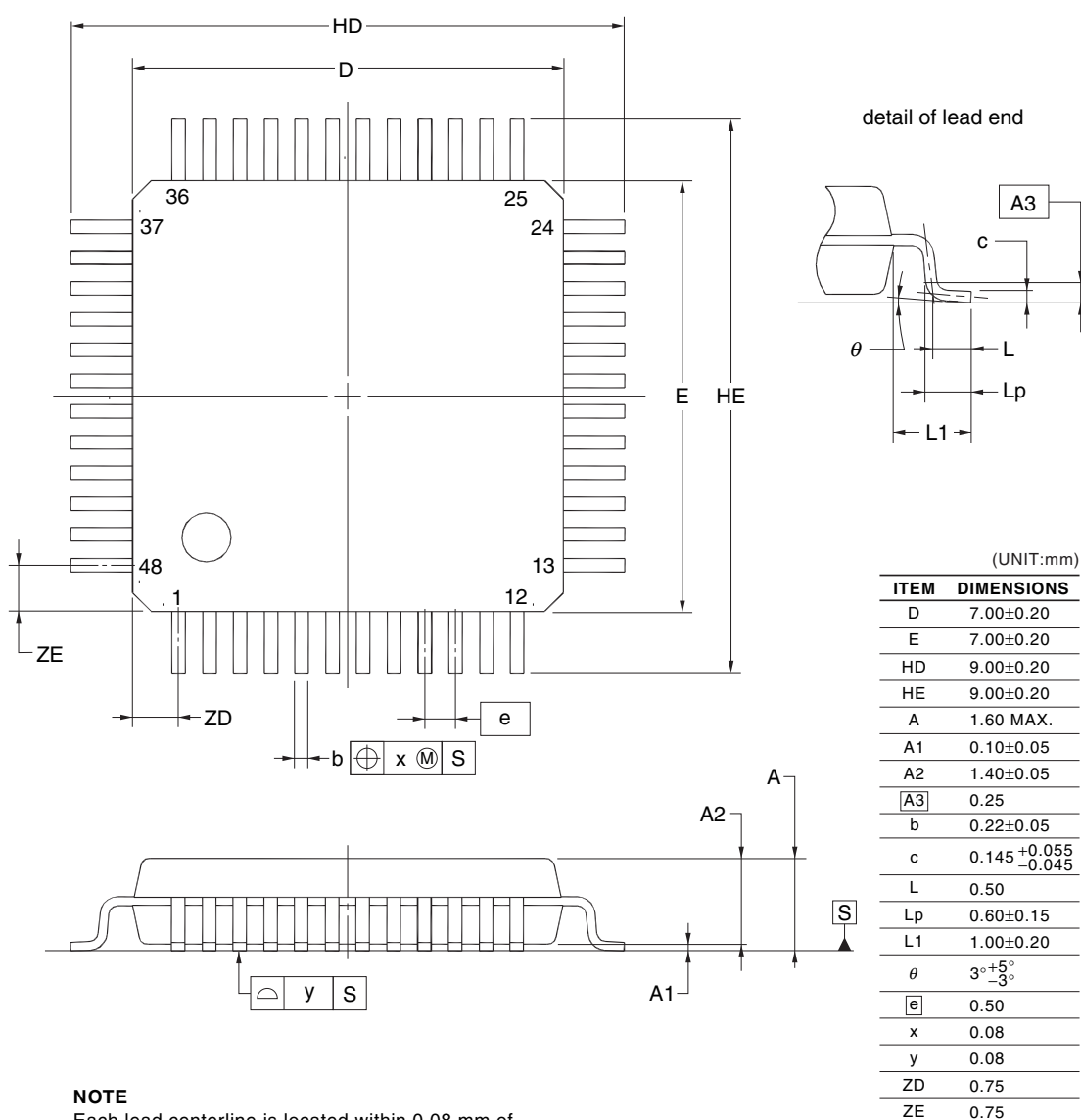
R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA
R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
R5F104MKAFA, R5F104MLAFA
R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69
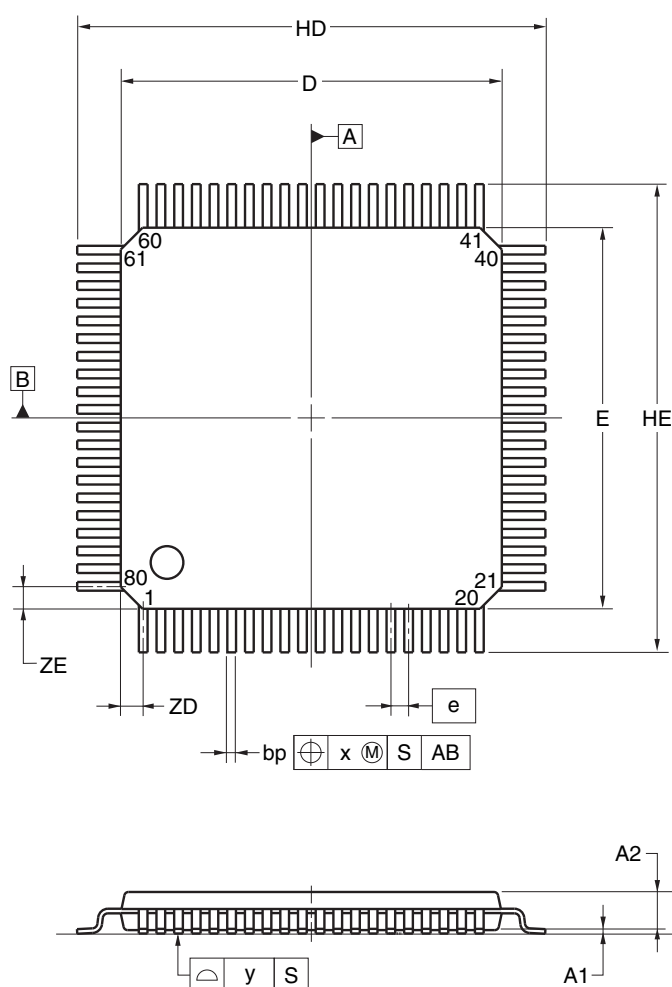
detail of lead end
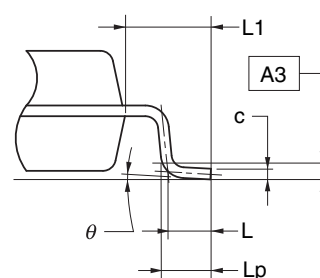
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	——	——	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	——	0.25	——
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	——	0.80	——
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
θ	0°	3°	8°
e	——	0.65	——
x	——	——	0.13
y	——	——	0.10
ZD	——	0.825	——
ZE	——	0.825	——