Renesas Electronics America Inc - R5F104LGAXXXFB#V0 Datasheet

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What is "Embedded - Microcontrollers"?

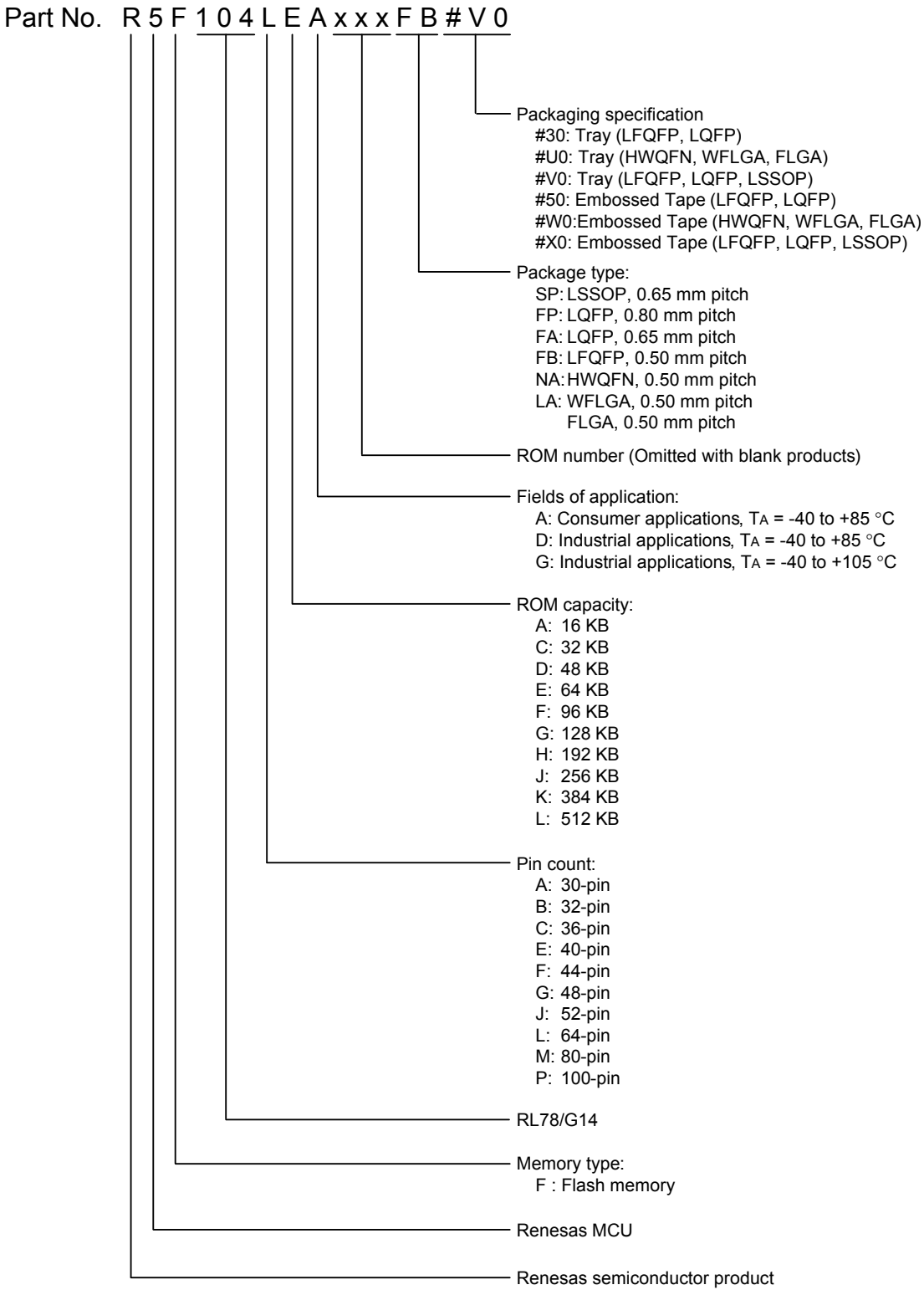
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104lgaxxxfb-v0

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14



(1/5)

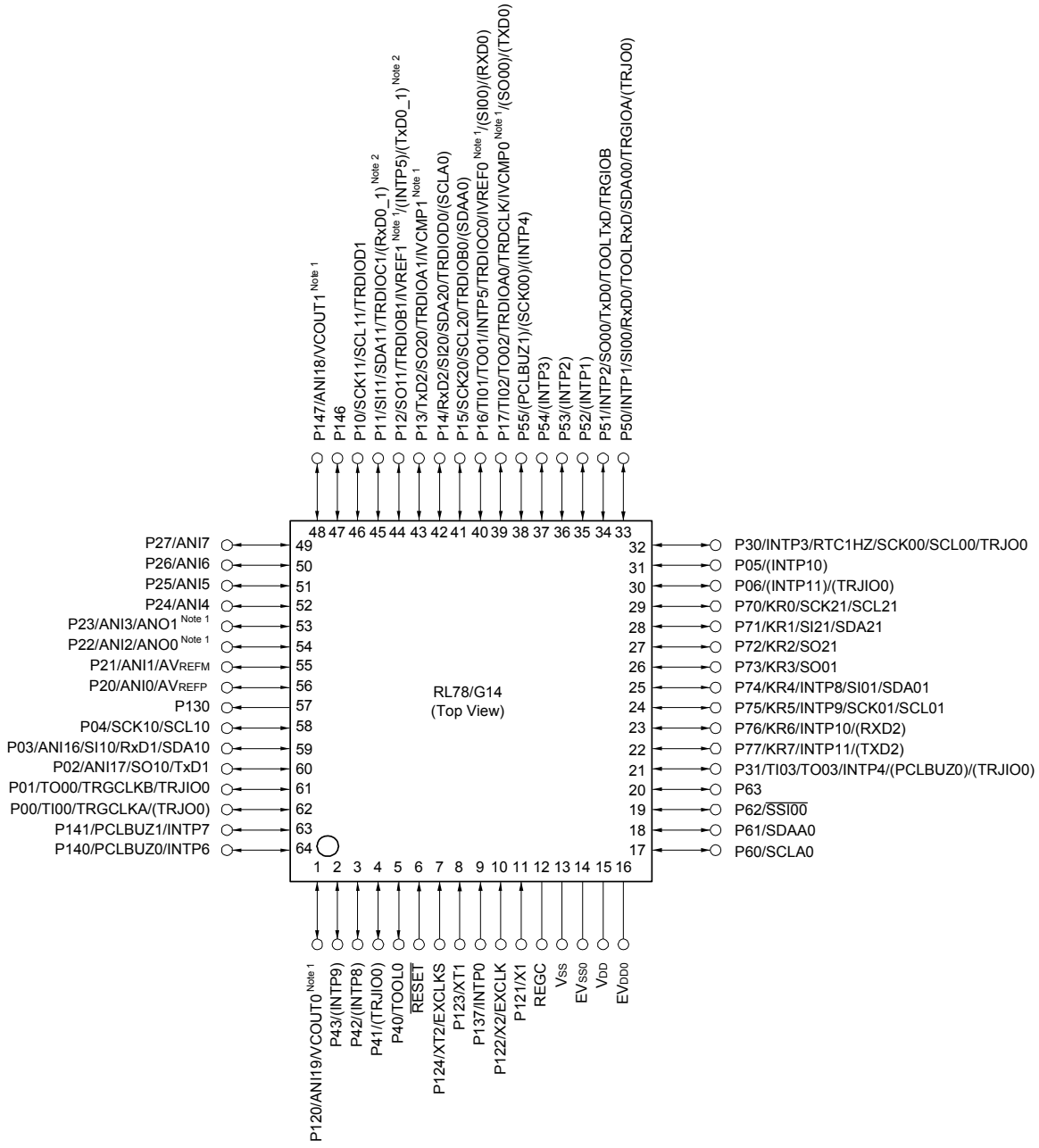
Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0 R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0 R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0 R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0 R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0 R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0 R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0 R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BFDFP#V0, R5F104BGDFP#V0 R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BFDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0 R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0 R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0 R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

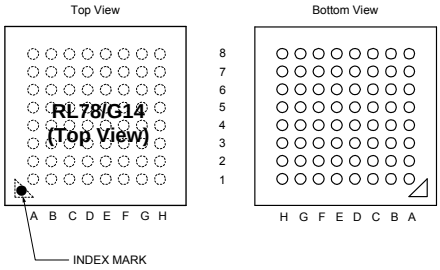
Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)



	A	B	C	D	E	F	G	H	
8	EV_{DD0}	EV_{SS0}	P121/X1	P122/X2/ EXCLK	P137/INTP0	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ $VCOUT0$ Note 1	8
7	P60/SCLA0	V_{DD}	V_{SS}	REGC	$\overline{RESET}$	P01/TO00/ TRGCLKB/ TRJIO0	P00/TI00/ TRGCLKA/ (TRJO0)	P140/ PCLBUZ0/ INTP6	7
6	P61/SDAA0	P62/$\overline{SSI00}$	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/ SO10/TxD1	P141/ PCLBUZ1/ INTP7	6
5	P77/KR7/ INTP11/(TXD2)	P31/TI03/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AV_{REFP}	5
4	P75/KR5/ INTP9/ SCK01/ SCL01	P76/KR6/ INTP10/ (RXD2)	P52/(INTP1)	P54/(INTP3)	P16/TI01/ TO01/INTP5/ TRDIOC0/ IVREF0 Note 1/ (SI00)/(RXD0)	P21/ANI1/ AV_{REFM}	P22/ANI2/ ANO0 Note 1	P23/ANI3/ ANO1 Note 1	4
3	P70/KR0/ SCK21/ SCL21	P73/KR3/ SO01	P74/KR4/ INTP8/SI01/ SDA01	P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note 1/ (SO00)/(TXD0)	P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0)	P12/SO11/ TRDIOB1/ IVREF1 Note 1/ (INTP5)/ (TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJO0	P72/KR2/ SO21	P71/KR1/ SI21/SDA21	P06/(INTP11)/ (TRJIO0)	P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)	P11/SI11/ SDA11/ TRDIOC1/ (RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJO0)	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P55/ (PCLBUZ1)/ (SCK00)/ (INTP4)	P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 Note 1	P10/SCK11/ SCL11/ TRDIOD1	P146	P147/ANI18/ $VCOUT1$ Note 1	1
	A	B	C	D	E	F	G	H	

Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as VSS pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

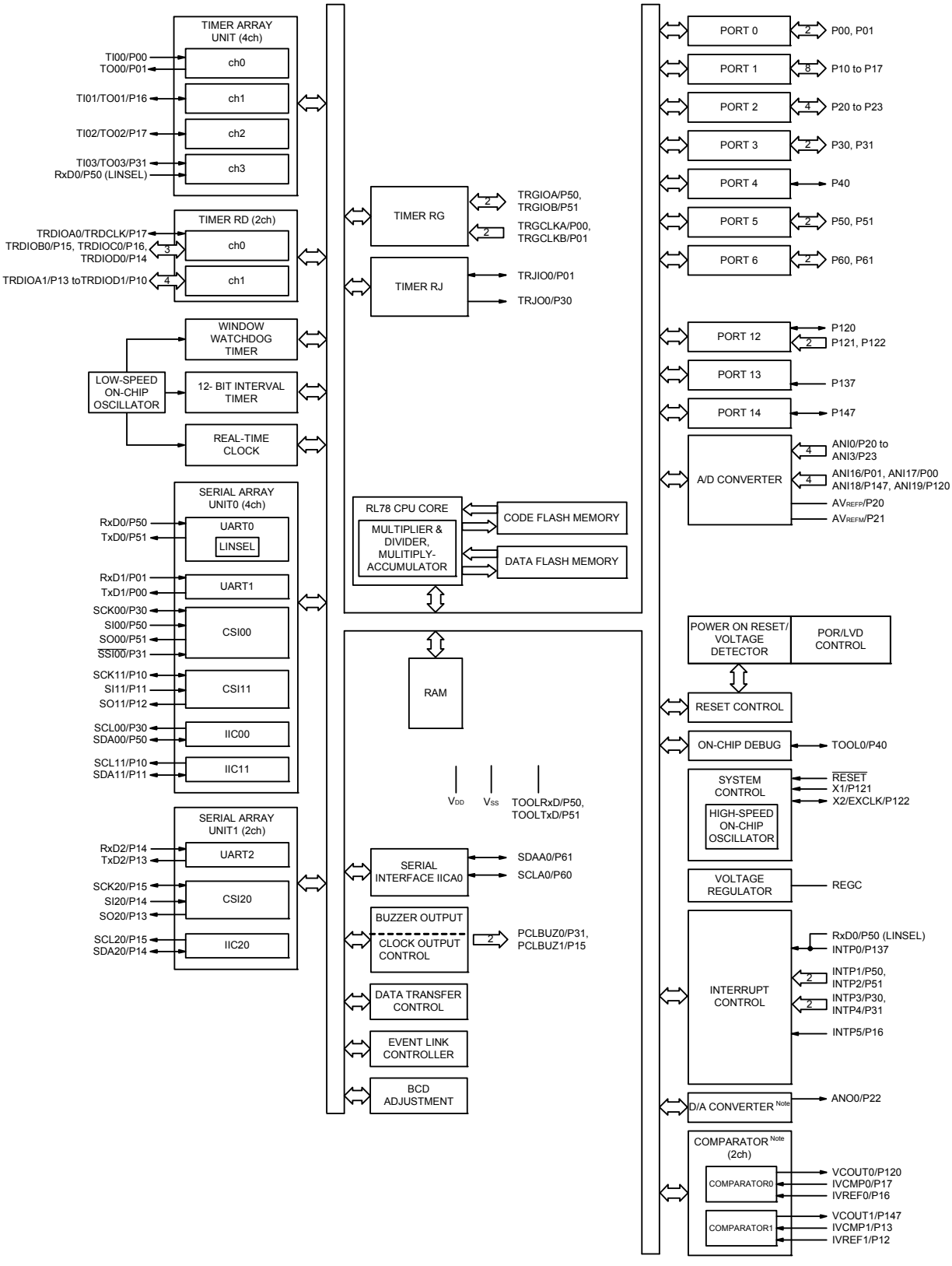
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

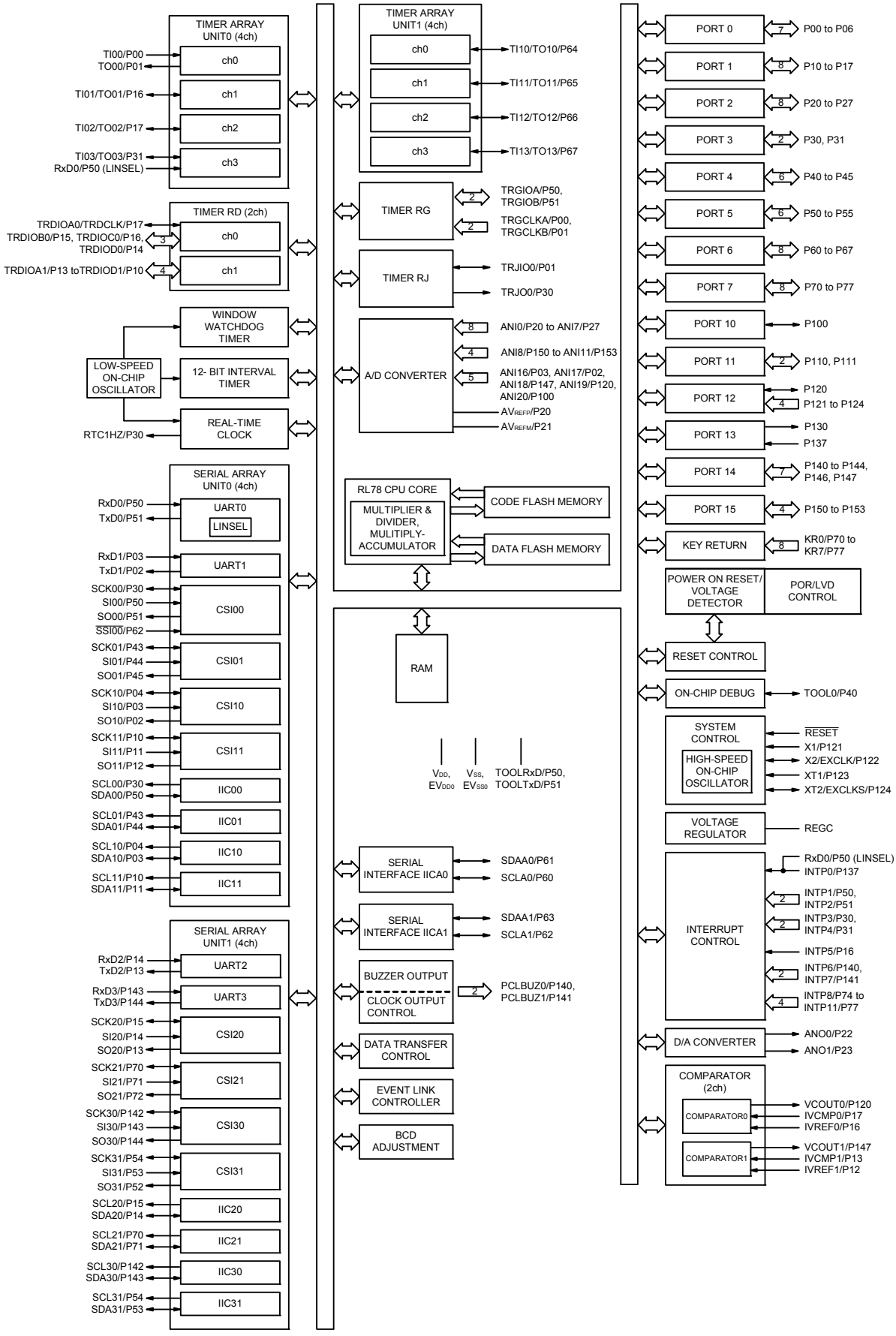
1.5 Block Diagram

1.5.1 30-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.5.9 80-pin products



(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(4/5)**

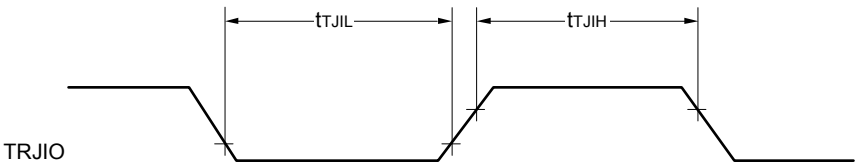
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

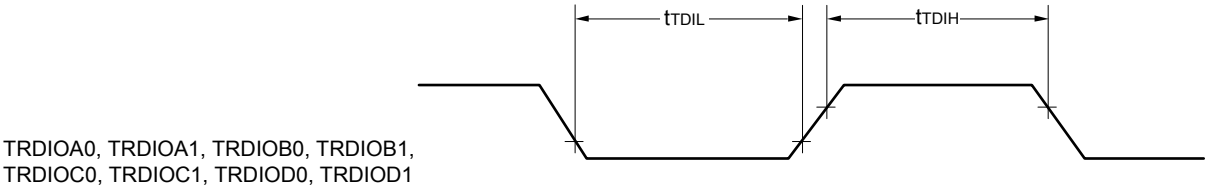
Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

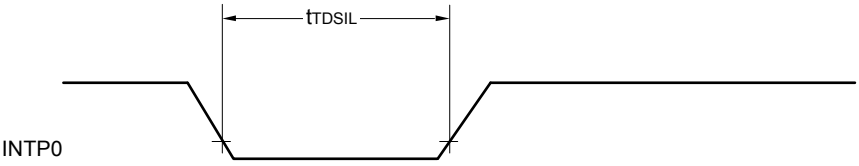
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

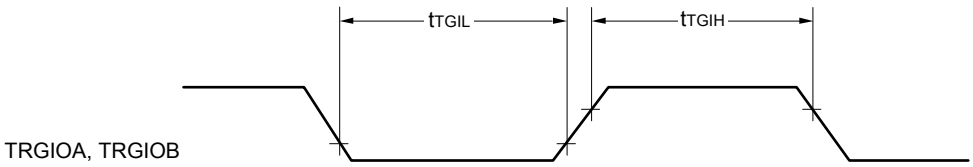
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/f_{CLK}			ns
Timer RD forced cutoff signal input low-level width	t_{TDSIL}	P130/INTP0	2MHz < f_{CLK} ≤ 32 MHz	1			µs
			f_{CLK} ≤ 2 MHz	1/f_{CLK} + 1			
Timer RG input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB		2.5/f_{CLK}			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EV_{DD0} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.6 V ≤ V_{DD} ≤ 5.5 V	1			µs
		INTP1 to INTP11	1.6 V ≤ EV_{DD0} ≤ 5.5 V	1			µs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	1.8 V ≤ EV_{DD0} ≤ 5.5 V	250			ns
			1.6 V ≤ EV_{DD0} < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs


tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1


tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 7		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4			10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $EV_{DD0} \geq V_b$.

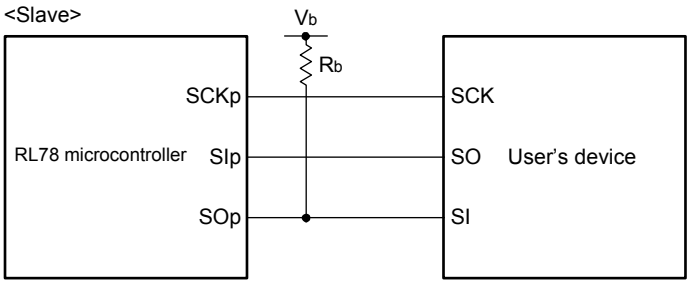
Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		V_{LVD12}	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		V_{LVD13}	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.4		mA
						V_{DD} = 3.0 V		2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		
						V_{DD} = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.1	9.3	mA
						V_{DD} = 3.0 V		5.1	9.3	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	8.7	
						V_{DD} = 3.0 V		4.8	8.7	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	7.3	
						V_{DD} = 3.0 V		4.0	7.3	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.8	6.7	
						V_{DD} = 3.0 V		3.8	6.7	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.9	
						V_{DD} = 3.0 V		2.8	4.9	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.7	mA
						Resonator connection		3.4	5.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.7	
						Resonator connection		3.4	5.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.4	
						Resonator connection		2.1	3.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.4	
						Resonator connection		2.1	3.5	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.7	6.1	µA
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.7	6.1	
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.8	6.7	
						Resonator connection		4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.8	7.5	
						Resonator connection		4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.4	8.9	
						Resonator connection		5.4	8.9	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		7.2	21.0	
						Resonator connection		7.3	21.1	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

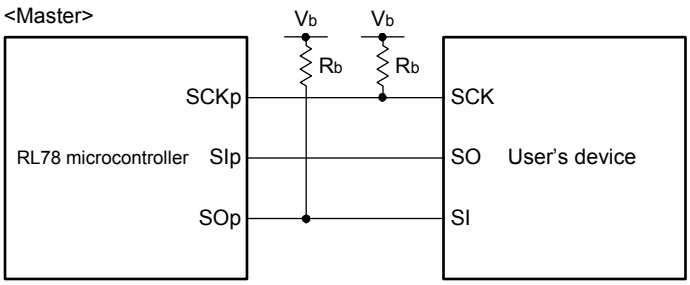
Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

CSI mode connection diagram (during communication at different potential



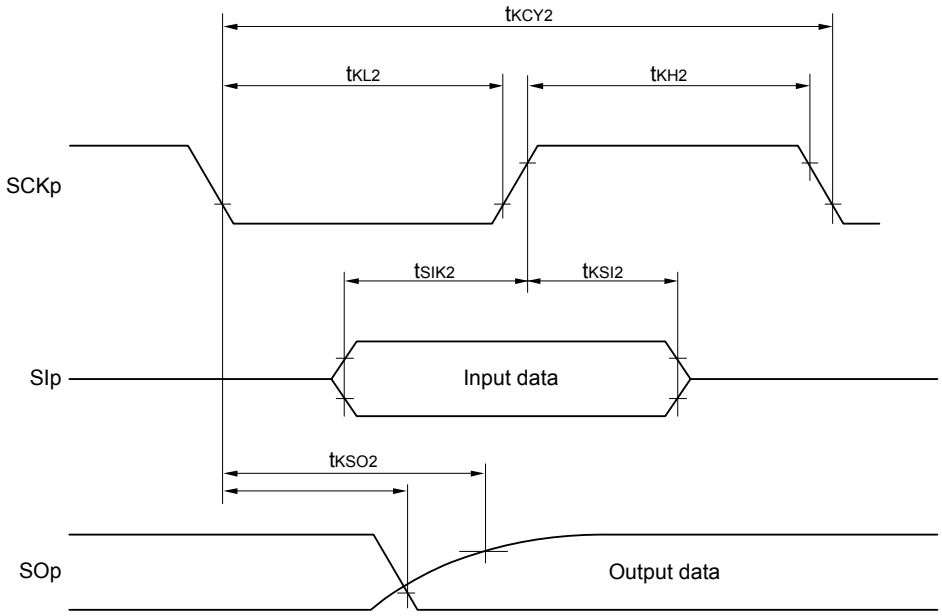
Remark 5. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 6. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

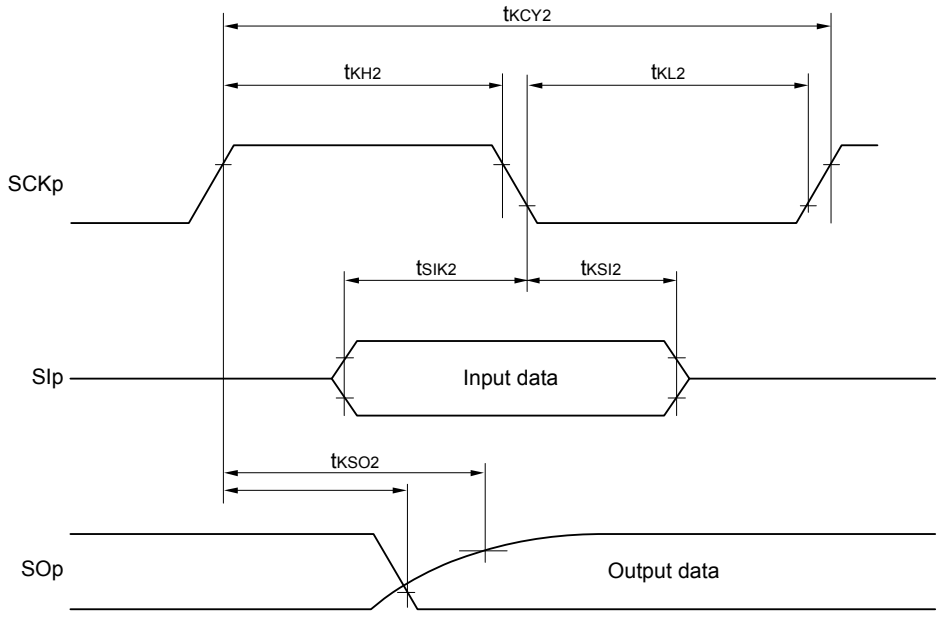
Remark 7. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 8. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



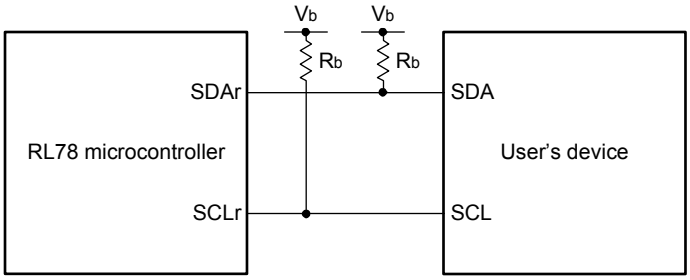
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



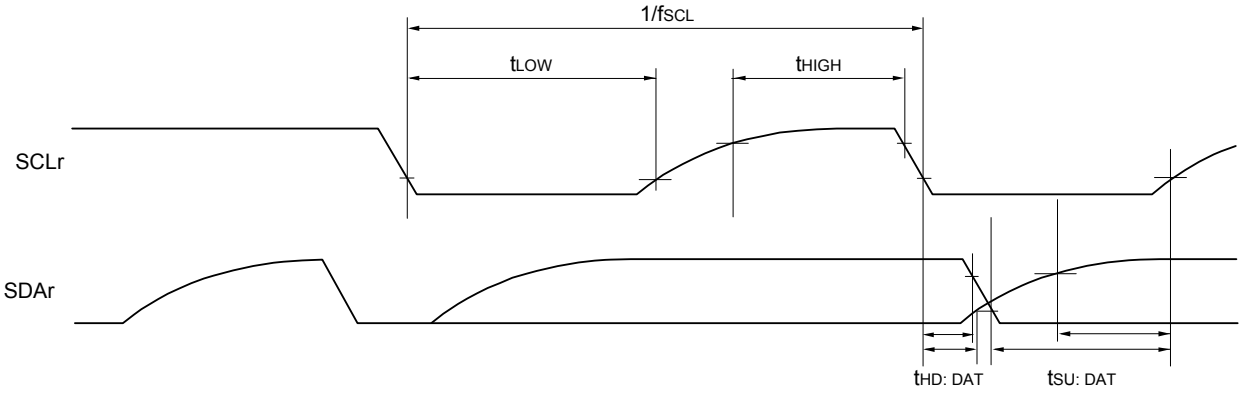
Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		µs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

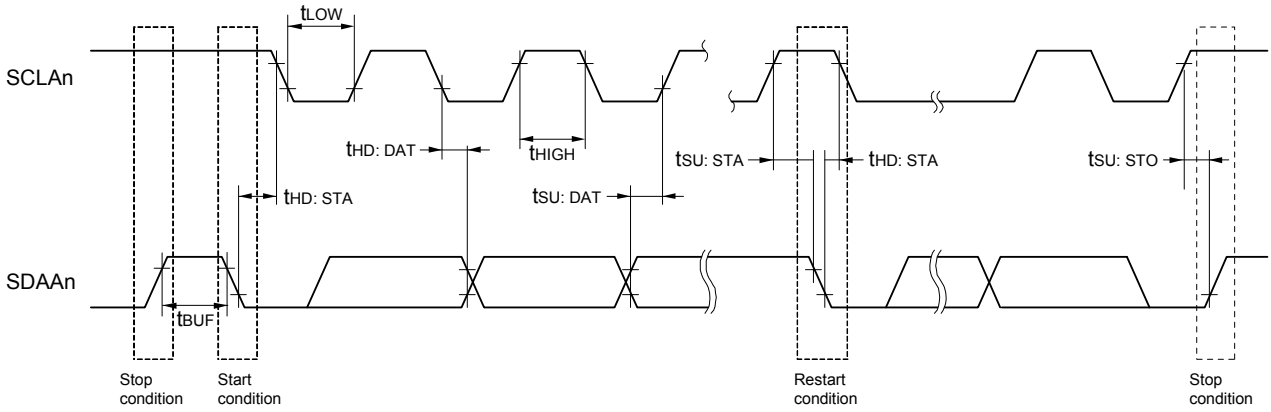
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

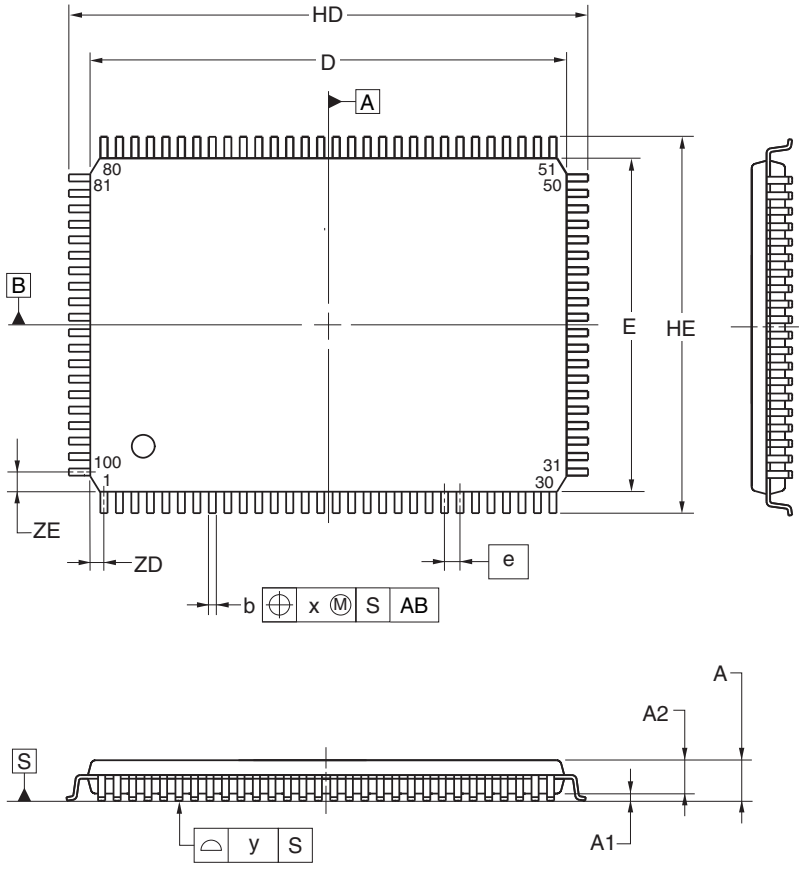
IICA serial transfer timing



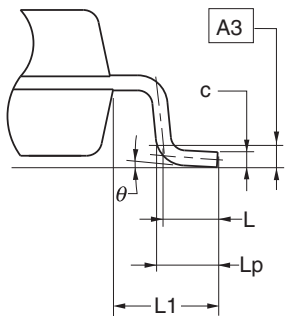
Remark n = 0, 1

R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJAFA
R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFA
R5F104PFGFA, R5F104PGGFA, R5F104PHGFA, R5F104PJGFA
R5F104PKAFA, R5F104PLAFA
R5F104PKGFA, R5F104PLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825