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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104lggxxxfb-v0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.5.3 36-pin products



Note Mounted on the 96 KB or more code flash memory products.



1.5.6 48-pin products



Note Mounted on the 96 KB or more code flash memory products.



1.5.7 52-pin products



Note Mounted on the 96 KB or more code flash memory products.



Note	The flash library uses RAM in self-programming and rewriting of the data flash memory.
	The target products and start address of the RAM areas used by the flash library are shown below.
	R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
	For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family
	(R20UT2944).



2.1 **Absolute Maximum Ratings**

Absolute Maximum Ratings

Absolute Maximum R	atings			(1/2)
Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	Vdd		-0.5 to +6.5	V
	EVDD0, EVDD1	EVDD0 = EVDD1	-0.5 to +6.5	V
	EVsso, EVss1	EVsso = EVss1	-0.5 to +0.3	V
REGC pin input voltage	VIREGC	REGC	-0.3 to +2.8 and -0.3 to VDD +0.3 ^{Note 1}	V
Input voltage	VI1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EVDD0 +0.3 and -0.3 to VDD +0.3 Note 2	V
	Vı2	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	Vı3	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to VDD +0.3 Note 2	V
Output voltage	Vo1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EVDD0 +0.3 and -0.3 to VDD +0.3 Note 2	V
	Vo2	P20 to P27, P150 to P156	-0.3 to VDD +0.3 Note 2	V
Analog input voltage	Vai1	ANI16 to ANI20	-0.3 to EVDD0 +0.3 and -0.3 to AVREF(+) +0.3 Notes 2, 3	V
Output voltage Analog input voltage	VAI2	ANI0 to ANI14	-0.3 to VDD +0.3 and -0.3 to AVREF(+) +0.3 ^{Notes 2, 3}	v

Note 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.

- Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
- Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AVREF (+): + side reference voltage of the A/D converter.

Remark 3. Vss: Reference voltage



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))



RL78/G14

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

Parameter	Symbol	Conditions		Conditions HS (high-speed main) mode		LS (low-speed mode	d main)	LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tксү1	tксү1 ≥ 2/fc∟к	$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 20 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$	200		1150		1150		ns
			$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_{b} \leq 2.7 \; V, \\ C_{b} = 20 \; pF, \; R_{b} = 2.7 \; k\Omega \end{array}$	300		1150		1150		ns
SCKp high-level width	tкнı			tkcy1/2 - 50		tkcy1/2 - 50		tkcy1/2 - 50		ns
				tксү1/2 - 120		tксү1/2 - 120		tксү1/2 - 120		ns
SCKp low-level width	tĸ∟ı			tксү1/2 - 7		tксү1/2 - 50		tkcy1/2 - 50		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 20 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		tксү1/2 - 10		tkcy1/2 - 50		tkcy1/2 - 50		ns
SIp setup time (to SCKp↑) ^{Note 1}	tsiк1	$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 20 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$		58		479		479		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq \\ C_{b} \texttt{=} 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) ^{Note 1}	tĸsı1	$\begin{array}{l} 4.0 \ V \leq EV_{DDO} \\ 2.7 \ V \leq V_{b} \leq V_{b} \\ C_{b} \texttt{=} 20 \ pF, \ R_{b} \end{array}$	0 ≤ 5.5 V, 4.0 V, = 1.4 kΩ	10		10		10		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq 1 \\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp out- put ^{Note 1}	tkso1	$\begin{array}{l} 4.0 \ V \leq EV_{DD}\\ 2.7 \ V \leq V_{b} \leq V\\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	0 ≤ 5.5 V, 4.0 V, = 1.4 kΩ		60		60		60	ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} \\ 2.3 \ V \leq V_{b} \leq \\ C_{b} = 20 \ pF, \ R_{b} \end{array}$	< 4.0 V, 2.7 V, = 2.7 kΩ		130		130		130	ns

(TA = -40 to +85°C, 2.7 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(Notes, Caution, and Remarks are listed on the next page.)



RL78/G14

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

Parameter	Symbol	Cor	Conditions		Conditions		HS (high-speed main) mode		r-speed mode	LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
SCKp cycle time	tксү2	$4.0~V \leq EV_{DD0} \leq 5.5~V,$	24 MHz < fмск	14/fмск		_		_		ns		
Note 1		$2.7~V \leq V_b \leq 4.0~V$	$20 \text{ MHz} < f_{MCK} \leq 24 \text{ MHz}$	12/fмск		—				ns		
		$8 \text{ MHz} < \text{fmck} \le 20 \text{ MHz}$	10/fмск		_				ns			
			$4 \text{ MHz} < f_{MCK} \le 8 \text{ MHz}$	8/fмск		16/fмск		_		ns		
		fмск ≤ 4 MHz	6/fмск		10/fмск		10/fмск		ns			
		$2.7~V \leq EV_{DD0} < 4.0~V,$	24 MHz < fмск	20/fмск		—		_		ns		
		$2.3 \text{ V} \leq \text{V}_b \leq 2.7 \text{ V}$	20 MHz < fмск ≤ 24 MHz	16/fмск		—		_		ns		
			16 MHz < fмск ≤ 20 MHz	14/fмск		—		_		ns		
			$8 \text{ MHz} < \text{fmck} \le 16 \text{ MHz}$	12/fмск		_		_		ns		
			$4 \text{ MHz} < \text{fmck} \le 8 \text{ MHz}$	8/fмск		16/fмск		_		ns		
			fмск ≤ 4 MHz	6/fмск		10/fмск		10/fмск		ns		
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V \\ Note \ 2 \end{array}$	24 MHz < fмск	48/fмск		_		_		ns		
1.6 $V \le V_b \le 2$ Note 2			20 MHz < fмск ≤ 24 MHz	36/fмск		_		_		ns		
			16 MHz < fmck \leq 20 MHz	32/fмск		—		_		ns		
			$8 \text{ MHz} < \text{fmck} \le 16 \text{ MHz}$	26/fмск		_		_		ns		
			$4 \text{ MHz} < \text{fmck} \le 8 \text{ MHz}$	16/fмск		16/fмск		_		ns		
		fмск ≤ 4 MHz	10/fмск		10/fмск		10/fмск		ns			
SCKp high-/ low-level width	tкн2, tкL2	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}, 2$	tксү2/2 - 12		tксү2/2 - 50		tксү2/2 - 50		ns			
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}, 2$	$2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}$	tксү2/2 - 18		tксү2/2 - 50		tксү2/2 - 50		ns		
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 3.3 \text{ V}, ^{2}$	$1.6 \text{ V} \leq V_b \leq 2.0 \text{ V} \text{ Note } 2$	tксү2/2 - 50		tксү2/2 - 50		tксү2/2 - 50		ns		
SIp setup time (to SCKp↑) ^{Note 3}	tsık2	$4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}, 2$	$2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns		
		$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}, 2$	$2.7 \text{ V} \le EV_{DD0} < 4.0 \text{ V}, 2.3 \text{ V} \le V_b \le 2.7 \text{ V}$			1/fмск + 30		1/fмск + 30		ns		
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 3.3 \text{ V}, $	$1.6 \text{ V} \leq V_b \leq 2.0 \text{ V} \text{ Note 2}$	1/fмск + 30		1/fмск + 30		1/fмск + 30		ns		
SIp hold time (from SCKp↑) Note 4	tksi2			1/fмск + 31		1/fмск + 31		1/fмск + 31		ns		
Delay time from SCKp↓ to SOp	tkso2	4.0 V \leq EVDD0 \leq 5.5 V, 2 Cb = 30 pF, Rb = 1.4 kΩ	$2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V},$		2/fмск + 120		2/fмск + 573		2/fмск + 573	ns		
output ^{Note 5}		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, 2 \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	$2.3 \text{ V} \le \text{V}_{\text{b}} \le 2.7 \text{ V},$		2/fмск + 214		2/fмск + 573		2/fмск + 573	ns		
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ C_b = 30 \ pF, \ R_V = 5.5 \ k\Omega \end{array}$	$1.6 \text{ V} \le \text{V}_b \le 2.0 \text{ V} \text{ Note 2},$		2/fмск + 573		2/fмск + 573		2/fмск + 573	ns		

($(T_A = -40 \text{ to } +85^{\circ}\text{C})$	18V<	< Vnn < 5 5 V	Vss = EVsso	= FVSS1 = 0	٧١
	1 = -40 10 + 00 0	1.0 V -		, v 33 – L v 330		• /

(Notes, Caution, and Remarks are listed on the next page.)



Parameter	Symbol	Conditions	HS (high-speed r mode	nain)	LS (low-speed m mode	nain)	LV (low-voltage r mode	nain)	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu:dat	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	1/fмск + 135 Note 3		1/fмск + 190 Note 3		1/fмск + 190 Note 3		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	1/fмск + 135 Note 3		1/fмск + 190 Note 3		1/fмск + 190 Note 3		ns
			1/fмск + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ p\text{F}, \ R_b = 2.7 \ k\Omega \end{array}$	1/fмск + 190 Note 3		1/fmck + 190 Note 3		1/fмск + 190 Note 3		ns
			1/fмск + 190 Note 3		1/fмск + 190 Note 3		1/fмск + 190 Note 3		ns
Data hold time (transmission)	thd:dat	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	0	305	0	305	0	305	ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	0	305	0	305	0	305	ns
		$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 100 \ p\text{F}, \ R_b = 2.8 \ k\Omega \end{array}$	0	355	0	355	0	355	ns
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	0	355	0	355	0	355	ns
			0	405	0	405	0	405	ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(TA = -40 to +85°C, 1.8 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

(2/2)

Note 1. The value must also be equal to or less than fmck/4.

Note 2. Use it with $EV_{DD0} \ge V_b$.

Note 3. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)



2.5.2 Serial interface IICA

(1) I²C standard mode

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(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)
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Parameter	Symbol	Conditions		Conditions HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	l
SCLA0 clock	fscL	Standard mode:	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V$	0	100	0	100	0	100	kHz
frequency		fc∟k ≥ 1 MHz	$1.8 \text{ V} \leq EV_{\text{DD0}} \leq 5.5 \text{ V}$	0	100	0	100	0	100	kHz
			$1.7~V \leq EV_{DD0} \leq 5.5~V$	0	100	0	100	0	100	kHz
		$1.6~V \le EV_{DD0} \le 5.5~V$	-	_	0	100	0	100	kHz	
Setup time of tsu: sta $2.7 \text{ V} \le \text{EV}$ DDO		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3$	5.5 V	4.7		4.7		4.7		μs
restart condition		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		4.7		4.7		4.7		μs
		$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		4.7		4.7		4.7		μs
1.6		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	-	_	4.7		4.7		μs
Hold time Note 1 thd: STA		$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	4.0		4.0		4.0		μs	
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			4.0		4.0		μs
		$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	4.0		4.0		4.0		μs	
		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		—		4.0		4.0		μs
Hold time when	tLOW	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	4.7		4.7		4.7		μs
SCLA0 = "L"		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	4.7		4.7		4.7		μs
		$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	4.7		4.7		4.7		μs
		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	-	_	4.7		4.7		μs
Hold time when	tніgн	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	4.0		4.0		4.0		μs
SCLA0 = "H"		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	4.0		4.0		4.0		μs
		$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 3$	5.5 V	4.0		4.0		4.0		μs
		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 8$	5.5 V	-	_	4.0		4.0		μs

 $(\ensuremath{\textit{Notes}}, \ensuremath{\textit{Caution}}, \ensuremath{\text{and}} \ensuremath{\textit{Remark}}$ are listed on the next page.)



2.7 **RAM Data Retention Characteristics**

(TA = -40 to +85°C, Vss = 0V)										
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit				
Data retention supply voltage	VDDDR		1.46 Note		5.5	V				

The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset Note is effected, but RAM data is not retained when a POR reset is effected.



2.8 **Flash Memory Programming Characteristics**

$(1A = -40 tO + 60 C, 1.6 V \le VDD \le 0.5 V, VSS = 0 V$	$(T_A = -40 \text{ to } +85^{\circ}\text{C}.)$	$1.8 \text{ V} \leq \text{VDD} \leq 5.5$	V. Vss = 0 V)
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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fclk	$1.8~V \leq V_{DD} \leq 5.5~V$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years Ta = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 **Dedicated Flash Memory Programmer Communication (UART)**

(TA = -40 to +85°C, 1.8 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps



(4) During communication at same potential (simplified I²C mode)

|--|

Parameter	Symbol	Conditions	HS (high-speed	HS (high-speed main) mode		
			MIN.	MAX.		
SCLr clock frequency	fscL	$\begin{array}{l} 2.7 \ \text{V} \leq EV_{\text{DD0}} \leq 5.5 \ \text{V}, \\ C_{b} = 50 \ \text{pF}, \ R_{b} = 2.7 \ \text{k}\Omega \end{array}$		400 Note 1	kHz	
		$\begin{array}{l} 2.4 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ C_{b} = 100 \ pF, \ R_{b} = 3 \ k\Omega \end{array}$		100 Note 1	kHz	
Hold time when SCLr = "L"	t∟ow	$\begin{array}{l} 2.7 \ \text{V} \leq E V_{\text{DD0}} \leq 5.5 \ \text{V}, \\ \text{C}_{\text{b}} = 50 \ \text{pF}, \ \text{R}_{\text{b}} = 2.7 \ \text{k}\Omega \end{array}$	1200		ns	
		$\begin{array}{l} 2.4 V \leq EV_{DD0} \leq 5.5 \; V, \\ C_{b} = 100 \; pF, \; R_{b} = 3 \; k\Omega \end{array}$	4600		ns	
Hold time when SCLr = "H"	tніgн	$\begin{array}{l} 2.7 \ \text{V} \leq E V_{\text{DD0}} \leq 5.5 \ \text{V}, \\ C_b = 50 \ \text{pF}, \ \text{R}_b = 2.7 \ \text{k}\Omega \end{array}$	1200		ns	
		$\begin{array}{l} 2.4 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ C_{b} \texttt{=} 100 \ pF, \ R_{b} \texttt{=} 3 \ k\Omega \end{array}$	4600		ns	
Data setup time (reception)	tsu: dat	$\begin{array}{l} 2.7 \ \text{V} \leq E V_{\text{DD0}} \leq 5.5 \ \text{V}, \\ C_b = 50 \ \text{pF}, \ \text{R}_b = 2.7 \ \text{k}\Omega \end{array}$	1/f _{MCK} + 220 Note 2		ns	
		$\label{eq:linear} \begin{split} 2.4 V &\leq E V_{DD0} \leq 5.5 \; V, \\ C_{b} &= 100 \; pF, \; R_{b} = 3 \; k \Omega \end{split}$	1/f _{MCK} + 580 Note 2		ns	
Data hold time (transmission)	thd: dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V},$ Cb = 50 pF, Rb = 2.7 k Ω	0	770	ns	
		$\begin{array}{l} 2.4 \ \text{V} \leq E V_{\text{DD0}} \leq 5.5 \ \text{V}, \\ \text{C}_{\text{b}} = 100 \ \text{pF}, \ \text{R}_{\text{b}} = 3 \ \text{k}\Omega \end{array}$	0	1420	ns	

Note 1. The value must also be equal to or less than fMCK/4.

Note 2. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)



The smaller maximum transfer rate derived by using fMck/12 or the following expression is the valid maximum transfer Note 5. rate.

Expression for calculating the transfer rate when 2.4 V \leq EVDD0 < 3.3 V and 1.6 V \leq Vb \leq 2.0 V

1

Maximum transfer rate =
$$\frac{1.5}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$

Baud rate e

$$\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}$$

$$(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Note 6. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.
- Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin Caution products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



(2) When reference voltage (+) = AVREFP/ANIO (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

Parameter	Symbol	Cond	Conditions		TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$		1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution	$3.6~V \leq V_{DD} \leq 5.5~V$	2.125		39	μs
		Target ANI pin: ANI16 to ANI20	$2.7~V \leq V_{DD} \leq 5.5~V$	3.1875		39	μs
			$2.4~V \leq V_{DD} \leq 5.5~V$	17		39	μs
Zero-scale error Notes 1, 2	Ezs	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$			±0.35	%FSR
Full-scale error Notes 1, 2	Efs	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$			±2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AVREFP and EVDD0	V

(TA = -40 to +105°C, 2.4 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, 2.4 V \leq AVREFP \leq VDD \leq 5.5 V, Vss = EVsso = EVss1 = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EVDD0 \le AVREFP \le VDD$, the MAX. values are as follows.

	Overall error:	Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
	Zero-scale error/Full-scale error:	Add $\pm 0.05\%$ FSR to the MAX. value when AVREFP = VDD.
	Integral linearity error/ Differential linearity error:	Add ±0.5 LSB to the MAX. value when AVREFP = VDD.
Note 4.	When AVREFP < EVDD0 \leq VDD, the MAX. values a	are as follows.
	Overall error:	Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error:

Add ±0.20%FSR to the MAX. value when AVREFP = VDD. Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.



(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +105°C, 2.4 V \leq VDD \leq 5.5 V, 1.6 V \leq EVDD = EVDD1 \leq VDD, Vss = EVss0 = EVss1 = 0 V,

Reference voltage (+) = VBGR Note 3, Reference voltage (-) = AVREFM = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Co	Conditions MIN. TYP. MAX.			MAX.	Unit
Resolution	RES		8			bit	
Conversion time	tCONV	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$	17		39	μs
Zero-scale error Notes 1, 2	Ezs	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.4~V \leq V_{DD} \leq 5.5~V$			±1.0	LSB
Analog input voltage	Vain			0		VBGR Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = Vss, the MAX. values are as follows.

Zero-scale error:Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.Integral linearity error:Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.Differential linearity error:Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.



3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, T _A = +25°C		1.05		V
Internal reference voltage	Vbgr	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	Fvtmps	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tamp		5			μs

(TA = -40 to +105°C, 2.4 V \leq VDD \leq 5.5 V, Vss = EVsso = EVss1 = 0 V, HS (high-speed main) mode)

3.6.3 D/A converter characteristics

(TA = -40 to +105°C, 2.4 V \leq EVsso = EVss1 \leq VDD \leq 5.5 V, Vss = EVsso = EVss1 = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 M Ω	$2.4~V \leq V_{DD} \leq 5.5~V$			±2.5	LSB
		Rload = 8 M Ω	$2.4~V \leq V_{DD} \leq 5.5~V$			±2.5	LSB
Settling time	t SET	Cload = 20 pF	$2.7~V \leq V_{DD} \leq 5.5~V$			3	μs
			$2.4~V \leq V_{DD} < 2.7~V$			6	μs



R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA R5F104LKALA, R5F104LLALA

R5F104LCGLA,R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA R5F104LKGLA, R5F104LLGLA



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R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA R5F104MKAFA, R5F104MLAFA R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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REVISION HISTORY	RL78/G14 Datasheet
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Pov Data			Description			
Nev.	Page		Summary			
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145	Modification of specifications in 3.3.2 Supply current characteristics			
		p.197	Modification of part number in 4.7 52-pin products			
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics			

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NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.