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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

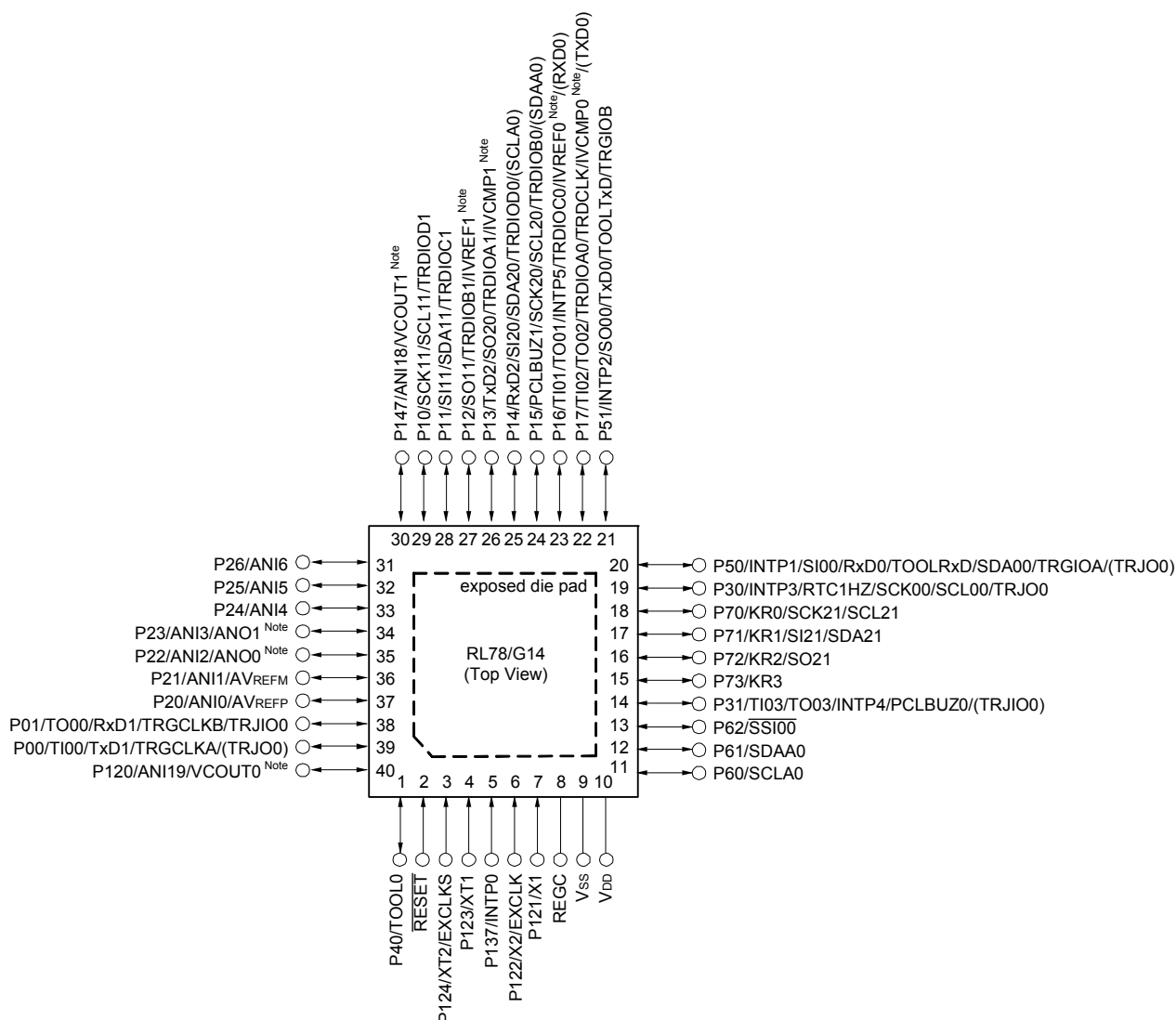
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104lhafb-v0

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

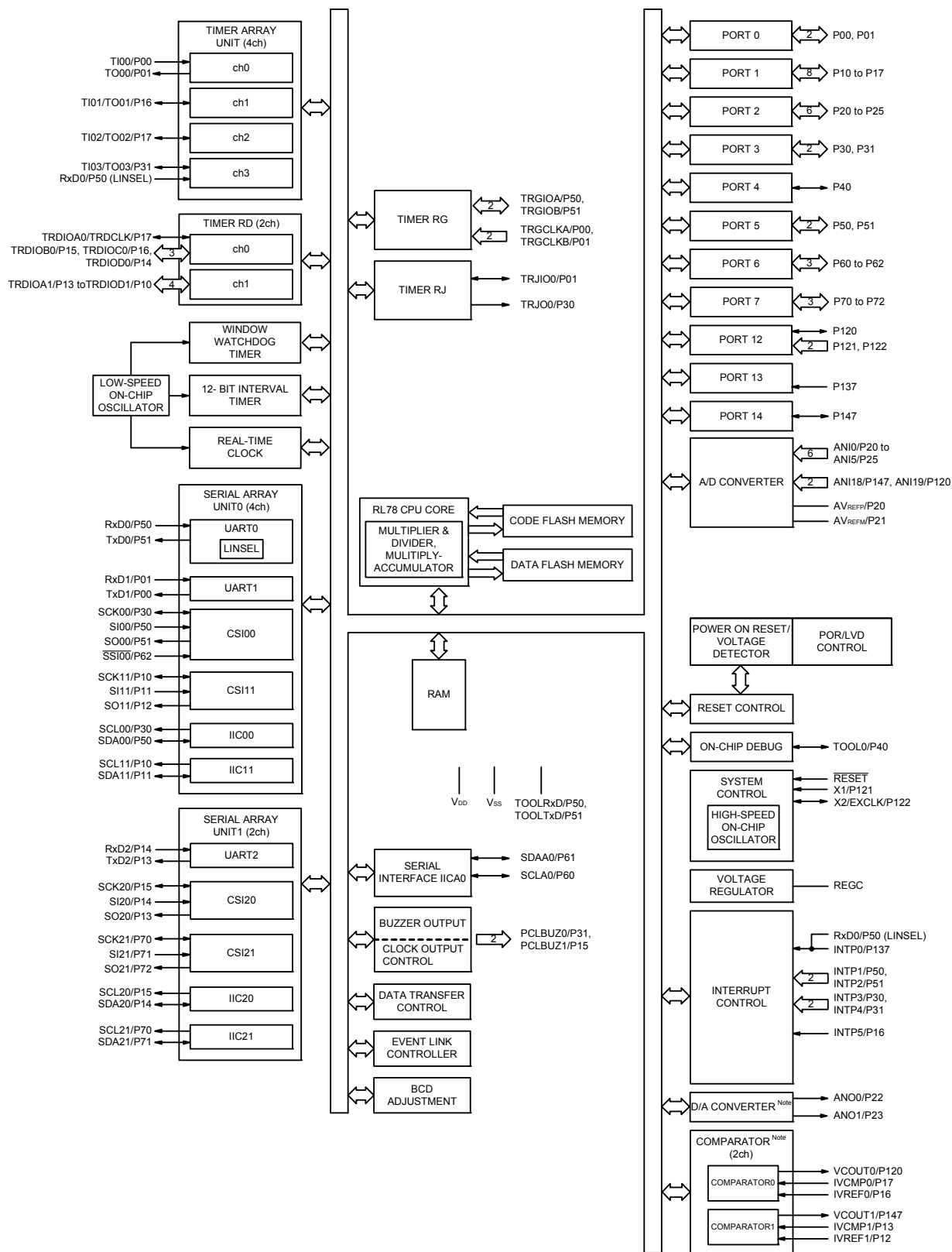
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to V_{SS}.

1.5.3 36-pin products



Note Mounted on the 96 KB or more code flash memory products.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.80	3.09	mA			
					VDD = 3.0 V		0.80	3.09				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	2.40				
					VDD = 3.0 V		0.49	2.40				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	2.40				
					VDD = 3.0 V		0.62	2.40				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	1.83				
					VDD = 3.0 V		0.4	1.83				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.37	1.38				
					VDD = 3.0 V		0.37	1.38				
				LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		260		710	μA	
						VDD = 2.0 V		260		710		
				LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		420		700	μA	
						VDD = 2.0 V		420		700		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.28	1.55	mA			
					Resonator connection		0.40	1.74				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.28		1.55		
						Resonator connection		0.40		1.74		
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.19		0.86		
						Resonator connection		0.25		0.93		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.19	0.86				
					Resonator connection		0.25	0.93				
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		95	550	μA		
						Resonator connection		140	590			
			fMX = 8 MHz Note 3, VDD = 2.0 V		Square wave input		95	550				
					Resonator connection		140	590				
			Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA			
					Resonator connection		0.44	0.76				
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57				
					Resonator connection		0.49	0.76				
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.36	1.17				
					Resonator connection		0.59	1.36				
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97				
					Resonator connection		0.72	2.16				
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37				
					Resonator connection		1.16	3.56				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.18	0.51	μA
					TA = +25°C					0.24	0.51	
					TA = +50°C					0.29	1.10	
					TA = +70°C					0.41	1.90	
					TA = +85°C					0.90	3.30	

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode Note 7	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	3.32	mA	
					VDD = 3.0 V		0.79	3.32		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	2.63		
					VDD = 3.0 V		0.49	2.63		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	2.57		
					VDD = 3.0 V		0.62	2.57		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.00		
					VDD = 3.0 V		0.4	2.00		
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	1.49		
					VDD = 3.0 V		0.38	1.49		
			LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		250	800	μA	
					VDD = 2.0 V		250	800		
			LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		420	755	μA	
					VDD = 2.0 V		420	755		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	1.63	mA	
					Resonator connection		0.40	1.85		
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30		1.63
					Resonator connection		0.40	1.85		
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20		0.89
					Resonator connection		0.25	0.97		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	0.89		
					Resonator connection		0.25	0.97		
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	580	μA
						Resonator connection		140	630	
			fMX = 8 MHz Note 3, VDD = 2.0 V		Square wave input		110	580		
					Resonator connection		140	630		
			Subsystem clock oper- ation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA	
					Resonator connection		0.47	0.85		
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66		
					Resonator connection		0.53	0.85		
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35		
					Resonator connection		0.56	2.54		
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08		
					Resonator connection		0.80	4.27		
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09		
					Resonator connection		1.74	8.28		
IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19	0.57	μA	
		TA = +25°C					0.25	0.57		
		TA = +50°C					0.33	2.26		
		TA = +70°C					0.52	3.99		
		TA = +85°C					1.46	8.00		

(Notes and Remarks are listed on the next page.)

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IIH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.9		mA
						V _{DD} = 3.0 V		2.9		
				f _{HOCO} = 32 MHz, f _{IIH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.5		
						V _{DD} = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IIH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		6.0	11.2	mA
						V _{DD} = 3.0 V		6.0	11.2	
				f _{HOCO} = 32 MHz, f _{IIH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.5	10.6	
						V _{DD} = 3.0 V		5.5	10.6	
				f _{HOCO} = 48 MHz, f _{IIH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.7	8.6	
						V _{DD} = 3.0 V		4.7	8.6	
				f _{HOCO} = 24 MHz, f _{IIH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.4	8.2	
						V _{DD} = 3.0 V		4.4	8.2	
				f _{HOCO} = 16 MHz, f _{IIH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.3	5.9	
						V _{DD} = 3.0 V		3.3	5.9	
			LS (low-speed main) mode Note 5	f _{HOCO} = 8 MHz, f _{IIH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.5	mA
						V _{DD} = 2.0 V		1.5	2.5	
			LV (low-voltage main) mode Note 5	f _{HOCO} = 4 MHz, f _{IIH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.1	mA
						V _{DD} = 2.0 V		1.5	2.1	
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8	
						Resonator connection		3.9	7.0	
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.3	4.1	
						Resonator connection		2.3	4.2	
			LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		5.2		μA
						Resonator connection		5.2		
				f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(Notes and Remarks are listed on the next page.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	8/fMCK		—		—		ns
			fMCK ≤ 20 MHz	6/fMCK		6/fMCK		6/fMCK		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	8/fMCK		—		—		ns
			fMCK ≤ 16 MHz	6/fMCK		6/fMCK		6/fMCK		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 500		6/fMCK and 500		6/fMCK and 500		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 750		6/fMCK and 750		6/fMCK and 750		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 1500		6/fMCK and 1500		6/fMCK and 1500		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		6/fMCK and 1500		6/fMCK and 1500		ns
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 7		tkCY2/2 - 7		tkCY2/2 - 7		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 8		tkCY2/2 - 8		tkCY2/2 - 8		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 18		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 66		tkCY2/2 - 66		tkCY2/2 - 66		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		tkCY2/2 - 66		tkCY2/2 - 66		ns
Slp setup time (to SCKp↑) Note 1	tsiK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 40		1/fMCK + 40		1/fMCK + 40		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		1/fMCK + 40		1/fMCK + 40		ns
Slp hold time (from SCKp↑) Note 2	tshiK2	1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 250		1/fMCK + 250		1/fMCK + 250		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		1/fMCK + 250		1/fMCK + 250		ns
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 44		2/fMCK + 110		2/fMCK + 110	ns
			2.4 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 75		2/fMCK + 110		2/fMCK + 110	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 100		2/fMCK + 110		2/fMCK + 110	ns
			1.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 220		2/fMCK + 220		2/fMCK + 220	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V		—		2/fMCK + 220		2/fMCK + 220	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

2.5.2 Serial interface IICA

(1) I²C standard mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t _{SU: STA}	2.7 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		4.7		4.7		μs
Hold time ^{Note 1}	t _{HD: STA}	2.7 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		4.0		4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V		4.7		4.7		4.7		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		4.7		4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V		4.0		4.0		4.0		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		4.0		4.0		μs

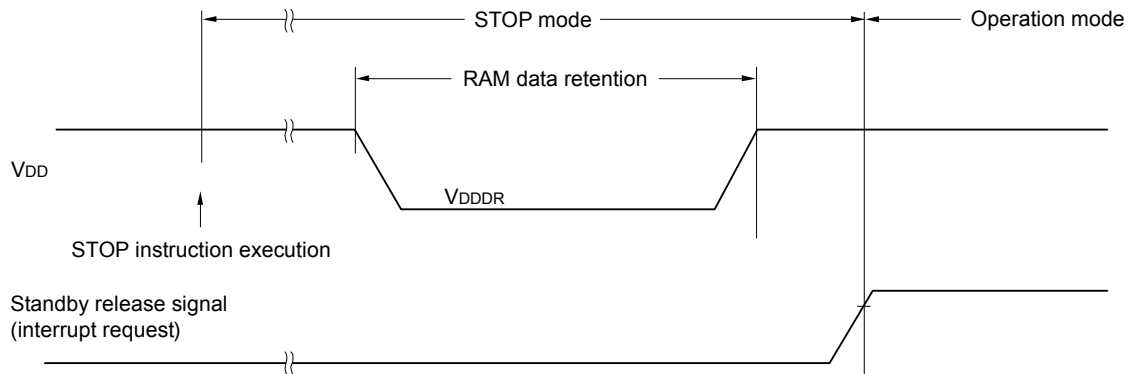
(Notes, Caution, and Remark are listed on the next page.)

2.7 RAM Data Retention Characteristics

(TA = -40 to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

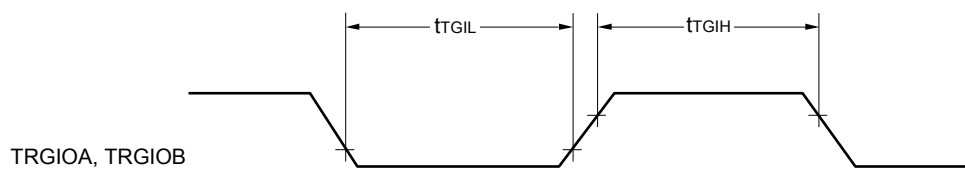
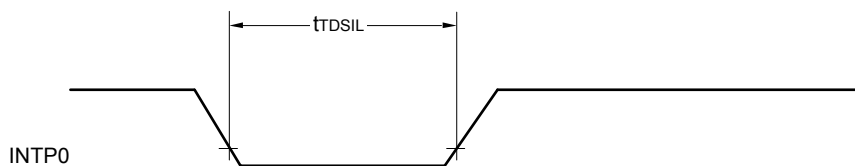
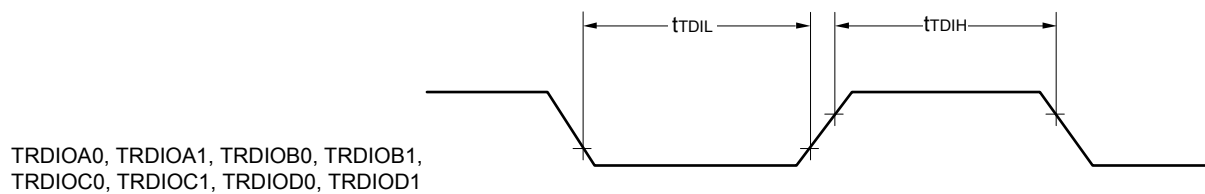
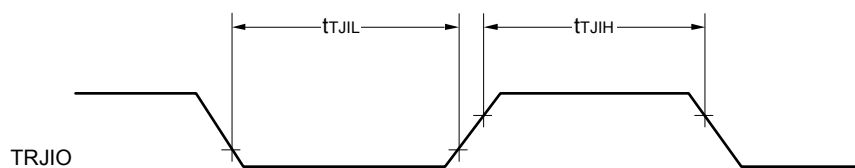
- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

<R>

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	5.16	mA	
					VDD = 3.0 V		0.93	5.16		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	4.47		
					VDD = 3.0 V		0.5	4.47		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	4.08		
					VDD = 3.0 V		0.72	4.08		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	3.51		
					VDD = 3.0 V		0.42	3.51		
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	2.38		
					VDD = 3.0 V		0.39	2.38		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	2.83	mA	
					Resonator connection		0.41	2.92		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	2.83		
					Resonator connection		0.41	2.92		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21	1.46		
					Resonator connection		0.26	1.57		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	1.46		
					Resonator connection		0.26	1.57		
		Subsystem clock operation	fsUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31	0.76	μA		
				Resonator connection		0.50	0.95			
				fsUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.38		0.76	
					Resonator connection		0.57		0.95	
				fsUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47		3.59	
					Resonator connection		0.70		3.78	
				fsUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80		6.20	
					Resonator connection		1.00		6.39	
				fsUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65		10.56	
					Resonator connection		1.84		10.75	
				fsUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		8.00		65.7	
					Resonator connection		8.00		65.7	
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19	0.63	μA
			TA = +25°C					0.30	0.63	
			TA = +50°C					0.41	3.47	
			TA = +70°C					0.80	6.08	
			TA = +85°C					1.53	10.44	
			TA = +105°C					6.50	67.14	

(Notes and Remarks are listed on the next page.)



(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	tsik1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	tkS11	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/ EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

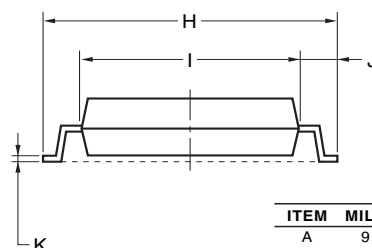
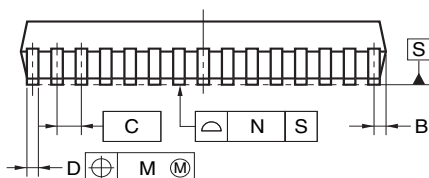
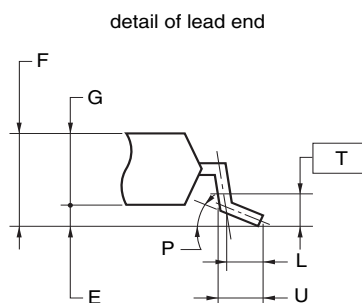
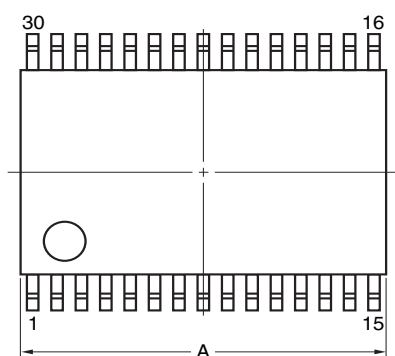
(Remarks are listed on the page after the next page.)

4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
 R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
 R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

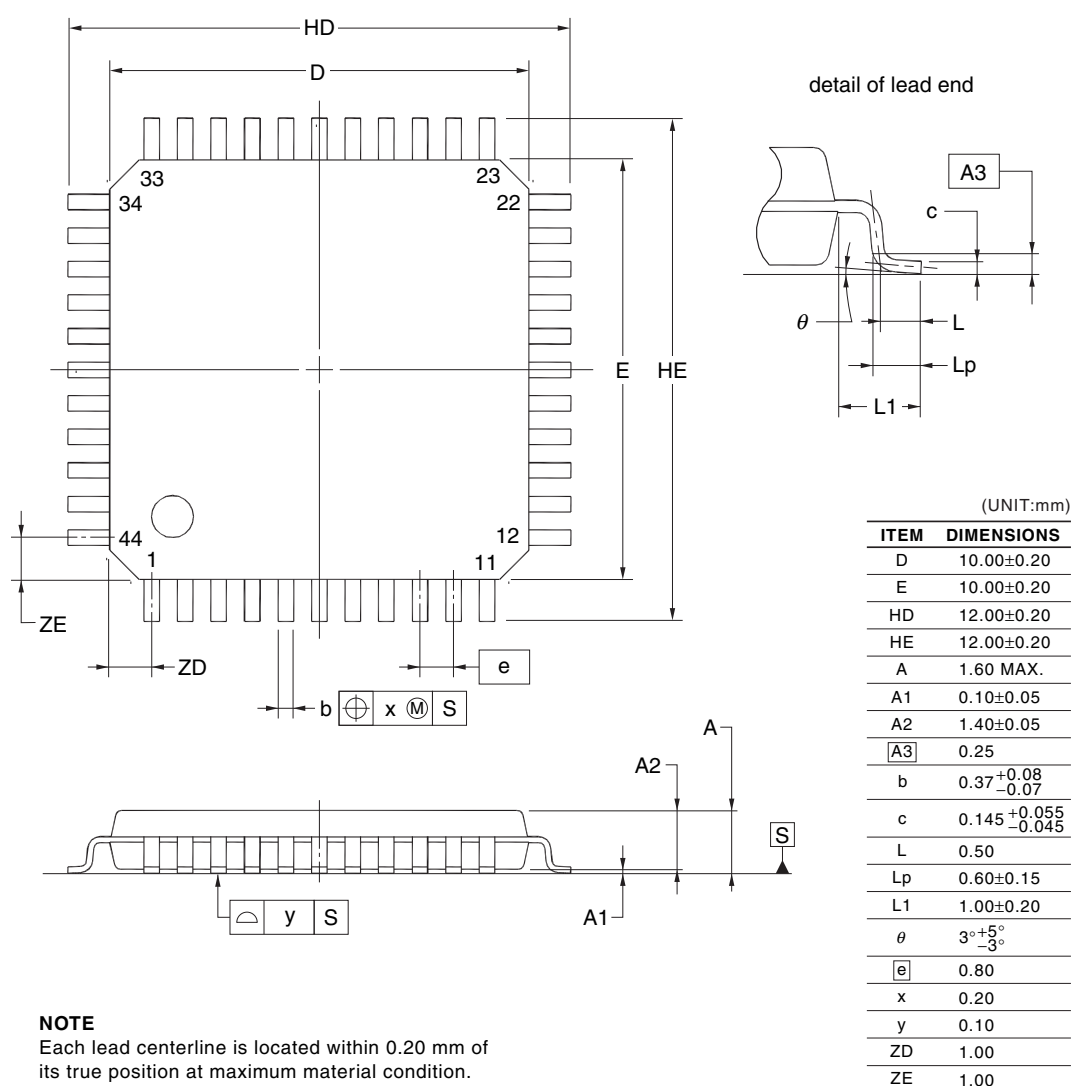
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

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4.5 44-pin products

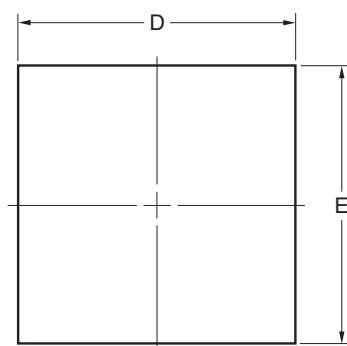
R5F104FAAFP, R5F104FCAFP, R5F104FDAFP, R5F104FEAFP, R5F104FFAFP, R5F104FGAFP,
 R5F104FHAFP, R5F104FJAFP
 R5F104FADFP, R5F104FCDFP, R5F104FDDFP, R5F104FEDFP, R5F104FFDFP, R5F104FGDFP,
 R5F104FHDFP, R5F104FJDFP
 R5F104FAGFP, R5F104FCGFP, R5F104FDGFP, R5F104FEGFP, R5F104FFGFP, R5F104FGGFP,
 R5F104FHGFP, R5F104FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36

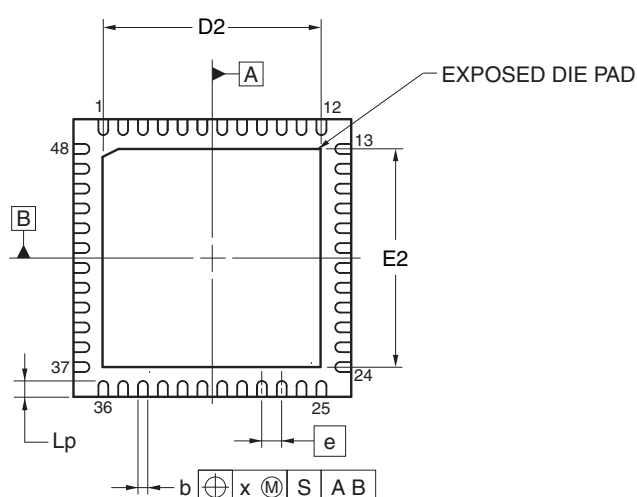
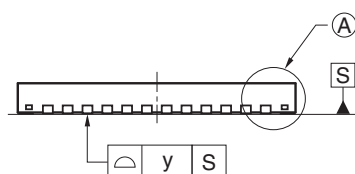
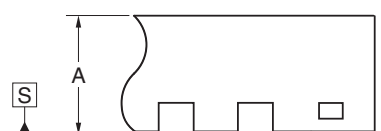


R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA,
 R5F104GHANA, R5F104GJANA
 R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA,
 R5F104GHDNA, R5F104GJDNA
 R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,
 R5F104GHGNA, R5F104GJGNA
 R5F104GKANA, R5F104GLANA
 R5F104GKGNA, R5F104GLGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



DETAIL OF (A) PART

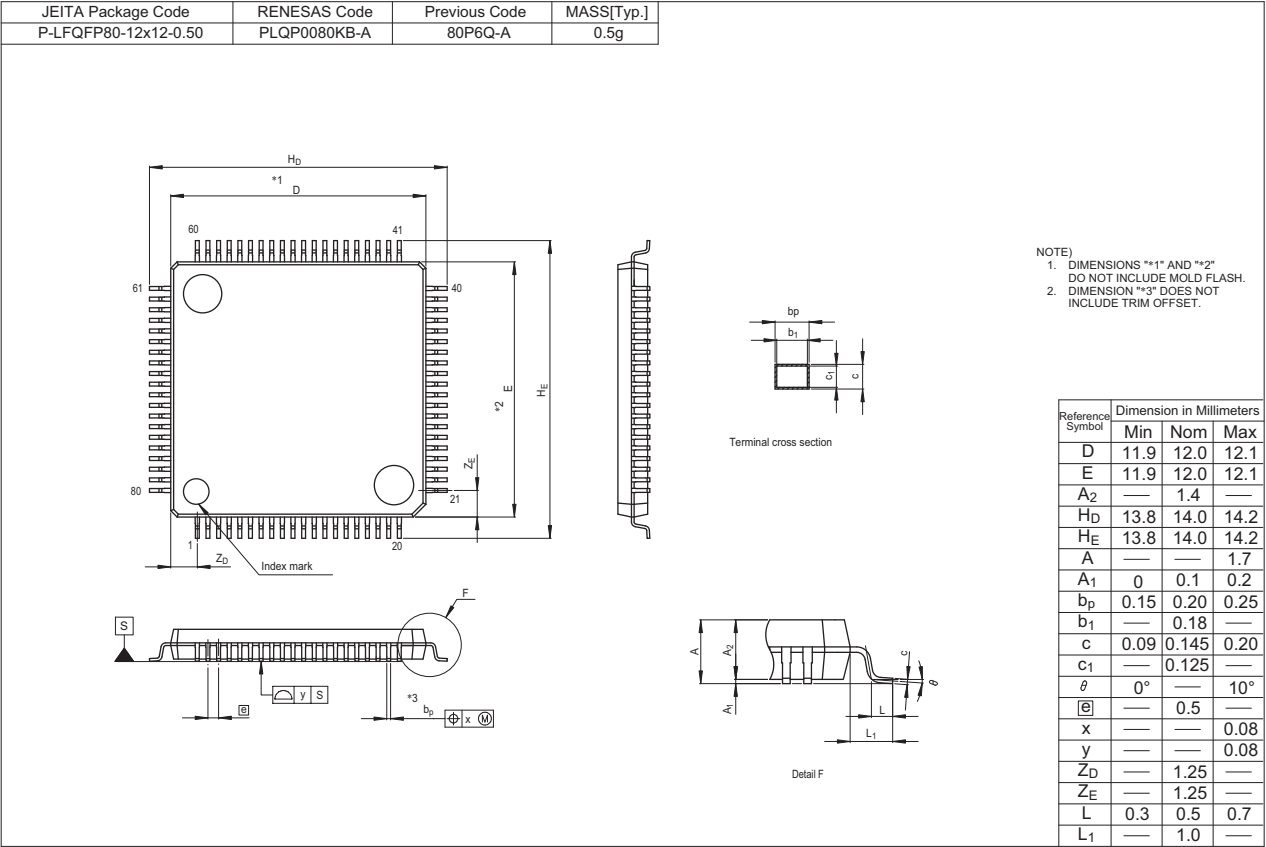


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB



REVISION HISTORY	RL78/G14 Datasheet
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Rev.	Date	Description	
		Page	Summary
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145 p.197	Modification of specifications in 3.3.2 Supply current characteristics Modification of part number in 4.7 52-pin products
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics

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