Renesas Electronics America Inc - R5F104LJAFB#30 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

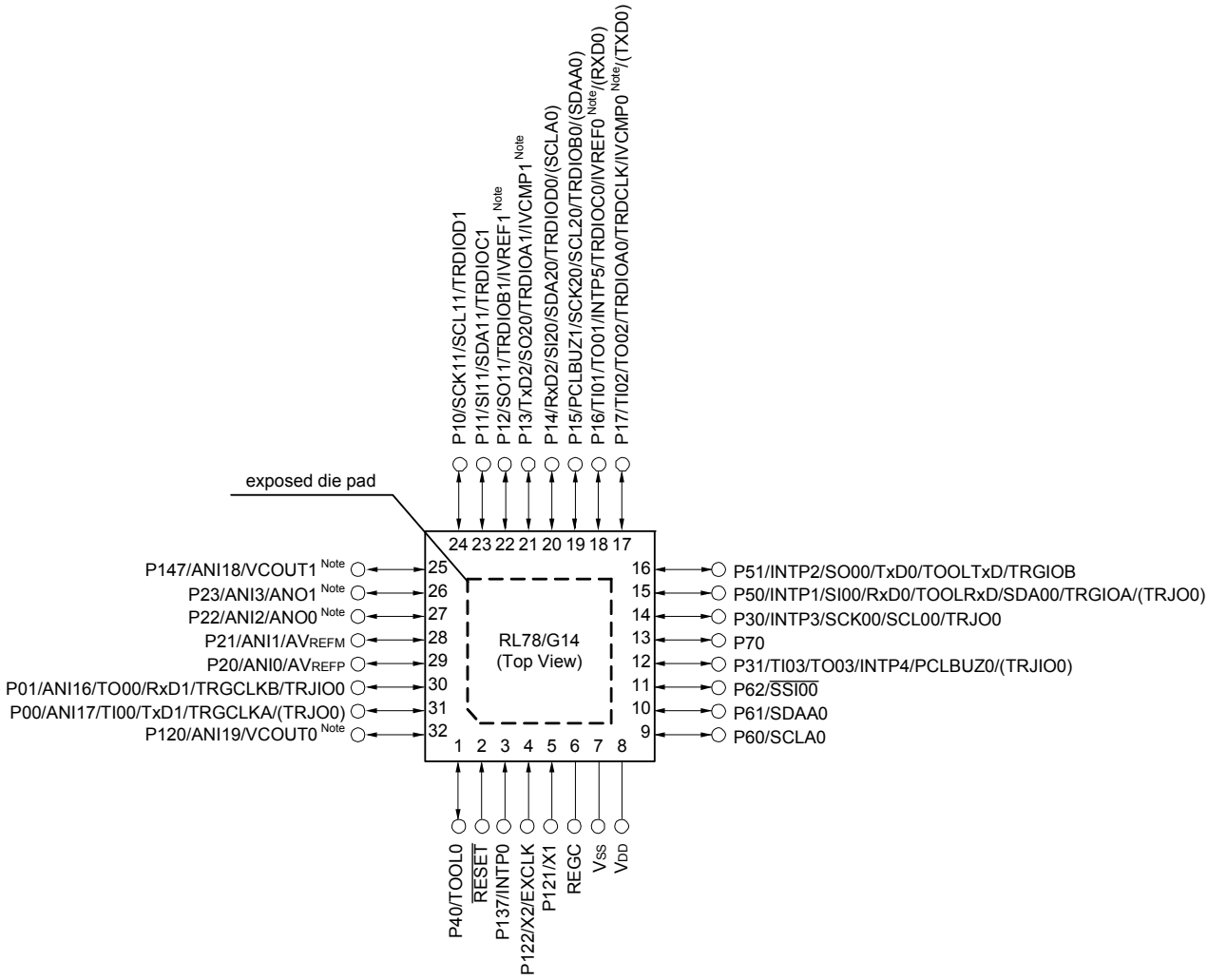
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ljafb-30

1.3.2 32-pin products

• 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

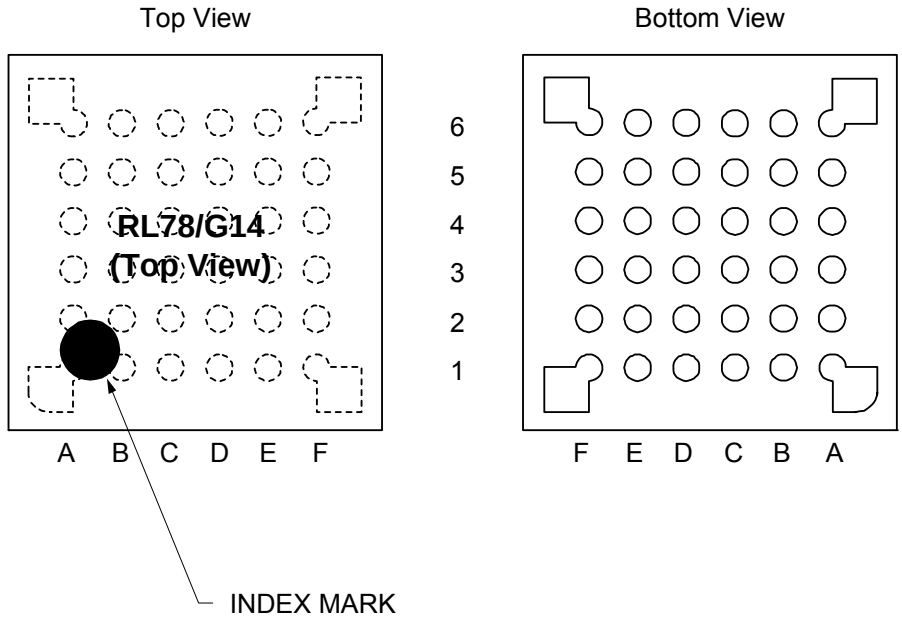
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.3 36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	P60/SCLA0	VDD	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62/$\overline{SSI00}$	P61/SDAA0	VSS	REGC	$\overline{RESET}$	P120/ANI19/ VCOUT0 Note	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0)	P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0)	P00/TI00/TxD1/ TRGCLKA/ (TRJO0)	P01/TO00/ RxD1/TRGCLKB/ TRJIO0	4
3	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0)	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0)	P22/ANI2/ ANO0 Note	P20/ANI0/ AVREFP	P21/ANI1/ AVREFM	3
2	P30/INTP3/ SCK00/SCL00/ TRJO0	P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0)	P12/SO11/ TRDIOB1/ IVREF1 Note	P11/SI11/ SDA11/ TRDIOC1	P24/ANI4	P23/ANI3/ ANO1 Note	2
1	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note/ (TXD0)	P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note	P10/SCK11/ SCL11/ TRDIOD1	P147/ANI18/ VCOUT1 Note	P25/ANI5	1
	A	B	C	D	E	F	

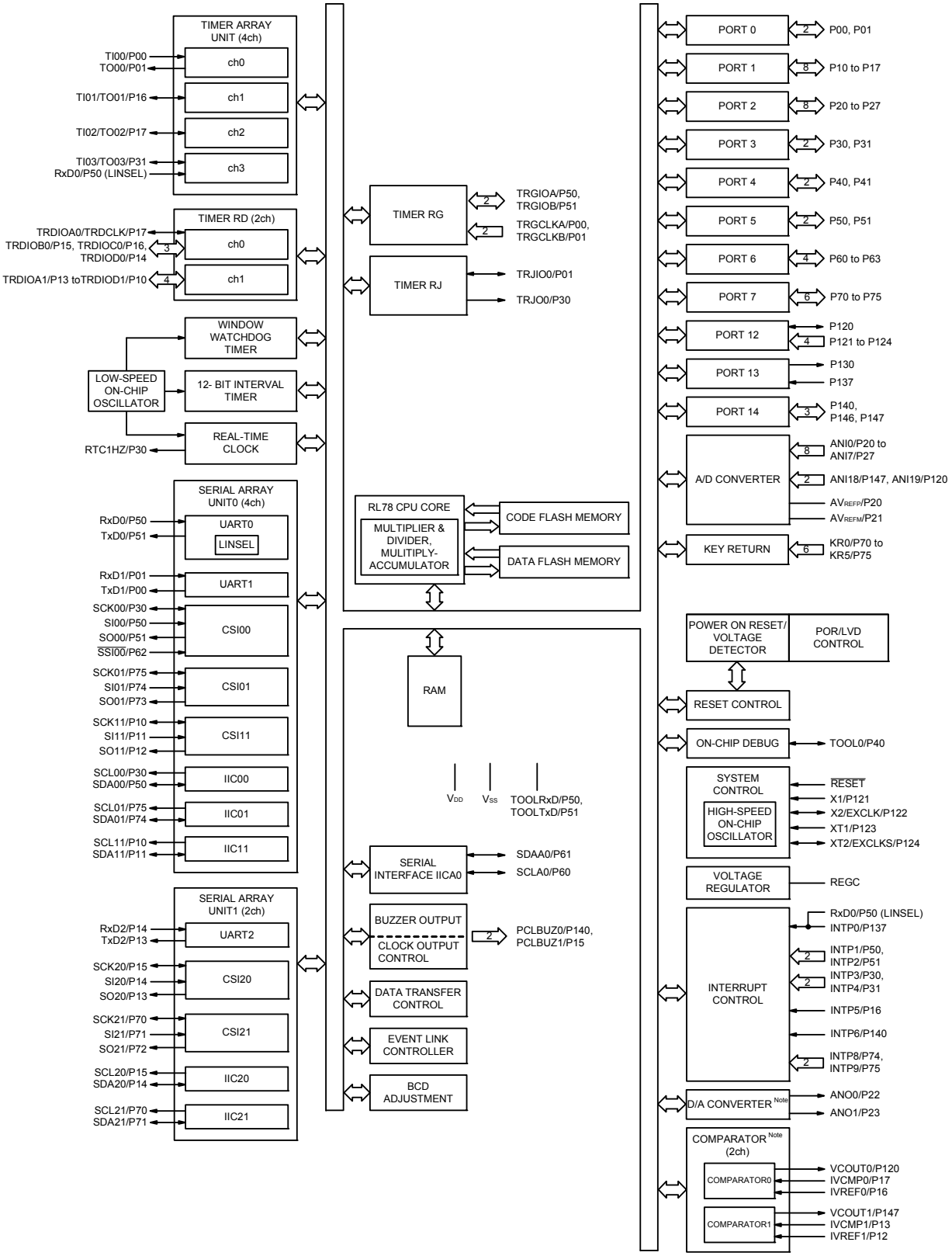
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.6 48-pin products



Note Mounted on the 96 KB or more code flash memory products.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin R5F104Fx (x = A, C to E)	48-pin R5F104Gx (x = A, C to E)	52-pin R5F104Jx (x = C to E)	64-pin R5F104Lx (x = C to E)
Code flash memory (KB)		16 to 64	16 to 64	32 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	4 to 5.5 Note	4 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)			

(**Note** is listed on the next page.)

(2/2)

Item		44-pin R5F104Fx (x = A, C to E)	48-pin R5F104Gx (x = A, C to E)	52-pin R5F104Jx (x = C to E)	64-pin R5F104Lx (x = C to E)
Clock output/buzzer output		2	2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		10 channels	10 channels	12 channels	12 channels
Serial interface		[44-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels [48-pin, 52-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels			
	I^2C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		29 sources	30 sources		31 sources
Event link controller (ELC)		Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt		4	6	8	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (T_A = –40 to +85°C) 1.51 ±0.06 V (T_A = –40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = –40 to +85°C) 1.50 ±0.06 V (T_A = –40 to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)			
Operating ambient temperature		T_A = –40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications T_A = -40 to +85°C
R5F104xxAxx
D: Industrial applications T_A = -40 to +85°C
R5F104xxDxx
G: Industrial applications when T_A = -40 to +105°C products is used in the range of T_A = -40 to +85°C
R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual**.**

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/2)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV_{DD0} +0.3 and -0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV_{DD0} +0.3 and -0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI20	-0.3 to EV_{DD0} +0.3 and -0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} +0.3 and -0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

Absolute Maximum Ratings **(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-55.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-80.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-5.0	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-135.0 Note 4	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V			-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Note 4. -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/f_{CLK}			ns
Timer RD forced cutoff signal input low-level width	t_{TDSIL}	P130/INTP0	2MHz < f_{CLK} ≤ 32 MHz	1			µs
			f_{CLK} ≤ 2 MHz	1/f_{CLK} + 1			
Timer RG input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB		2.5/f_{CLK}			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EV_{DD0} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EV_{DD0} ≤ 5.5 V			4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.6 V ≤ V_{DD} ≤ 5.5 V	1			µs
		INTP1 to INTP11	1.6 V ≤ EV_{DD0} ≤ 5.5 V	1			µs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	1.8 V ≤ EV_{DD0} ≤ 5.5 V	250			ns
			1.6 V ≤ EV_{DD0} < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		µs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5		1.2	±8.5	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} Notes 3, 4	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 5			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD0} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 5. When the conversion time is set to 57 µs (min.) and 95 µs (max.).

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.4		mA
						V_{DD} = 3.0 V		2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		
						V_{DD} = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.1	9.3	mA
						V_{DD} = 3.0 V		5.1	9.3	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	8.7	
						V_{DD} = 3.0 V		4.8	8.7	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	7.3	
						V_{DD} = 3.0 V		4.0	7.3	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.8	6.7	
						V_{DD} = 3.0 V		3.8	6.7	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.9	
						V_{DD} = 3.0 V		2.8	4.9	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.7	mA
						Resonator connection		3.4	5.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.7	
						Resonator connection		3.4	5.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.4	
						Resonator connection		2.1	3.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.4	
						Resonator connection		2.1	3.5	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.7	6.1	µA
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.7	6.1	
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.8	6.7	
						Resonator connection		4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.8	7.5	
						Resonator connection		4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.4	8.9	
						Resonator connection		5.4	8.9	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		7.2	21.0	
						Resonator connection		7.3	21.1	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

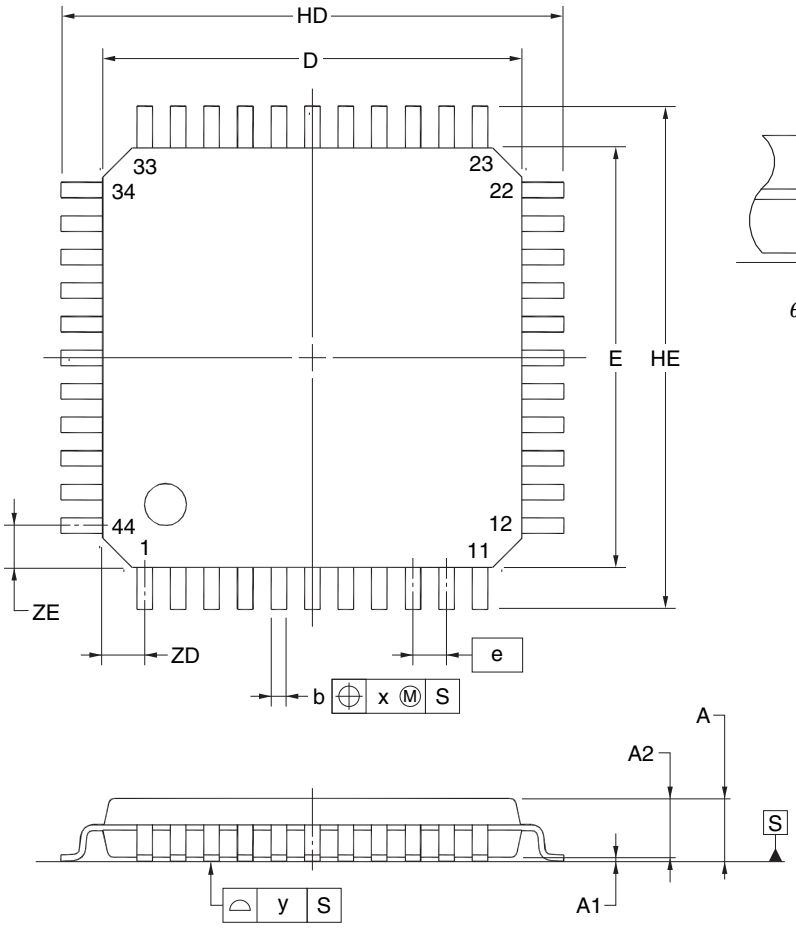
Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

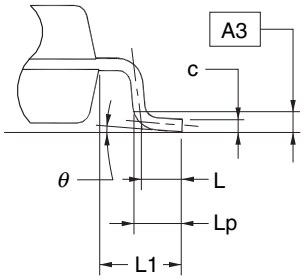
Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

4.5 44-pin products

R5F104FAAFP, R5F104FCAFP, R5F104FDAFP, R5F104FEAFP, R5F104FFAFP, R5F104FGAFP, R5F104FHAFP, R5F104FJAFP
R5F104FADFP, R5F104FCDFP, R5F104FDDFP, R5F104FEDFP, R5F104FFDFP, R5F104FGDFP, R5F104FHDFP, R5F104FJDFP
R5F104FAGFP, R5F104FCGFP, R5F104FDGFP, R5F104FEGFP, R5F104FFGFP, R5F104FGGFP, R5F104FHGFP, R5F104FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36





(UNIT:mm)

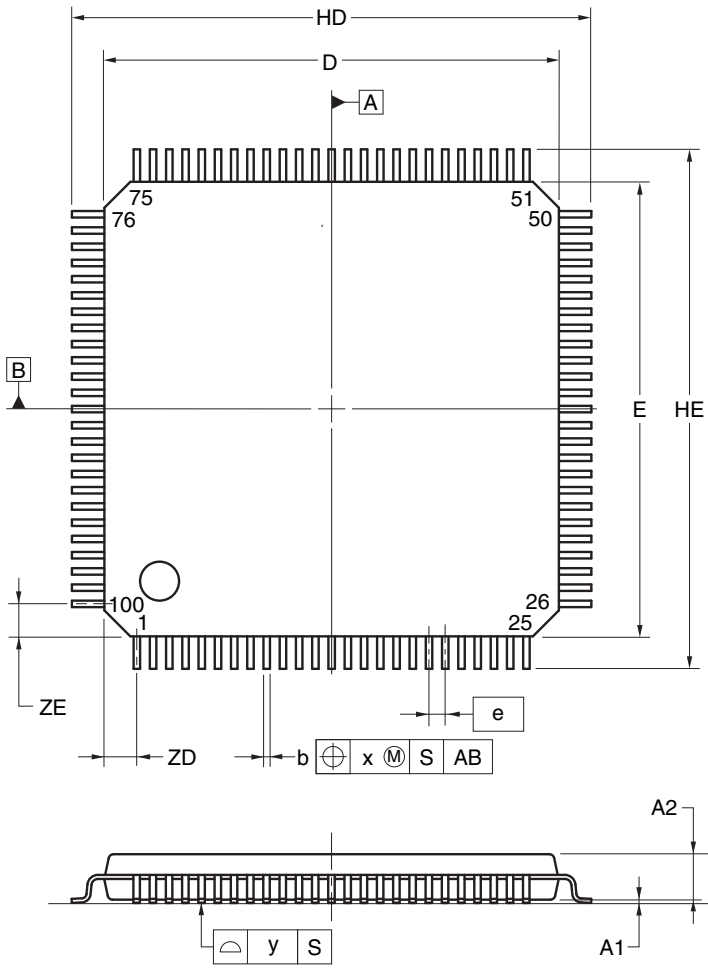
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

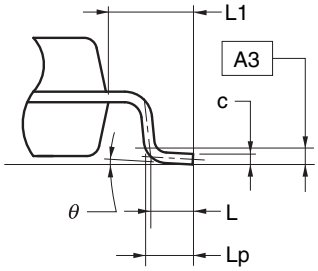
4.10 100-pin products

R5F104PFAFB, R5F104PGAFB, R5F104PHAFB, R5F104PJAFB
R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

REVISION HISTORY	RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145	Modification of specifications in 3.3.2 Supply current characteristics
		p.197	Modification of part number in 4.7 52-pin products
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics