**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

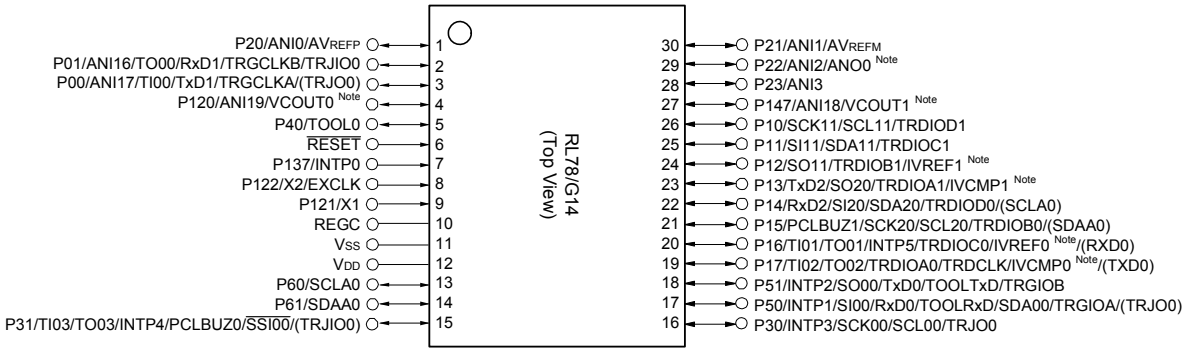
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ljafb-x0 |

## 1.3 Pin Configuration (Top View)

### 1.3.1 30-pin products

• 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

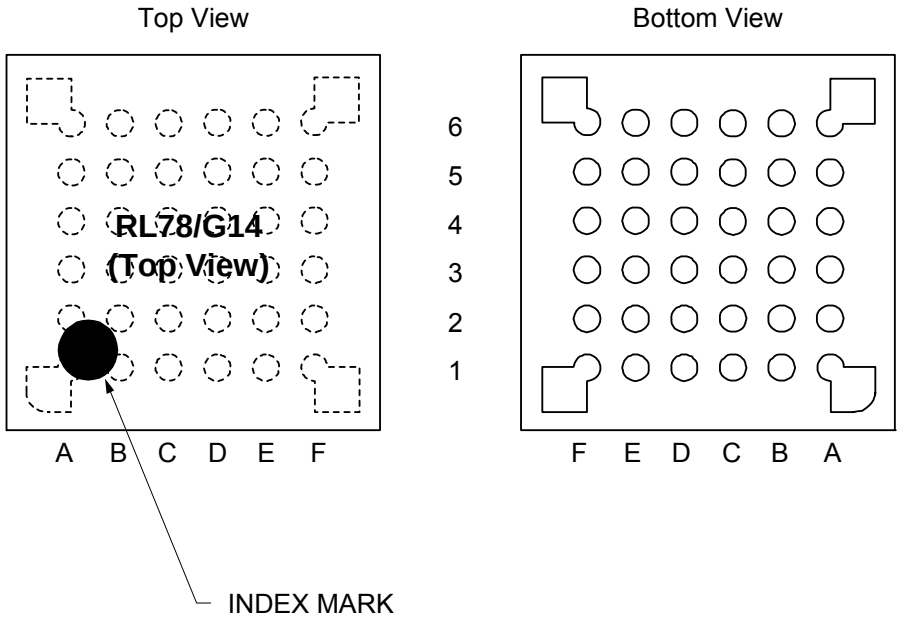
**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.3 36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)




| | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|
| 6 | P60/SCLA0 | VDD | P121/X1 | P122/X2/EXCLK | P137/INTP0 | P40/TOOL0 | 6 |
| 5 | P62/$\overline{SSI00}$ | P61/SDAA0 | VSS | REGC | $\overline{RESET}$ | P120/ANI19/ VCOUT0 Note | 5 |
| 4 | P72/SO21 | P71/SI21/ SDA21 | P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0) | P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0) | P00/TI00/TxD1/ TRGCLKA/ (TRJO0) | P01/TO00/ RxD1/TRGCLKB/ TRJIO0 | 4 |
| 3 | P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0) | P70/SCK21/ SCL21 | P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0) | P22/ANI2/ ANO0 Note | P20/ANI0/ AVREFP | P21/ANI1/ AVREFM | 3 |
| 2 | P30/INTP3/ SCK00/SCL00/ TRJO0 | P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0) | P12/SO11/ TRDIOB1/ IVREF1 Note | P11/SI11/ SDA11/ TRDIOC1 | P24/ANI4 | P23/ANI3/ ANO1 Note | 2 |
| 1 | P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB | P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note/ (TXD0) | P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note | P10/SCK11/ SCL11/ TRDIOD1 | P147/ANI18/ VCOUT1 Note | P25/ANI5 | 1 |
| | A | B | C | D | E | F | |

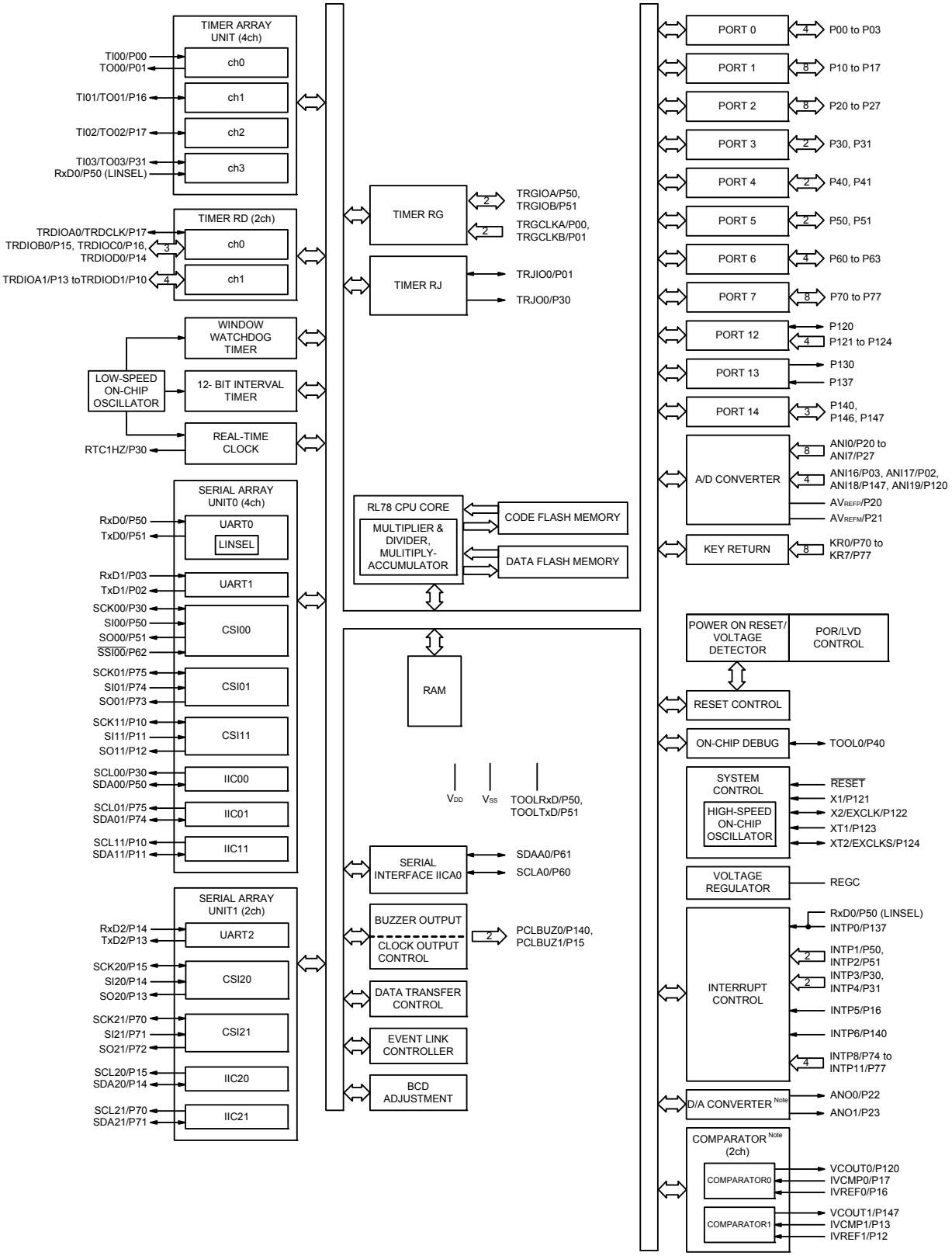
**Note** Mounted on the 96 KB or more code flash memory products.

**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

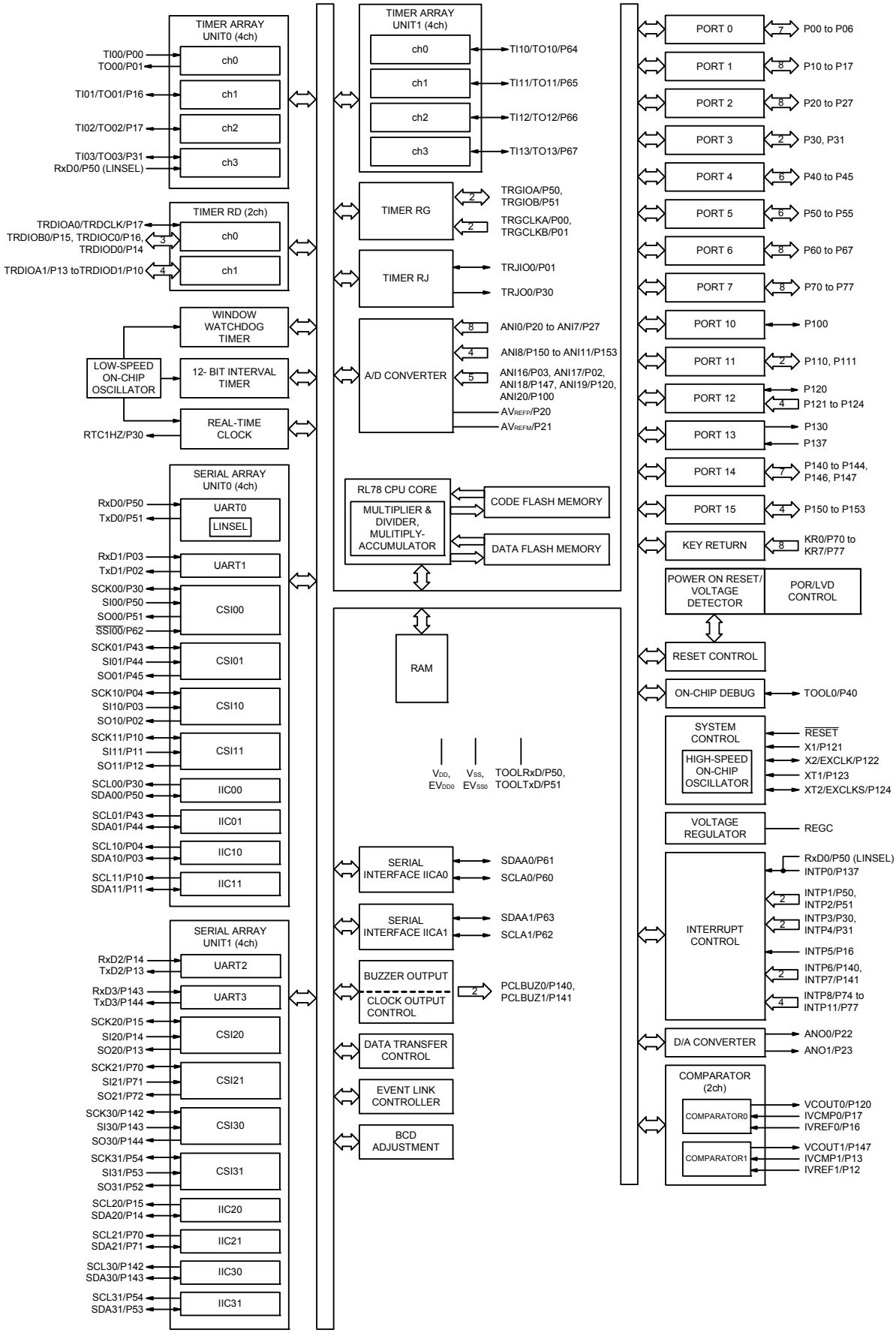
**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

## 1.5.7 52-pin products




**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.9 80-pin products



**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = F, G) | R5F104Bx (x = F, G) | R5F104Cx (x = F, G) | R5F104Ex (x = F to H) |
| Code flash memory (KB) | | 96 to 128 | 96 to 128 | 96 to 128 | 96 to 192 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 16 Note | 12 to 16 Note | 12 to 16 Note | 12 to 20 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | — | | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | — | | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 26 | 28 | 32 | 36 |
| | CMOS I/O | 21 | 22 | 26 | 28 |
| | CMOS input | 3 | 3 | 3 | 5 |
| | CMOS output | — | — | — | — |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 3 | 3 | 3 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |

(**Note** is listed on the next page.)

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use it with $EV_{DD0} \geq V_b$.

**Note 6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 7.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### (2) $I^2C$ fast mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$ Reference voltage (-)= $AV_{REFM}$ |
|---|---|---|---|
| ANI0 to ANI14 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI20 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | 1.2 | ±7.0 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±5.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±2.0 | LSB |
| Analog input voltage | VAIN | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 5 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 5 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** Values when the conversion time is set to 57 µs (min.) and 95 µs (max.).

**Note 5.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = -40 to +105°C

R5F104xxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.**

**Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When RL78/G14 is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

## 3.3.2 Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.1 | 9.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.1 | 9.3 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.7 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.3 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.7 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | mA |
| | | | | | | Resonator connection | | 3.4 | 5.8 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | |
| | | | | | | Resonator connection | | 3.4 | 5.8 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 7.2 | 21.0 | |
| | | | | | | Resonator connection | | 7.3 | 21.1 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03, TI10 to TI13 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

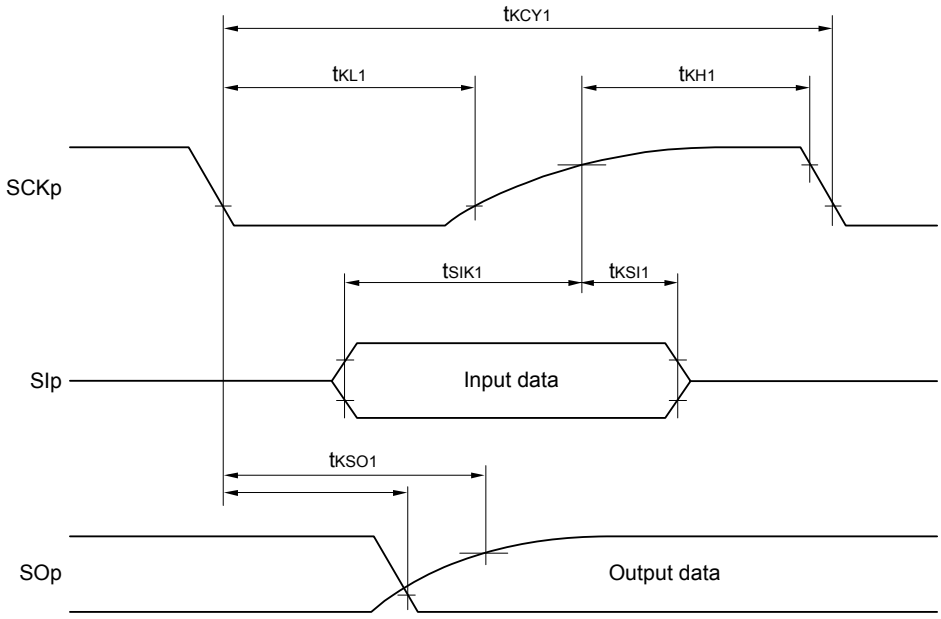
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 150 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

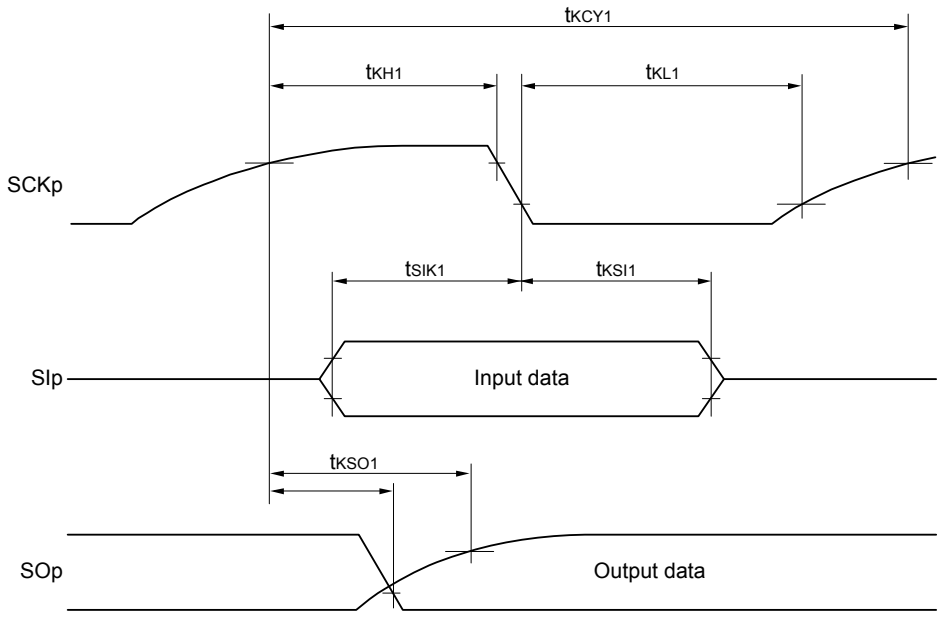
**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

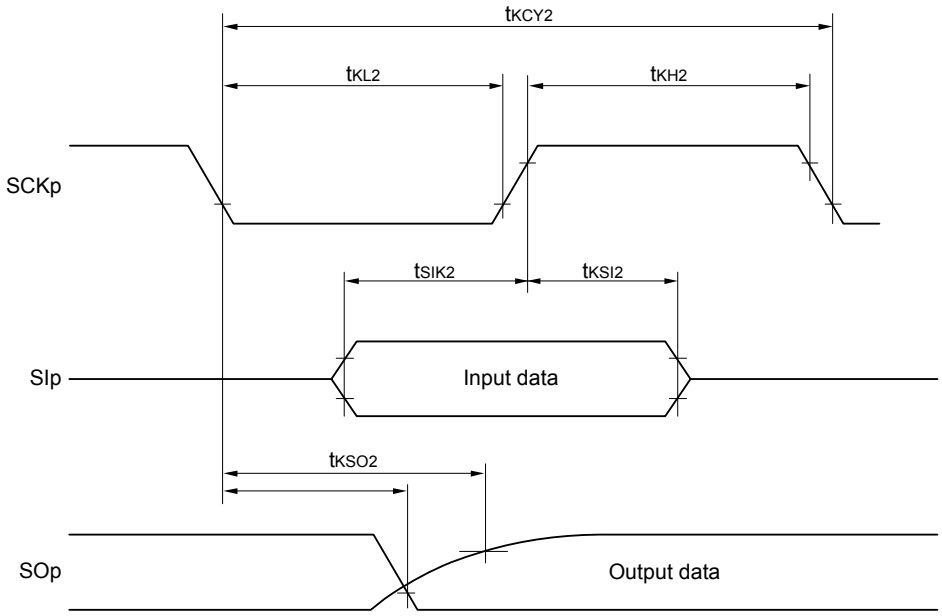
### (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

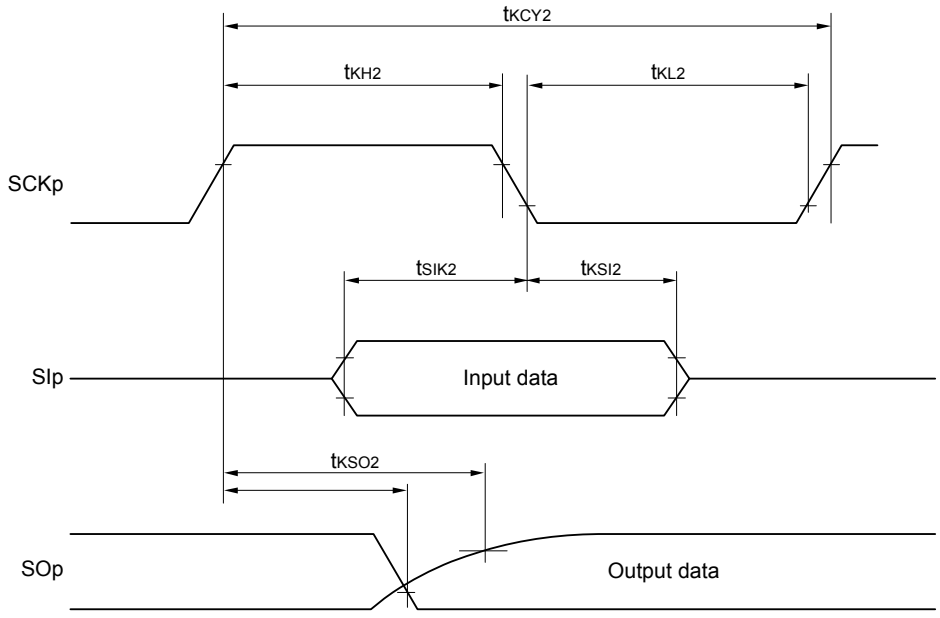
| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

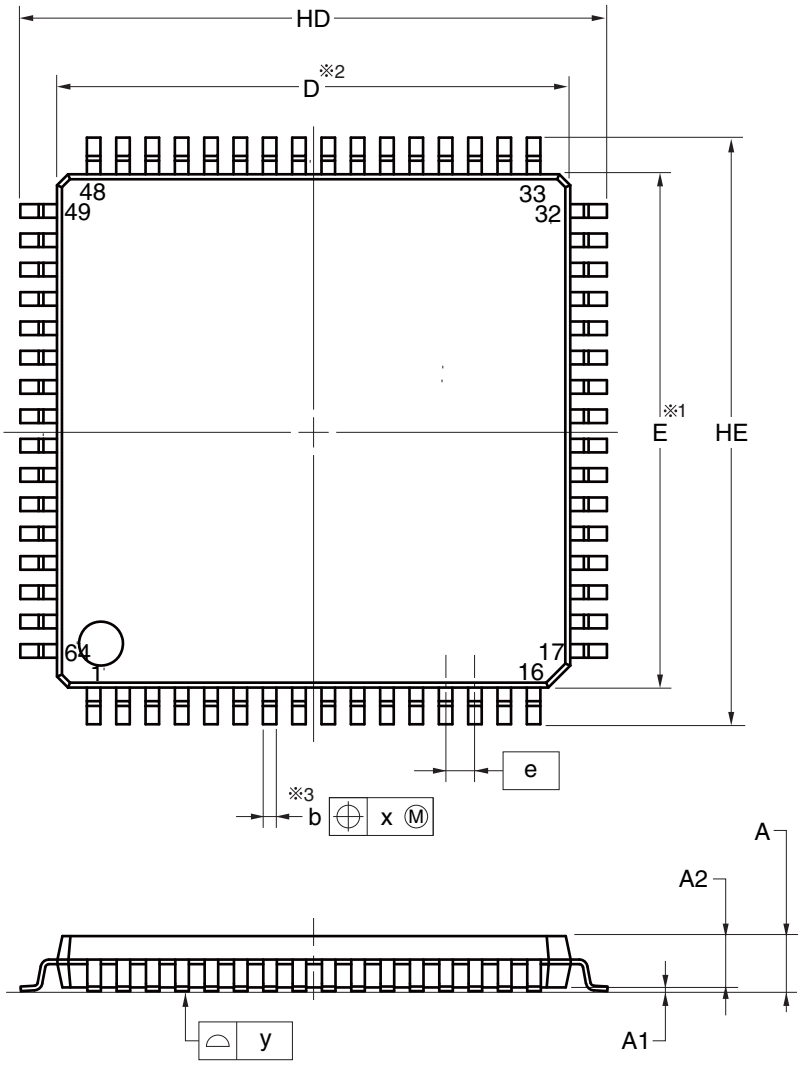
### 3.6.3 D/A converter characteristics

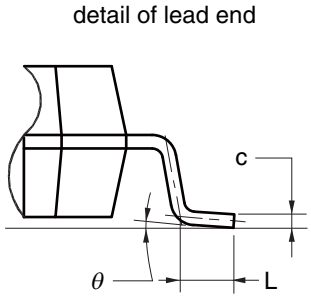
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{SS0}$ = $EV_{SS1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | $t_{SET}$ | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 3 | μs |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 6 | μs |

R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LFDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | P64GC-80-GBW-1 | 0.7 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.10 |
| E | 14.00±0.10 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | $0.37^{+0.08}_{-0.05}$ |
| c | $0.125^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.