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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104ljgfb-v0

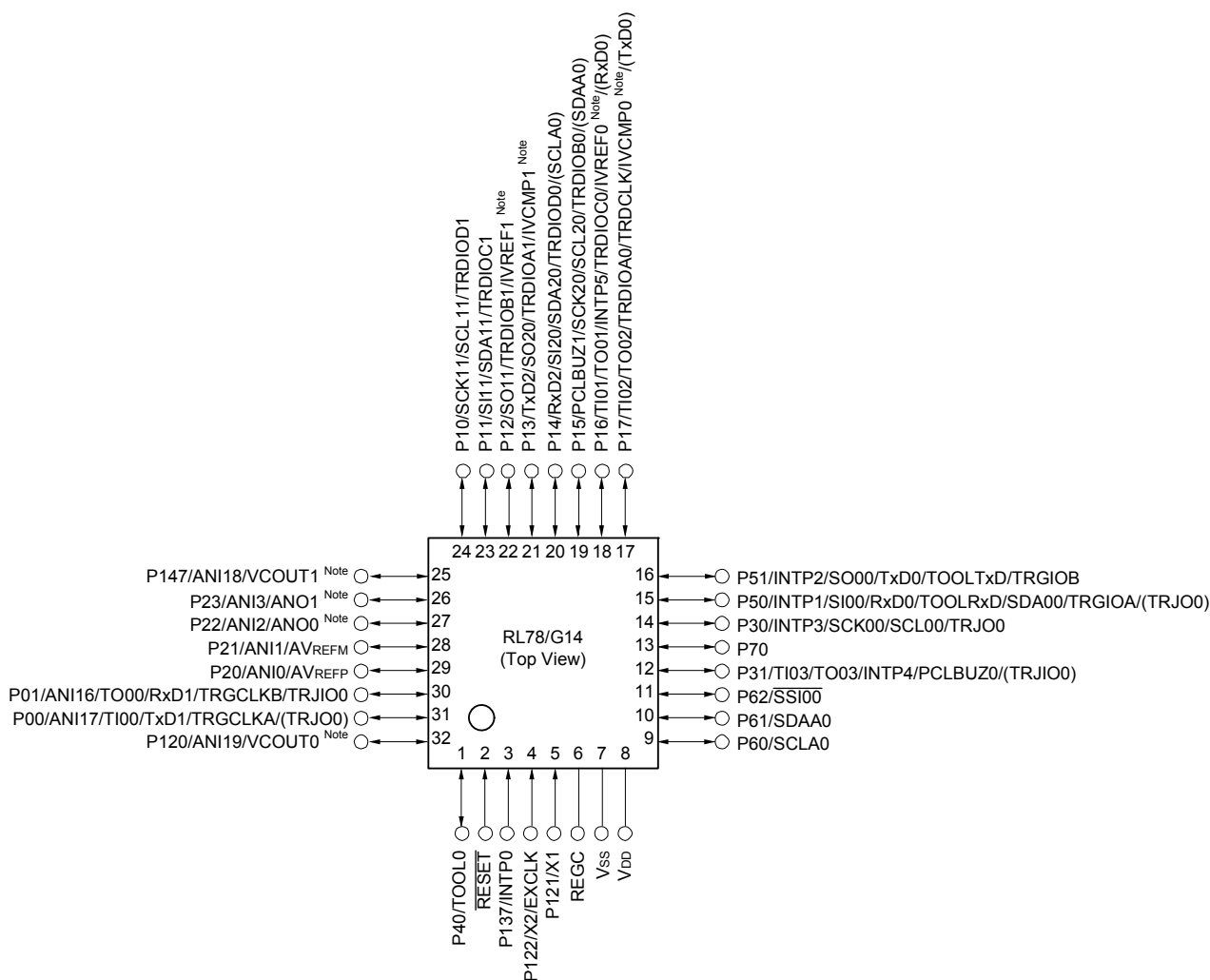
(1/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0 R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0 R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0 R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0 R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0 R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0 R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0 R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BDFP#V0, R5F104BGDFP#V0 R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0 R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0 R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0 R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

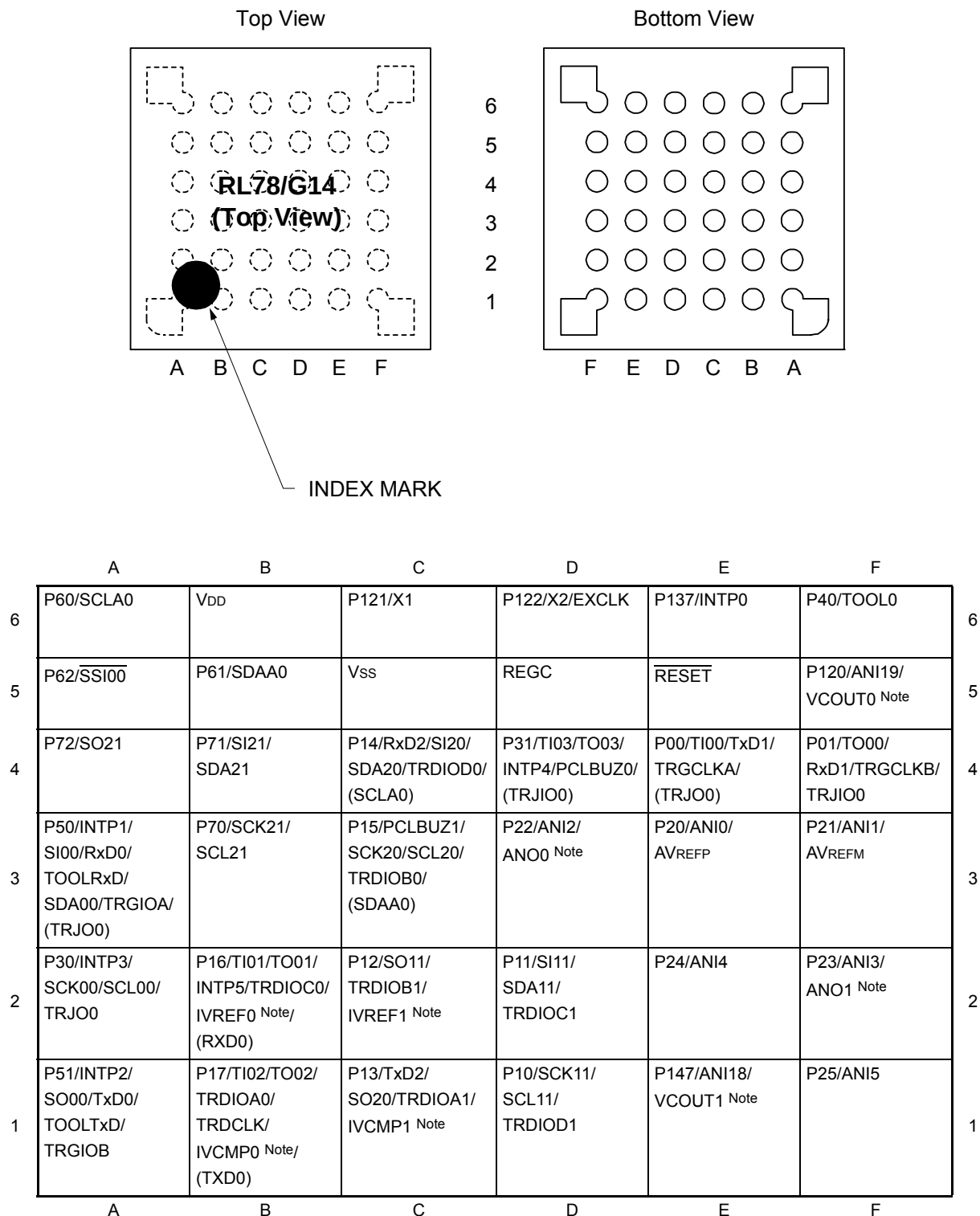
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



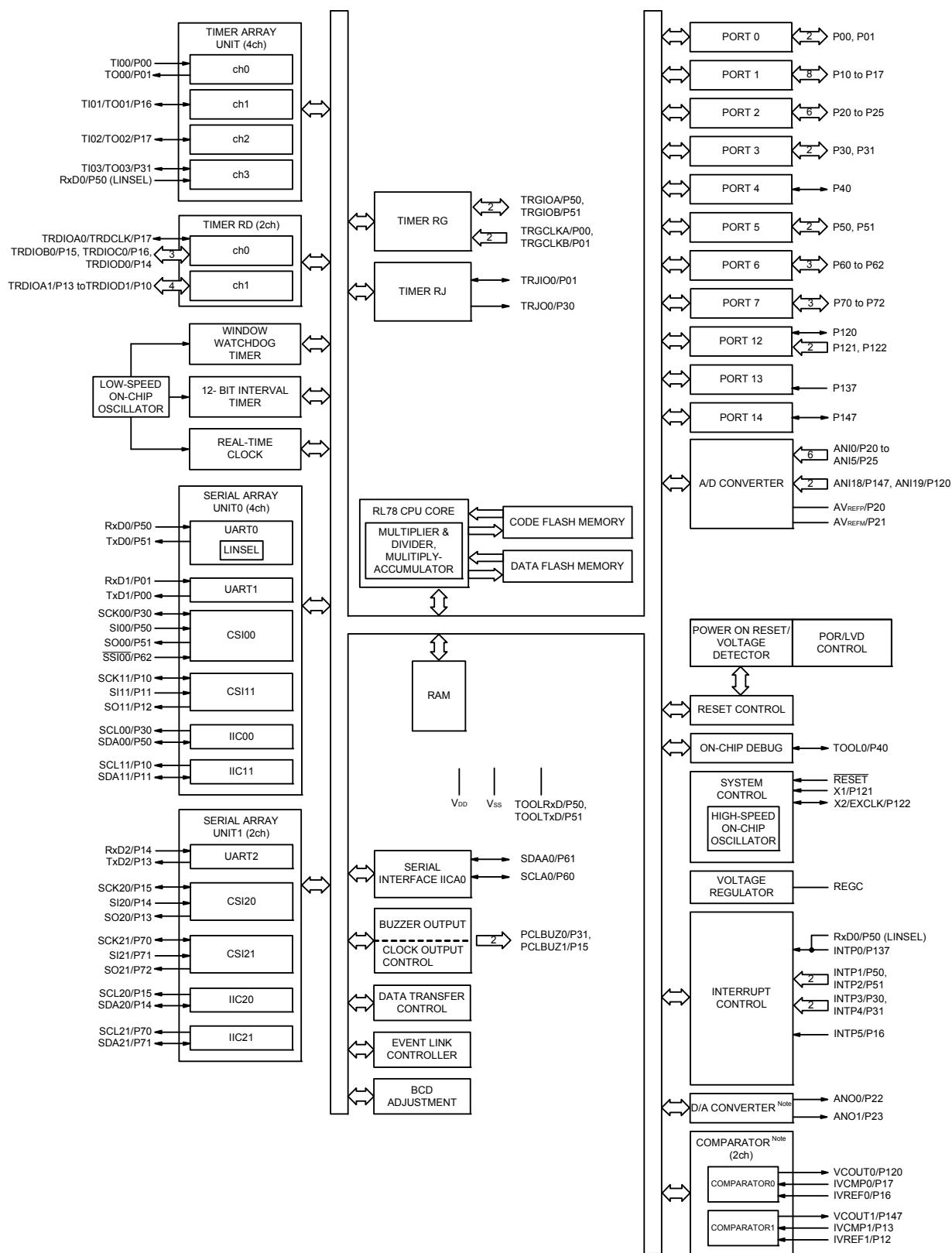
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.3 36-pin products



Note Mounted on the 96 KB or more code flash memory products.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7		mA
						VDD = 3.0 V		5.1	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	6.9		
						VDD = 3.0 V		4.0	6.9		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3		
						VDD = 3.0 V		3.8	6.3		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6		
						VDD = 3.0 V		2.8	4.6		
			LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0		mA
						VDD = 2.0 V		1.3	2.0		
			LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8		mA
						VDD = 2.0 V		1.3	1.8		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3		mA
						Resonator connection		3.4	5.5		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.3		
						Resonator connection		3.4	5.5		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
			LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9		mA
						Resonator connection		1.2	2.0		
				fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9		
						Resonator connection		1.2	2.0		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)

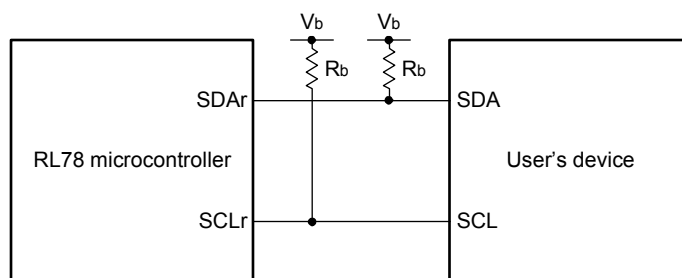
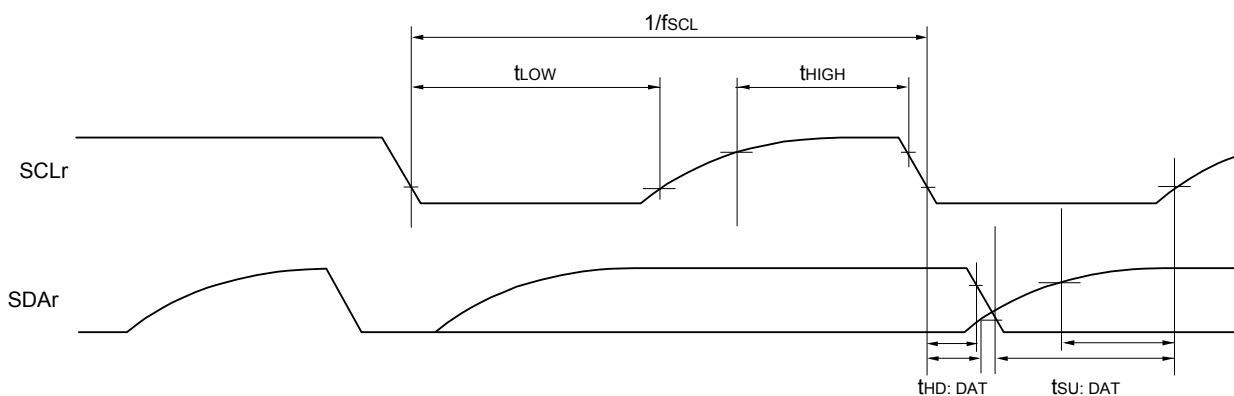
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		t _{KCY1} /2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		t _{KCY1} /2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		t _{KCY1} /2 - 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns

Note Use it with EVDD0 ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r : IIC number ($r = 00, 01, 10, 11, 20, 30, 31$), g : PIM, POM number ($g = 0, 1, 3$ to $5, 14$)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS mn bit of serial mode register mn (SMR mn). m : Unit number ($m = 0, 1$),
 n : Channel number ($n = 0, 2$), $mn = 00, 01, 02, 10, 12, 13$)

(1) I²C standard mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) Note 2	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		0	3.45	0	3.45	μs
Setup time of stop condition	tsu: STO	2.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.0		4.0		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} \leq EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	±5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		±2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		±2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(2) Interrupt & Reset Mode**(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVDA0	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	VLVDA1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	VLVDB1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	VLVDC1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDC3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.7 Power supply voltage rising slope characteristics**(TA = -40 to +85°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

Operation of products rated “G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

Parameter	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$: $\pm 1.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\%$ @ $T_A = -40$ to -20°C $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$: $\pm 5.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\%$ @ $T_A = -40$ to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$: $\pm 2.0\%$ @ $T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\%$ @ $T_A = -40$ to -20°C
Serial array unit	UART CSI: $f_{CLK}/2$ (16 Mbps supported), $f_{CLK}/4$ Simplified I ² C communication	UART CSI: $f_{CLK}/4$ Simplified I ² C communication
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fast mode
Voltage detector	- Rising: 1.67 V to 4.06 V (14 stages) - Falling: 1.63 V to 3.98 V (14 stages)	- Rising: 2.61 V to 4.06 V (8 stages) - Falling: 2.55 V to 3.98 V (8 stages)

Remark The electrical characteristics of products rated “G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to 3.1 to 3.10.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			80.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA		EVDD0 - 0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA		EVDD0 - 0.6	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA		EVDD0 - 0.5	V
	VOH2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA		VDD - 0.5	V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
	VOL2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operat- ing mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4			mA
						VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1			
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	9.3		mA
						VDD = 3.0 V		5.1	9.3		
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.7		
						VDD = 3.0 V		4.8	8.7		
				fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	7.3		
						VDD = 3.0 V		4.0	7.3		
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.7		
						VDD = 3.0 V		3.8	6.7		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.9		
						VDD = 3.0 V		2.8	4.9		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.7		mA
						Resonator connection		3.4	5.8		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.7		
						Resonator connection		3.4	5.8		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.4		
						Resonator connection		2.1	3.5		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.4		
						Resonator connection		2.1	3.5		
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1		μA
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1		
						Resonator connection		4.7	6.1		
				fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7		
						Resonator connection		4.8	6.7		
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5		
						Resonator connection		4.8	7.5		
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9		
						Resonator connection		5.4	8.9		
				fSUB = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		7.2	21.0		
						Resonator connection		7.3	21.1		

(Notes and Remarks are listed on the next page.)

(4) Peripheral Functions (Common to all products)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	$f_{\text{IL}} = 15\text{ kHz}$			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = \text{VDD} = 5.0\text{ V}$		1.3	1.7	mA
			Low voltage mode, $\text{AV}_{\text{REFP}} = \text{VDD} = 3.0\text{ V}$		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
D/A converter operating current	I_{DAC} Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	I_{CMP} Notes 1, 12, 13	$\text{VDD} = 5.0\text{ V}$, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		$\text{VDD} = 5.0\text{ V}$, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, $\text{AV}_{\text{REFP}} = \text{VDD} = 3.0\text{ V}$		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to VDD .**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	tsik1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	tkS11	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/ EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

3.6.4 Comparator

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		$\text{EVDD0} - 1.4$	V
	Ivcmp		-0.3		$\text{EVDD0} + 0.3$	V
Output delay	td	$\text{VDD} = 3.0\text{ V}$ Input slew rate $> 50\text{ mV}/\mu\text{s}$ Comparator high-speed mode, standard mode			1.2	μs
		Comparator high-speed mode, window mode			2.0	μs
		Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode		0.76 VDD		V
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode		0.24 VDD		V
Operation stabilization wait time	tcMP		100			μs
Internal reference voltage Note	VBGR	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.50	V

Note Not usable in sub-clock operation or STOP mode.

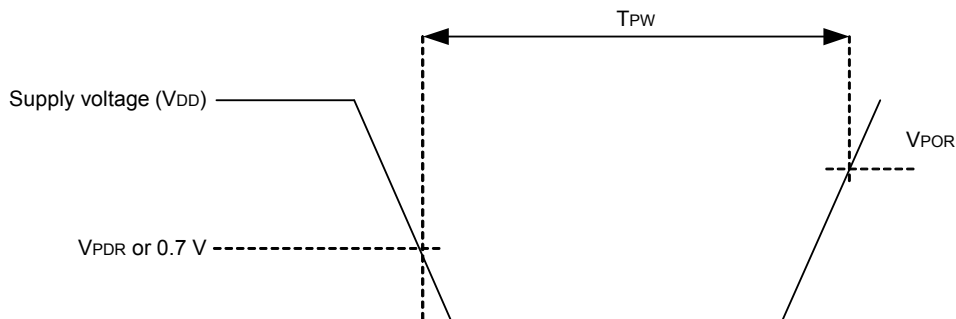
3.6.5 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $\text{VSS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.45	1.51	1.57	V
	VPDR	Voltage threshold on VDD falling Note 1	1.44	1.50	1.56	V
Minimum pulse width Note 2	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

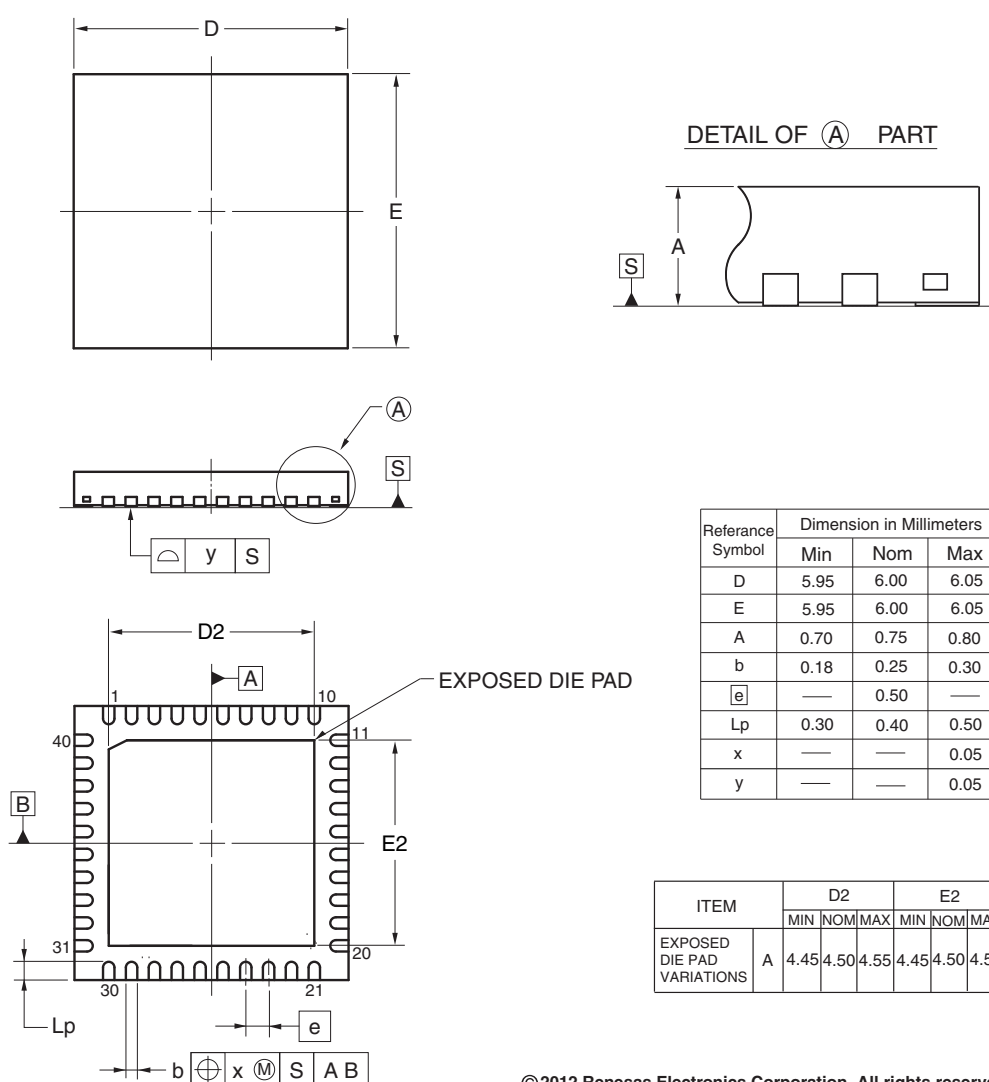
Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR . This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.4 40-pin products

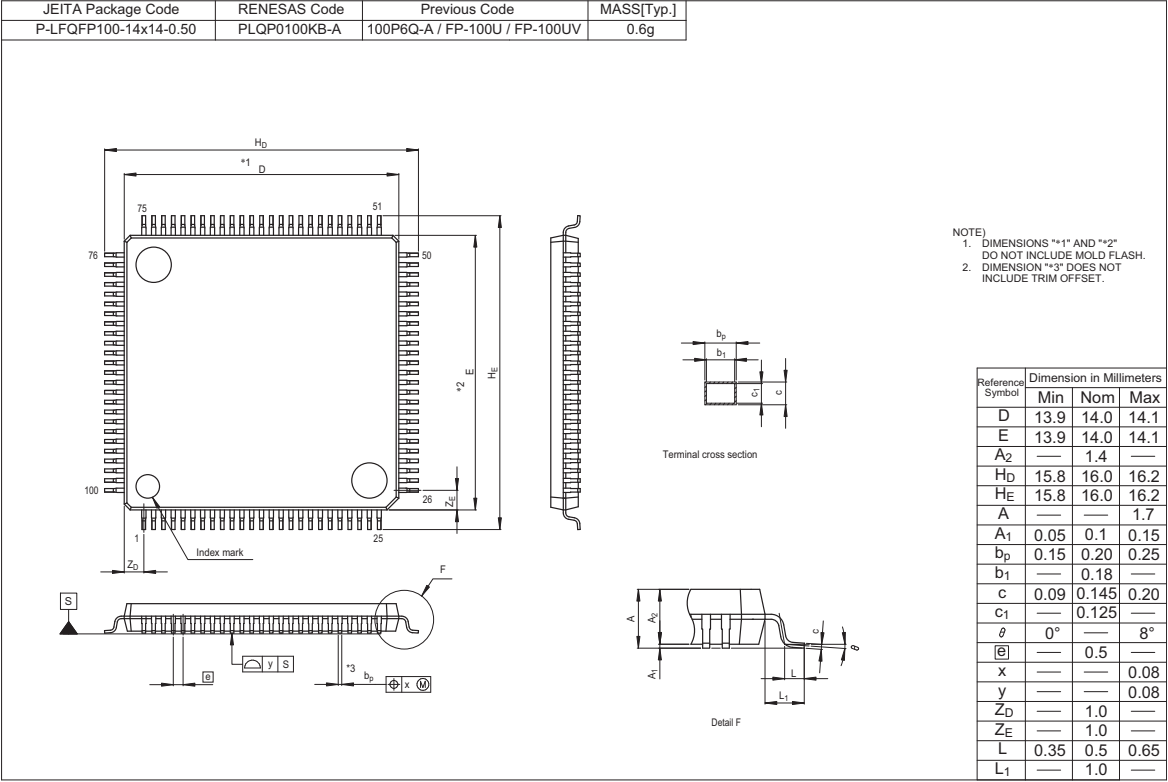
R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA,
 R5F104EHANA
 R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA,
 R5F104EHDNA
 R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA,
 R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



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R5F104PKAFB, R5F104PLAFB
R5F104PKGFB, R5F104PLGFB



NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.