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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104llafb-30

(4/5)

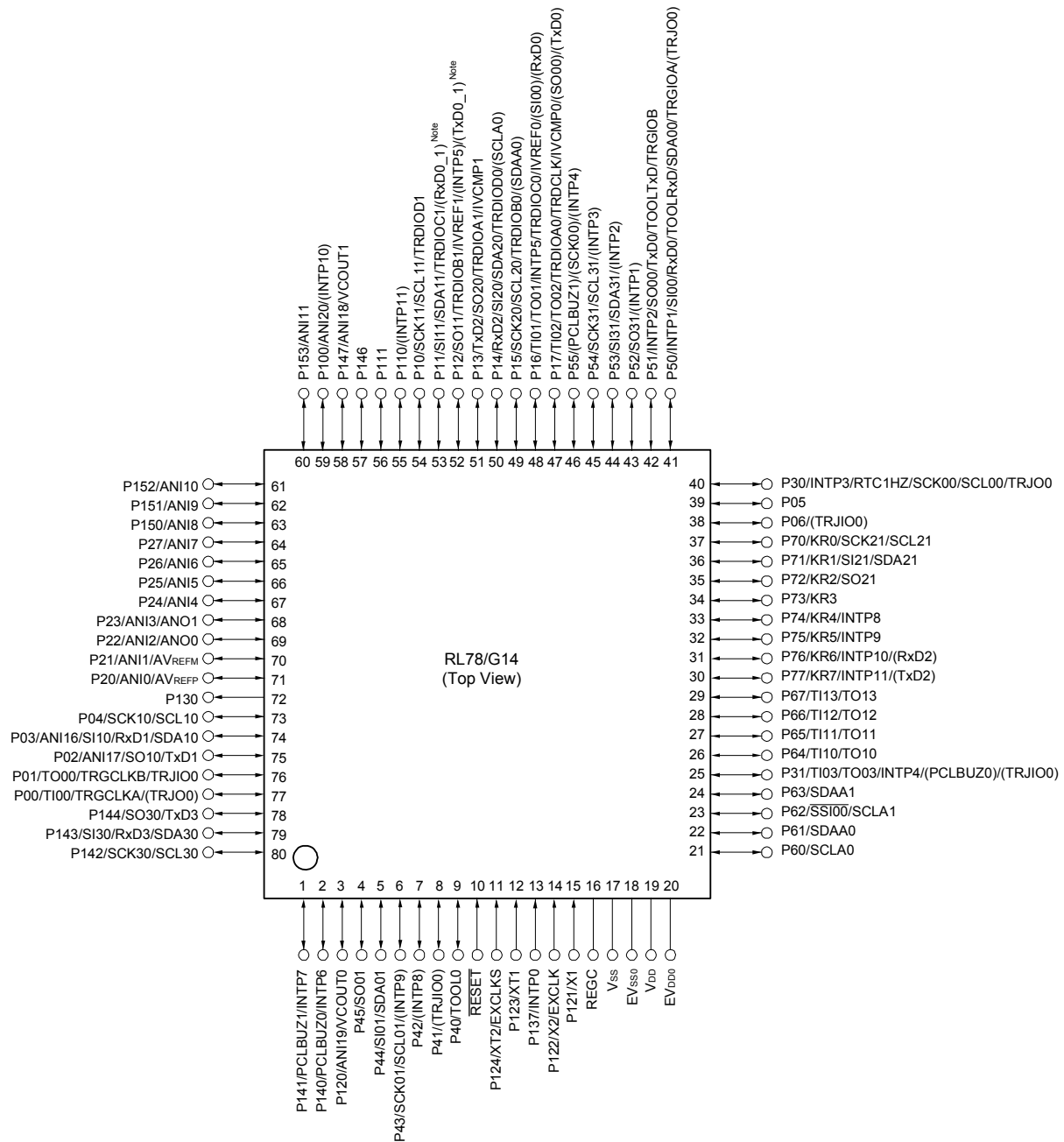
Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAF#V0, R5F104LHAF#V0, R5F104LJAF#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAF#X0, R5F104LHAF#X0, R5F104LJAF#X0 R5F104LKAFA#30, R5F104LLAFA#30 R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LDFDA#V0, R5F104LGDF#V0, R5F104LHDF#V0, R5F104LJDF#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LDFDA#X0, R5F104LGDF#X0, R5F104LHDF#X0, R5F104LJDF#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LDFDB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LDFDB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0 R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0 R5F104LKALA#U0, R5F104LLALA#U0 R5F104LKALA#W0, R5F104LLALA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
D		R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LDFDP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LDFDP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0	
G		R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0	

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

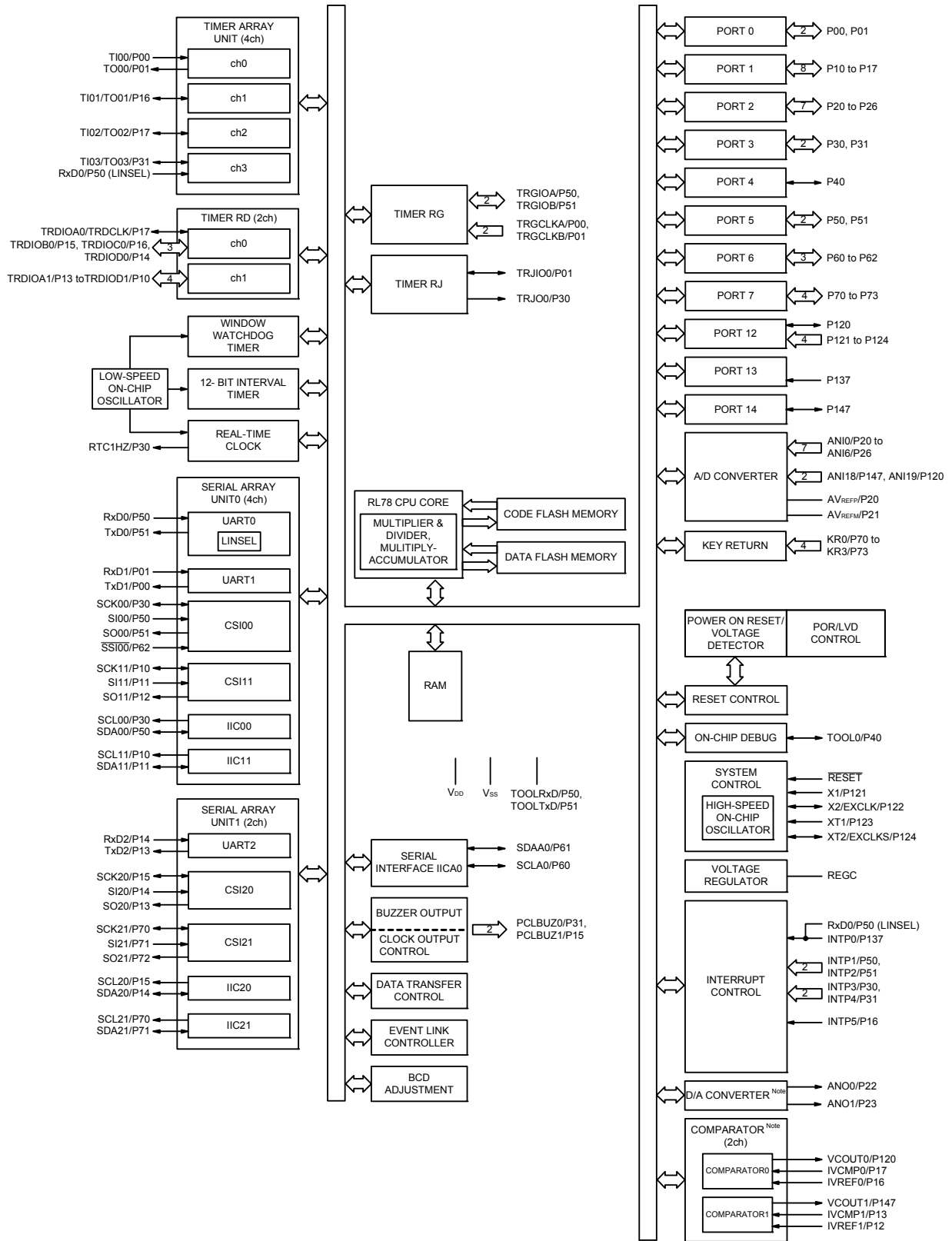
Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.4 40-pin products



Note Mounted on the 96 KB or more code flash memory products.

[80-pin, 100-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256
Data flash memory (KB)		8	8
RAM (KB)		12 to 24 Note	12 to 24 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
General-purpose register		8 bits \times 32 registers (8 bits \times 8 registers \times 4 banks)	
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits \times 8 bits, 16 bits \times 16 bits), Division (16 bits \div 16 bits, 32 bits \div 32 bits) • Multiplication and Accumulation (16 bits \times 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	

Note In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low ^{Note 1}	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 Note 2	mA	
					15.0 Note 2	mA	
			Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0	mA
				2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
		1.8 V ≤ EVDD0 < 2.7 V			9.0	mA	
		1.6 V ≤ EVDD0 < 1.8 V			4.5	mA	
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0	mA	
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA	
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA	
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA	
	Total of all pins (When duty ≤ 70% ^{Note 3})			150.0	mA		
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA	
			Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V	2.4		mA
				VDD = 3.0 V		2.4			
				fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V	2.1		mA
			VDD = 3.0 V	2.1					
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V	5.1	8.7	mA
				VDD = 3.0 V		5.1	8.7		
		fHOCO = 32 MHz, fIH = 32 MHz Note 3		Normal operation	VDD = 5.0 V	4.8	8.1	mA	
		VDD = 3.0 V			4.8	8.1			
		fHOCO = 48 MHz, fIH = 24 MHz Note 3		Normal operation	VDD = 5.0 V	4.0	6.9	mA	
		VDD = 3.0 V			4.0	6.9			
		fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V	3.8	6.3	mA		
		VDD = 3.0 V		3.8	6.3				
		fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V	2.8	4.6	mA		
		VDD = 3.0 V		2.8	4.6				
		LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V	1.3	2.0	mA	
			VDD = 2.0 V		1.3	2.0			
		LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V	1.3	1.8	mA	
			VDD = 2.0 V		1.3	1.8			
		HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input	3.3	5.3	mA	
					Resonator connection	3.4	5.5		
			fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input	3.3	5.3	mA	
					Resonator connection	3.4	5.5		
			fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input	2.0	3.1	mA	
					Resonator connection	2.1	3.2		
fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation		Square wave input	2.0	3.1	mA			
			Resonator connection	2.1	3.2				
LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input	1.2	1.9	mA			
			Resonator connection	1.2	2.0				
	fMX = 8 MHz Note 2, VDD = 2.0 V	Normal operation	Square wave input	1.2	1.9	mA			
			Resonator connection	1.2	2.0				
Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input	4.7	6.1	μA			
			Resonator connection	4.7	6.1				
	fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input	4.7	6.1	μA			
			Resonator connection	4.7	6.1				
	fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input	4.8	6.7	μA			
			Resonator connection	4.8	6.7				
	fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input	4.8	7.5	μA			
			Resonator connection	4.8	7.5				
	fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input	5.4	8.9	μA			
			Resonator connection	5.4	8.9				

(Notes and Remarks are listed on the next page.)

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

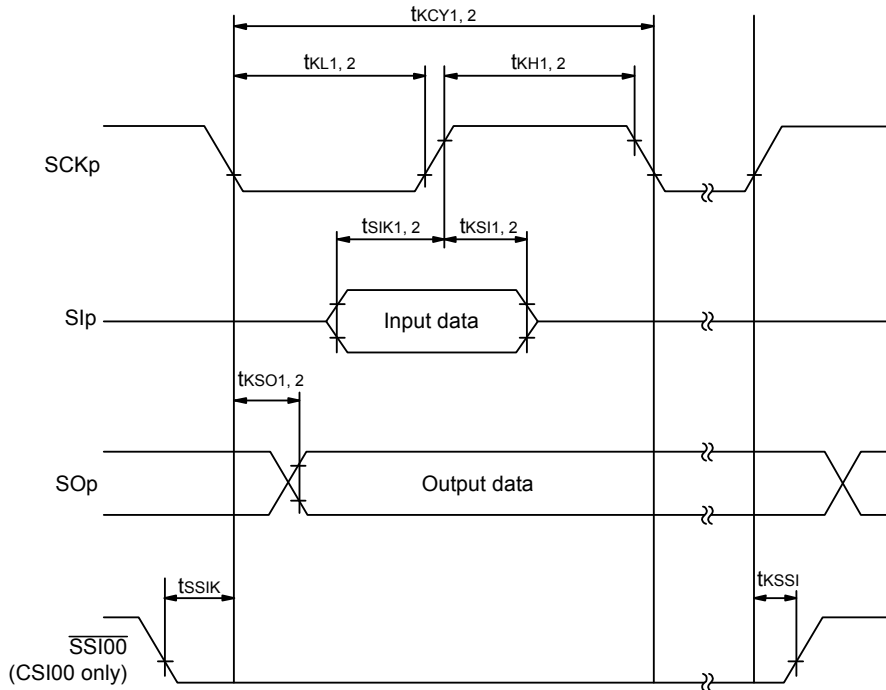
(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.9		mA		
						V _{DD} = 3.0 V		2.9				
					f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.5			
							V _{DD} = 3.0 V		2.5			
					HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		6.0	11.2	mA
								V _{DD} = 3.0 V		6.0	11.2	
						f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.5	10.6	
								V _{DD} = 3.0 V		5.5	10.6	
						f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.7	8.6	
								V _{DD} = 3.0 V		4.7	8.6	
						f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.4	8.2	
							V _{DD} = 3.0 V		4.4	8.2		
						f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.3	5.9	
							V _{DD} = 3.0 V		3.3	5.9		
					LS (low-speed main) mode Note 5	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.5	mA
									V _{DD} = 2.0 V		1.5	
					LV (low-voltage main) mode Note 5	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.1	mA
									V _{DD} = 2.0 V		1.5	
					HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA
								Resonator connection		3.9	7.0	
							Normal operation	Square wave input		3.7	6.8	
								Resonator connection		3.9	7.0	
						f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1	
								Resonator connection		2.3	4.2	
		Normal operation	Square wave input				2.3	4.1				
			Resonator connection				2.3	4.2				
		LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA			
					Resonator connection		1.4	2.5				
			Normal operation	Square wave input		1.4	2.4					
				Resonator connection		1.4	2.5					
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		5.2		μA			
					Resonator connection		5.2					
			f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		5.3	7.7				
					Resonator connection		5.3	7.7				
			f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.5	10.6				
					Resonator connection		5.5	10.6				
		f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.9	13.2					
				Resonator connection		6.0	13.2					
		f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.8	17.5					
				Resonator connection		6.9	17.5					

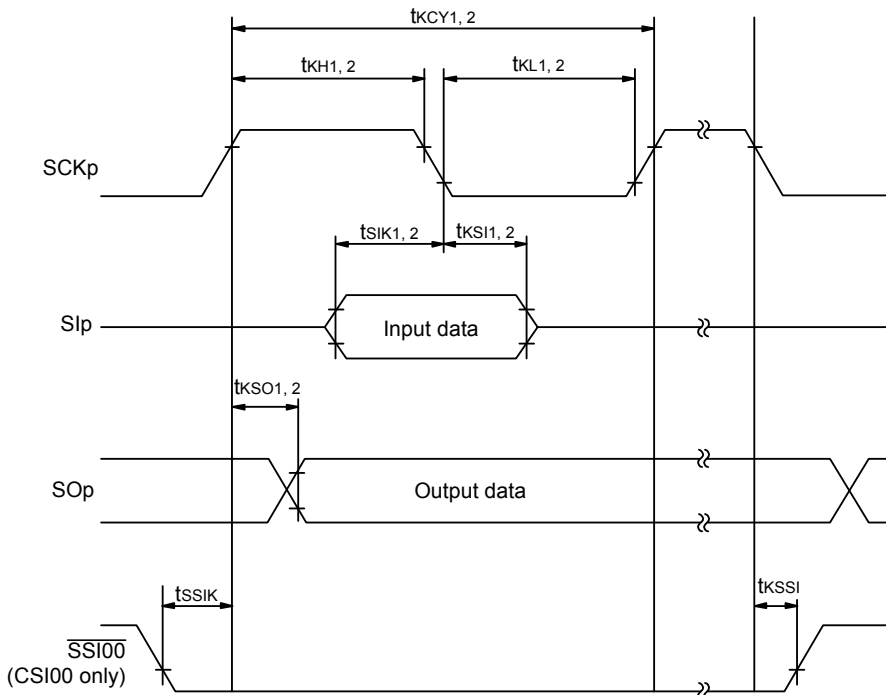
(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz |
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	200		1150		1150		ns
			300		1150		1150		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 7		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 10		tkCY1/2 - 50		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp out- put Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(2) Interrupt & Reset Mode**(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Voltage detection threshold	VLVDA0	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	VLVDA1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	VLVDB1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
VLVDB3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V	
		Falling interrupt voltage	3.00	3.06	3.12	V	
VLVDC0	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V		
VLVDC1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V	
		Falling interrupt voltage	2.50	2.55	2.60	V	
VLVDC2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V	
		Falling interrupt voltage	2.60	2.65	2.70	V	
VLVDC3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V	
		Falling interrupt voltage	3.60	3.67	3.74	V	
VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V		
VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	
VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V	
		Falling interrupt voltage	3.90	3.98	4.06	V	

2.6.7 Power supply voltage rising slope characteristics**(TA = -40 to +85°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A = +85$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G14 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$).

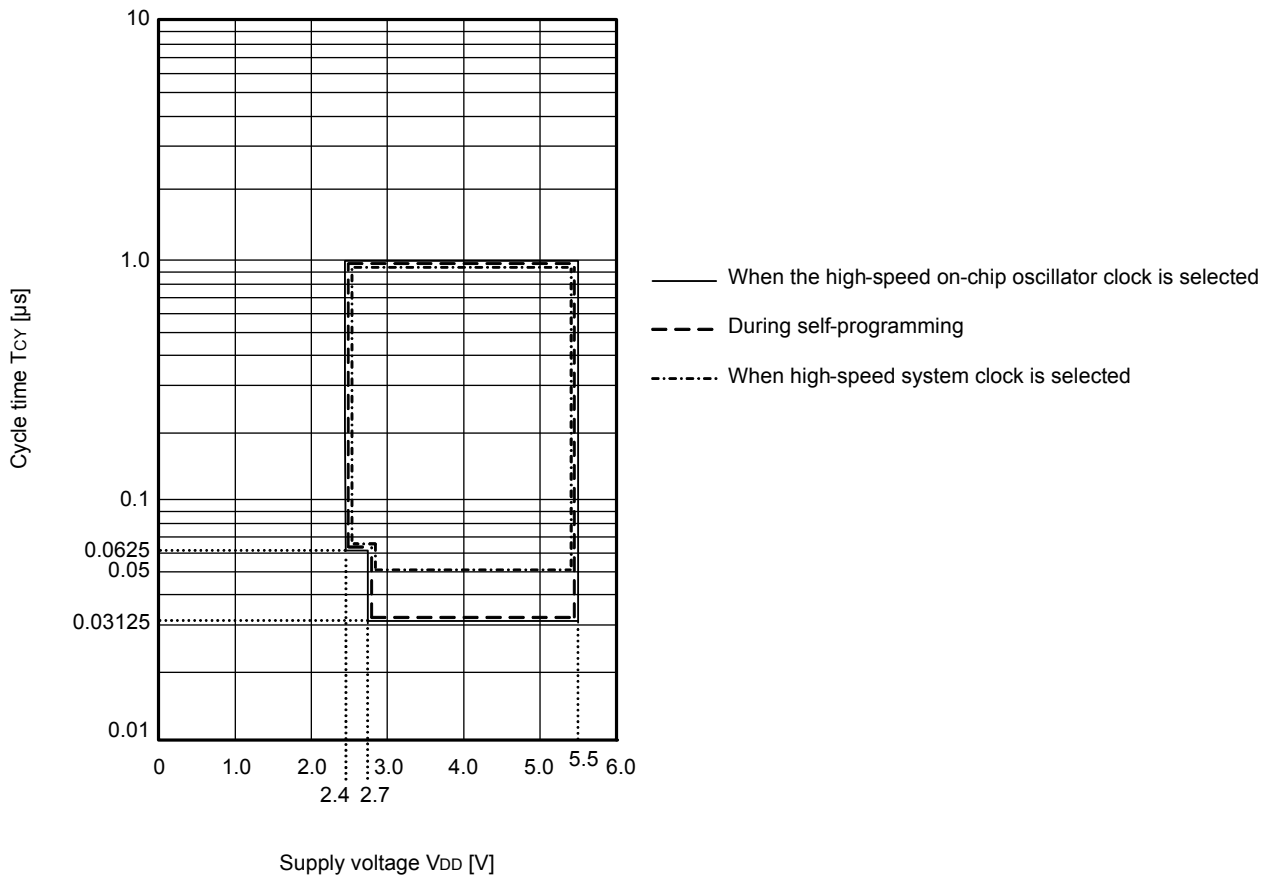
(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

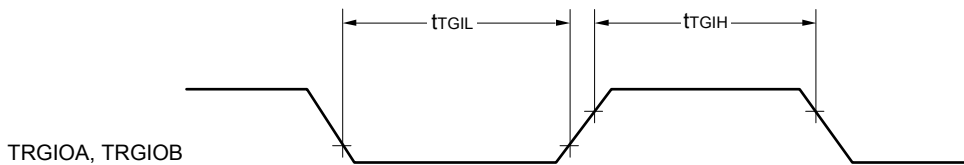
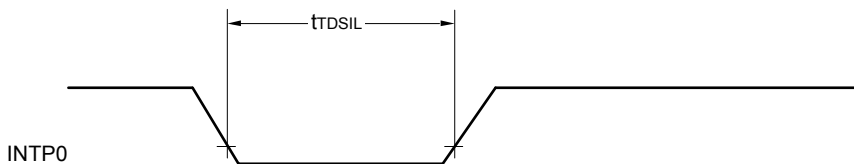
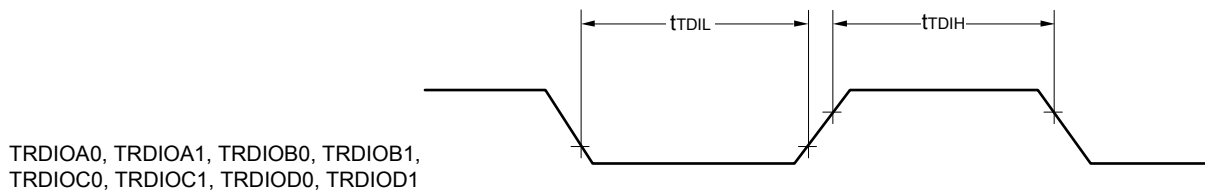
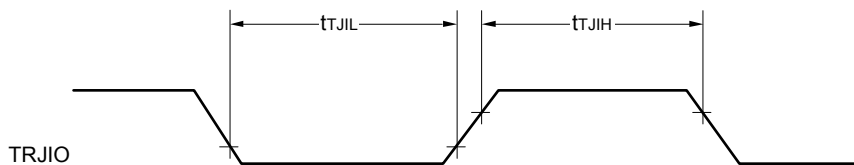
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.6		mA	
				V _{DD} = 3.0 V		2.6					
			f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3				
			V _{DD} = 3.0 V		2.3						
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.4	10.9		mA
				V _{DD} = 3.0 V		5.4	10.9				
		f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3		Normal operation	V _{DD} = 5.0 V		5.0	10.3			
		V _{DD} = 3.0 V			5.0	10.3					
		f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.2	8.2			
		V _{DD} = 3.0 V		4.2	8.2						
		f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.0	7.8	mA			
		V _{DD} = 3.0 V		4.0	7.8						
		f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	5.6	mA			
		V _{DD} = 3.0 V		3.0	5.6						
		HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	6.6	mA		
			Resonator connection		3.6	6.7					
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.4		6.6	
			Resonator connection		3.6	6.7					
		f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V		Normal operation	Square wave input		2.1	3.9	mA		
		Resonator connection		2.2	4.0						
			f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.9		mA	
Resonator connection		2.2	4.0								
	Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		4.9	7.1	μA			
Resonator connection			4.9	7.1							
		f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.9	7.1				
Resonator connection			4.9	7.1							
		f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		5.1	8.8				
Resonator connection			5.1	8.8							
	f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		5.5	10.5	μA				
Resonator connection		5.5	10.5								
	f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		6.5	14.5	μA				
Resonator connection		6.5	14.5								
	f _{SUB} = 32.768 kHz Note 4 T _A = +105°C	Normal operation	Square wave input		13.0	58.0	μA				
Resonator connection		13.0	58.0								

(Notes and Remarks are listed on the next page.)

Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)





(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	4600		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	4600		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	620		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	500		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	2700		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	2400		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ	1830		ns

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Resolution	RES			8		10	bit	
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB	
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs	
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs	
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs	
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs	
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs	
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs	
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR	
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR	
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB	
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB	
Analog input voltage	V _{AIN}	ANI0 to ANI14		0		V _{DD}	V	
		ANI16 to ANI20		0		EV _{DD0}	V	
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} Note 3				V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} Note 3				V

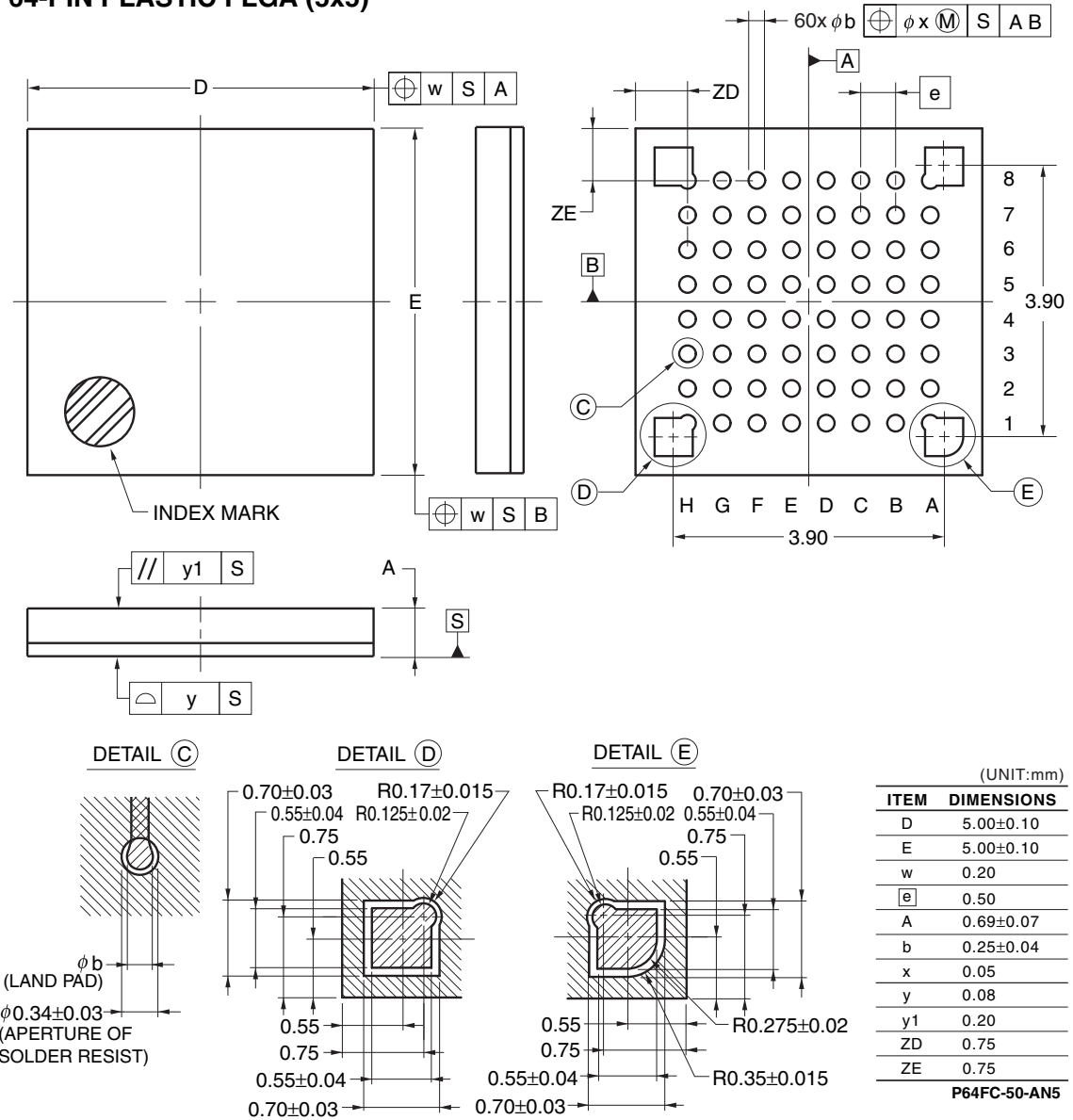
Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
 R5F104LKALA, R5F104LLALA
 R5F104LCGLA, R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
 R5F104LKGLA, R5F104LLGLA

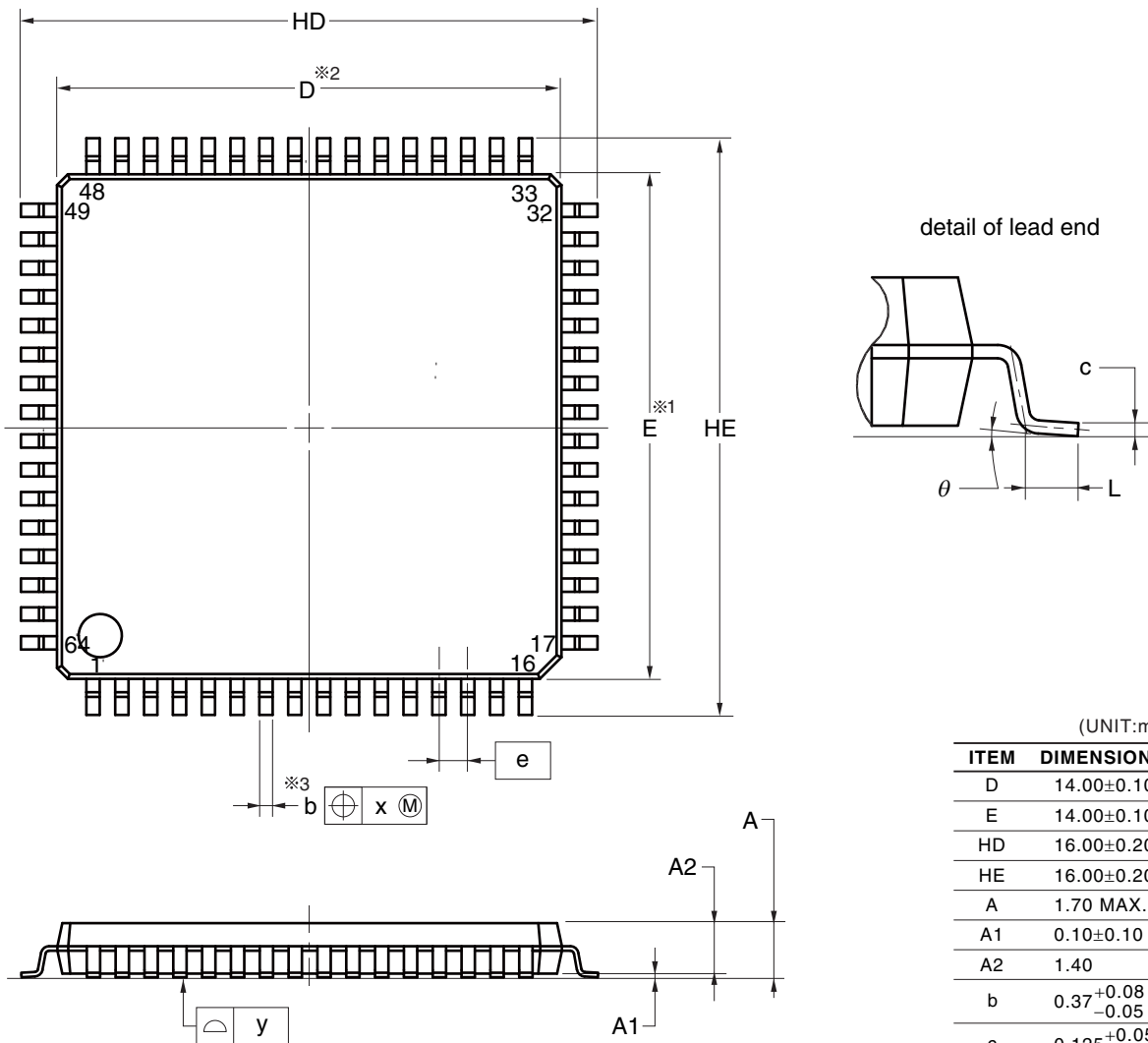
64-PIN PLASTIC FLGA (5x5)



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R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
 R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
 R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7



NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

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