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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104mgdfb-50

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0,
	(7.62 mm (300), 0.65 mm pitch)		R5F104AFASP#V0, R5F104AGASP#V0
			R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AEASP#X0, R5F104ACASP#X0
		D	
		D	R5F104AFDSP#V0, R5F104AGDSP#V0
			R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0,
			R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0
			R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 $\times$ 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0
			R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0,
			R5F104BFDNA#U0, R5F104BGDNA#U0
			R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0,
		G	RSF104BFDINA#W0, RSF104BGDINA#W0
		0	R5F104BFGNA#U0, R5F104BGGNA#U0
			R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP $(7 \times 7, 0.8 \text{ mm pitch})$	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0
			R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BEAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BEDFP#V0, R5F104BGDFP#V0
			R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BEDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0
			R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 $\times$ 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0
			R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0
			R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



## RL78/G14

## 1.3.5 44-pin products

• 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1  $\mu\text{F}).$ 

- Remark 1. For pin identification, see 1.4 Pin Identification.
- **Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).



Note	The flash library uses RAM in self-programming and rewriting of the data flash memory.
	The target products and start address of the RAM areas used by the flash library are shown below.
	R5F104xD (x = A to C, E to G, J, L): Start address FE900H
	R5F104xE (x = A to C, E to G, J, L): Start address FE900H
	For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family
	(R20UT2944).



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		48-pin	64-pin		
Item		R5F104Gx	R5F104Lx		
		(x = K, L)	(x = K, L)		
Clock output/buzzer outp	ut	2	2		
		<ul> <li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation)</li> <li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fsuB = 32.768 kHz operation)</li> </ul>			
8/10-bit resolution A/D co	nverter	10 channels	12 channels		
D/A converter		2 channels			
Comparator		2 channels			
Serial interface		<ul> <li>[48-pin products]</li> <li>CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>CSI: 1 channel/UART: 1 channel/simplified I<sup>2</sup>C: 1 channel</li> <li>CSI: 2 channels/UART: 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>[64-pin products]</li> <li>CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>CSI: 2 channels/UART: 1 channel/simplified I<sup>2</sup>C: 2 channels</li> <li>CSI: 2 channels/UART: 1 channel/simplified I<sup>2</sup>C: 2 channels</li> </ul>			
	I <sup>2</sup> C bus	1 channel	1 channel		
Data transfer controller (DTC)		32 sources	33 sources		
Event link controller (ELC	;)	Event input: 22 Event trigger output: 9			
Vectored interrupt	Internal	24	24		
sources	External	10	13		
Key interrupt		6	8		
Reset		Reset by RESET pin     Internal reset by watchdog timer     Internal reset by power-on-reset     Internal reset by voltage detector     Internal reset by illegal instruction execution <sup>Note</sup> Internal reset by RAM parity error     Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: $1.51 \pm 0.04 \text{ V} (\text{TA} = -40 \text{ to } +85^{\circ}\text{C})$ $1.51 \pm 0.06 \text{ V} (\text{TA} = -40 \text{ to } +105^{\circ}\text{C})$ • Power-down-reset: $1.50 \pm 0.04 \text{ V} (\text{TA} = -40 \text{ to } +85^{\circ}\text{C})$ $1.50 \pm 0.06 \text{ V} (\text{TA} = -40 \text{ to } +105^{\circ}\text{C})$			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)			
Operating ambient tempe	erature	TA = -40 to +85°C (A: Consumer applications, TA = -40 to +105°C (G: Industrial applications)	D: Industrial applications),		

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

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		80-pin	100-pin				
It	tem	R5F104Mx	R5F104Px				
		(x = F to H, J)	(x = F  to  H, J)				
Clock output/buzz	er output	2	2				
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.4	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz				
		(Main system clock: fмаin = 20 MHz operation	on)				
		• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.09	96 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz				
		(Subsystem clock: fs∪B = 32.768 kHz opera	tion)				
8/10-bit resolution	A/D converter	17 channels	20 channels				
D/A converter		2 channels	2 channels				
Comparator		2 channels	2 channels				
Serial interface		[80-pin, 100-pin products]					
		CSI: 2 channels/UART (UART supporting L	N-bus): 1 channel/simplified I <sup>2</sup> C: 2 channels				
		CSI: 2 channels/UART: 1 channel/simplified	I <sup>2</sup> C: 2 channels				
		CSI: 2 channels/UART: 1 channel/simplified	I <sup>2</sup> C: 2 channels				
		CSI: 2 channels/UART: 1 channel/simplified	I <sup>2</sup> C: 2 channels				
	I <sup>2</sup> C bus	2 channels	2 channels				
Data transfer controller (DTC)		39 sources	39 sources				
Event link controller (ELC)		Event input: 26					
		Event trigger output: 9					
Vectored inter-	Internal	32	32				
rupt sources	External	13	13				
Key interrupt		8 8					
Reset		Reset by RESET pin					
		<ul> <li>Internal reset by watchdog timer</li> </ul>					
		<ul> <li>Internal reset by power-on-reset</li> </ul>					
		<ul> <li>Internal reset by voltage detector</li> </ul>					
		Internal reset by illegal instruction execution	Note				
		<ul> <li>Internal reset by RAM parity error</li> </ul>	Internal reset by RAM parity error				
		Internal reset by illegal-memory access					
Power-on-reset ci	rcuit	• Power-on-reset: 1.51 ±0.04 V (T <sub>A</sub> = -40 to +85°C)					
		$1.51 \pm 0.06 \text{ V} (\text{TA} = -40 \text{ to } +105^{\circ}\text{C})$					
		• Power-down-reset: $1.50 \pm 0.04 \vee (T_{A} = -40)$	• Power-down-reset: $1.50 \pm 0.04 \text{ V}$ (TA = -40 to +85°C)				
Voltage detector		1.63 V to 4.06 V (14 stages)	$1.30 \text{ II.00 V (IA = -40 (0 + 105 \text{ C}))}$				
On-chip debug fu	nction	Provided					
Power supply yelt	200	$V_{DD} = 1.6 \text{ to } 5.5 \text{ V} (T_{A} = 40 \text{ to } \pm 85^{\circ} \text{ C})$					
	aye	$V_{DD} = 2.4 \text{ to } 5.5 \text{ V} (TA = -40 \text{ to } +0.5 \text{ C})$					
Operating ambien	it temperature	$T_{A} = -40$ to +85°C (A: Consumer applications	D: Industrial applications)				
		$T_A = -40$ to +105°C (G: Industrial applications	)				

Note

The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## 2.3.2 Supply current characteristics

## (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

Parameter	Symbol	Conditions							MAX.	Unit	
Supply	IDD1	DD1 Operat- HS (high-speed main ing mode mode Note 5	Operat-	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.4		mA
current			mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4			
NOLE I				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.1			
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1			
			HS (high-speed main)	fносо = 64 MHz,	Normal	VDD = 5.0 V		5.1	8.7	mA	
		mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		5.1	8.7			
				fносо = 32 MHz,	Normal	VDD = 5.0 V		4.8	8.1		
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		4.8	8.1		
				fносо = 48 MHz,	Normal	VDD = 5.0 V		4.0	6.9		
				fiH = 24 MHz Note 3	operation	VDD = 3.0 V		4.0	6.9		
				fносо = 24 MHz,	Normal	VDD = 5.0 V		3.8	6.3		
				fiH = 24 MHz Note 3	operation	VDD = 3.0 V		3.8	6.3		
				fносо = 16 MHz,	Normal	VDD = 5.0 V		2.8	4.6		
				fiH = 16 MHz Note 3	operation	VDD = 3.0 V		2.8	4.6		
		LS (low-speed main) 1 mode Note 5 LV (low-voltage main) 1 mode Note 5 HS (high-speed main) 1 mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz <sup>Note 3</sup>	Normal	VDD = 3.0 V		1.3	2.0	mA		
				operation	VDD = 2.0 V		1.3	2.0			
			fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8	mA		
					VDD = 2.0 V		1.3	1.8			
			f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA		
					Resonator connection		3.4	5.5			
				f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		3.3	5.3	-	
						Resonator connection		3.4	5.5		
			LS (low-speed main) mode Note 5	f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> ,	Normal	Square wave input		2.0	3.1		
				V <sub>DD</sub> = 5.0 V f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	operation Normal operation	Resonator connection		2.1	3.2		
						Square wave input		2.0	3.1		
						Resonator connection		2.1	3.2		
		l		f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA	
						Resonator connection		1.2	2.0		
				fmx = 8 MHz Note 2,	Normal operation	Square wave input		1.2	1.9		
				VDD = 2.0 V		Resonator connection		1.2	2.0		
			Subsystem clock	fsue = 32.768 kHz Note 4	Normal	Square wave input		4.7	6.1	μΑ	
			operation	TA = -40°C	operation	Resonator connection		4.7	6.1		
				fsue = 32.768 kHz Note 4	Normal	Square wave input		4.7	6.1		
			TA = +25°C	operation	Resonator connection		4.7	6.1			
				fsue = 32.768 kHz Note 4	Normal	Square wave input		4.8	6.7		
				TA = +50°C	operation	Resonator connection		4.8	6.7		
				fsue = 32.768 kHz Note 4	Normal	Square wave input		4.8	7.5		
				TA = +70°C	operation	Resonator connection		4.8	7.5		
				fsub = 32.768 kHz Note 4	Normal	Square wave input		5.4	8.9		
				T <sub>A</sub> = +85°C	operation	Resonator connection		5.4	8.9		

(Notes and Remarks are listed on the next page.)

- Note 1. Total current flowing into VDD, EVDDD, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDD, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
   Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3. When high-speed system clock and subsystem clock are stopped.
- **Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}_{\text{@1}} \text{ MHz to } 32 \text{ MHz}$ 

2.4 V  $\leq$  VDD  $\leq$  5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode:  $$1.8~V \le V \mbox{DD} \le 5.5~V \ensuremath{\textcircled{0}}1~\mbox{MHz}$ to 8 MHz}$$ 

LV (low-voltage main) mode:  $1.6 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$  to 4 MHz

- Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHoco: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remark 3.** fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsuB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C



- Note 1. Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
   Note 2. During HALT instruction execution by flash memory.
- **Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 4.** When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
  - HS (high-speed main) mode:  $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$  to 32 MHz
    - 2.4 V  $\leq$  VDD  $\leq$  5.5 V@1 MHz to 16 MHz
  - LS (low-speed main) mode:  $1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$  to 8 MHz
  - LV (low-voltage main) mode:  $1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}_{\textcircled{O}}1 \text{ MHz}$  to 4 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remark 3.** file: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remark 4.** fsuB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C





CSI mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





- Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

## (2) I<sup>2</sup>C fast mode

## (TA = -40 to +85°C, 1.6 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (hig main)	h-speed mode	LS (lov main)	/-speed mode	LV (low main)	-voltage mode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsc∟	Fast mode:	$2.7~V \leq EV_{DD0} \leq 5.5~V$	0	400	0	400	0	400	kHz
		fc∟k ≥ 3.5 MHz	$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$	0	400	0	400	0	400	kHz
Setup time of restart condi-	tsu: STA	$2.7~V \leq EV_{DD0} \leq$	5.5 V	0.6		0.6		0.6		μs
tion		$1.8 \text{ V} \leq EV_{DD0} \leq$	5.5 V	0.6		0.6		0.6		μs
Hold time Note 1	thd: STA	$2.7~V \leq EV_{DD0} \leq$	5.5 V	0.6		0.6		0.6		μs
		$1.8 \text{ V} \leq EV_{DD0} \leq$	$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			0.6		0.6		μs
Hold time when SCLA0 = "L"	t∟ow	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		1.3		1.3		1.3		μs
		$1.8 \text{ V} \leq EV_{DD0} \leq$	$1.8 \text{ V} \leq EV_{DD0} \leq 5.5 \text{ V}$			1.3		1.3		μs
Hold time when SCLA0 = "H"	tніgн	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		0.6		0.6		0.6		μs
1.8 V ≤		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$		0.6		0.6		0.6		μs
Data setup time (reception)	tsu: dat	$2.7~V \leq EV_{DD0} \leq$	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			100		100		ns
		$1.8~V \leq EV_{DD0} \leq$	5.5 V	100		100		100		ns
Data hold time (transmission)	thd: dat	$2.7~V \leq EV_{DD0} \leq$	5.5 V	0	0.9	0	0.9	0	0.9	μs
Note 2		$1.8 \text{ V} \leq EV_{\text{DD0}} \leq$	5.5 V	0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	tsu: sto	$2.7~V \leq EV_{\text{DD0}} \leq$	5.5 V	0.6		0.6		0.6		μs
		$1.8 \text{ V} \leq EV_{DD0} \leq$	$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$			0.6		0.6		μs
Bus-free time	tвuғ	$2.7 \text{ V} \leq EV_{DD0} \leq$	5.5 V	1.3		1.3		1.3		μs
	$1.8 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		1.3		1.3		1.3		μs	

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of the DEAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

- Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.
- **Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode:  $C_b$  = 320 pF,  $R_b$  = 1.1 k $\Omega$ 



## 2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C	, 1.8 V $\leq$ EVDD0 =	$EVDD1 \leq VDD \leq 5.5 V$	, $Vss = EVsso = EVss1 = 0 V$ )
--------------------	------------------------	-----------------------------	---------------------------------

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuinit	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	thd	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** tsuinit. The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

 $\ensuremath{\text{tHD:}}$   $\ensuremath{\text{How}}$  long to keep the TOOL0 pin at the low level from when the external resets end

(excluding the processing time of the firmware to control the flash memory)



# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C)

This chapter describes the following electrical specifications. Target products G: Industrial applications  $T_A = -40$  to  $+105^{\circ}C$ R5F104xxGxx

- Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.
- Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.
- Caution 4. Please contact Renesas Electronics sales office for derating of operation under TA = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
- Remark When RL78/G14 is used in the range of T<sub>A</sub> = -40 to +85°C, see 2. ELECTRICAL SPECIFICATIONS (T<sub>A</sub> = -40 to +85°C).



$1A = -40 \ (0 + 103 \ 0, 2.4 \ 0 \le 2000 = 2000 \le 3.3 \ 0, 333 = 20330 = 20331 = 0 \ 0) $ (2)							
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147				8.5 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145(When duty $\leq$ 70% Note 3)Total of P05, P06, P10 to P17, P30, P31, P50 to P57,	$4.0~V \leq EV_{DD0} \leq 5.5~V$			40.0	mA
			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 4.0 \text{ V}$			15.0	mA
			$2.4~V \leq EV_{DD0} < 2.7~V$			9.0	mA
			$4.0~V \leq EV_{DD0} \leq 5.5~V$			40.0	mA
			$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} < 4.0 \text{ V}$			35.0	mA
	P80 to P P111, P (When of (When of	P80 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq$ 70% <sup>Note 3</sup> )	2.4 V ≤ EVDD0 < 2.7 V			20.0	mA
		Total of all pins (When duty $\leq$ 70% <sup>Note 3</sup> )				80.0	mA
	IOL2         Per pin for P20 to P27, P150 to P156				0.4 Note 2	mA	
		Total of all pins (When duty $\leq$ 70% <sup>Note 3</sup> )	$2.4 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$			5.0	mA

(TA = -40 to +105°C, 2.4 V  $\leq$  EVDD0 = EVDD1  $\leq$  VDD  $\leq$  5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVsso, EVss1, and Vss pins.

Note 2. Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor  $\leq$  70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IoL × 0.7)/(n × 0.01)
  - <Example> Where n = 80% and IoL = 10.0 mA

Total output current of pins =  $(10.0 \times 0.7)/(80 \times 0.01) \approx 8.7$  mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



- Note 1. Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or Vss, EVss0, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
   Note 2. During HALT instruction execution by flash memory.
- Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- **Note 4.** When high-speed system clock and subsystem clock are stopped.
- **Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.<br/>HS (high-speed main) mode:  $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}$ @1 MHz to 32 MHz
  - 2.4 V  $\leq$  VDD  $\leq$  5.5 V@1 MHz to 16 MHz
- Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- **Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



AC Timing Test Points



External System Clock Timing



TI/TO Timing







## (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode)

(TA = -40 to +105°C, 2	$2.4 V \leq EVDD0 = EVDD^{2}$	$1 \leq VDD \leq 5.5 V, VSS$	= EVss0 $=$ EVss1 $=$ 0 V)
(			

(1/2)

Parameter	Parameter Symbol Condit		HS (high-spe	ed main) mode	Unit	
			MIN.	MAX.		
SCLr clock frequency	fsc∟			400 Note 1	kHz	
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		400 Note 1	kHz	
		$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_{b} \leq 4.0 \; V, \\ C_{b} = 100 \; pF, \; R_{b} = 2.8 \; k\Omega \end{array}$		100 Note 1	kHz	
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		100 Note 1	kHz	
		$\label{eq:2.4} \begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$		100 Note 1	kHz	
Hold time when SCLr = "L"	tLOW		1200		ns	
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	1200		ns	
			4600		ns	
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	4600		ns	
		$\begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$	4650		ns	
Hold time when SCLr = "H"	tнigн		620		ns	
		$\begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	500		ns	
		$\begin{array}{l} 4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 100 \; pF, \; R_b = 2.8 \; k\Omega \end{array}$	2700		ns	
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$	2400		ns	
		$\label{eq:2.4} \begin{array}{l} 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V \leq V_b \leq 2.0 \; V, \\ C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{array}$	1830		ns	



## (2) When reference voltage (+) = AVREFP/ANIO (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$		1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution	$3.6 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	2.125		39	μs
		Target ANI pin: ANI16 to ANI20	$2.7~V \leq V_{DD} \leq 5.5~V$	3.1875		39	μs
			$2.4~V \leq V_{DD} \leq 5.5~V$	17		39	μs
Zero-scale error Notes 1, 2	Ezs	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$			±0.35	%FSR
Full-scale error Notes 1, 2	Efs	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EVDD0 ≤ AVREFP = VDD Notes 3, 4	$2.4 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			±2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI20		0		AVREFP and EVDD0	V

## (TA = -40 to +105°C, 2.4 V $\leq$ EVDD0 = EVDD1 $\leq$ VDD $\leq$ 5.5 V, 2.4 V $\leq$ AVREFP $\leq$ VDD $\leq$ 5.5 V, Vss = EVsso = EVss1 = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

#### Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When  $EVDD0 \le AVREFP \le VDD$ , the MAX. values are as follows.

	Overall error:	Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
	Zero-scale error/Full-scale error:	Add $\pm 0.05\%$ FSR to the MAX. value when AVREFP = VDD.
	Integral linearity error/ Differential linearity error:	Add ±0.5 LSB to the MAX. value when AVREFP = VDD.
Note 4.	When AVREFP < EVDD0 $\leq$ VDD, the MAX. values a	are as follows.
	Overall error:	Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error:

Add ±0.20%FSR to the MAX. value when AVREFP = VDD. Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.



## 4.2 32-pin products

R5F104BAANA, R5F104BCANA, R5F104BDANA, R5F104BEANA, R5F104BFANA, R5F104BGANA R5F104BADNA, R5F104BCDNA, R5F104BDDNA, R5F104BEDNA, R5F104BFDNA, R5F104BGDNA R5F104BAGNA, R5F104BCGNA, R5F104BDGNA, R5F104BEGNA, R5F104BFGNA, R5F104BGGNA











Referance	Dimension in Millimeters					
Symbol	Min	Nom	Max			
D	4.95	5.00	5.05			
E	4.95	5.00	5.05			
Α	0.70	0.75	0.80			
b	0.18	0.25	0.30			
е		0.50				
Lp	0.30	0.40	0.50			
x			0.05			
У			0.05			

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

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R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJAFA R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA R5F104MKAFA, R5F104MLAFA R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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### NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.