Renesas Electronics America Inc - R5F104MHAFB#V0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104mhafb-v0

(1/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0 R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0 R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0 R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0 R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0 R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0 R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0 R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BFDFP#V0, R5F104BGDFP#V0 R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BFDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0 R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0 R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0 R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

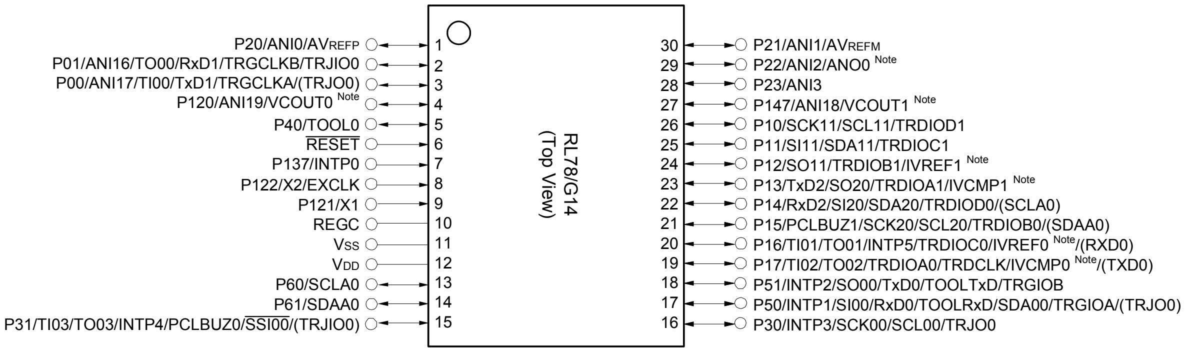
Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



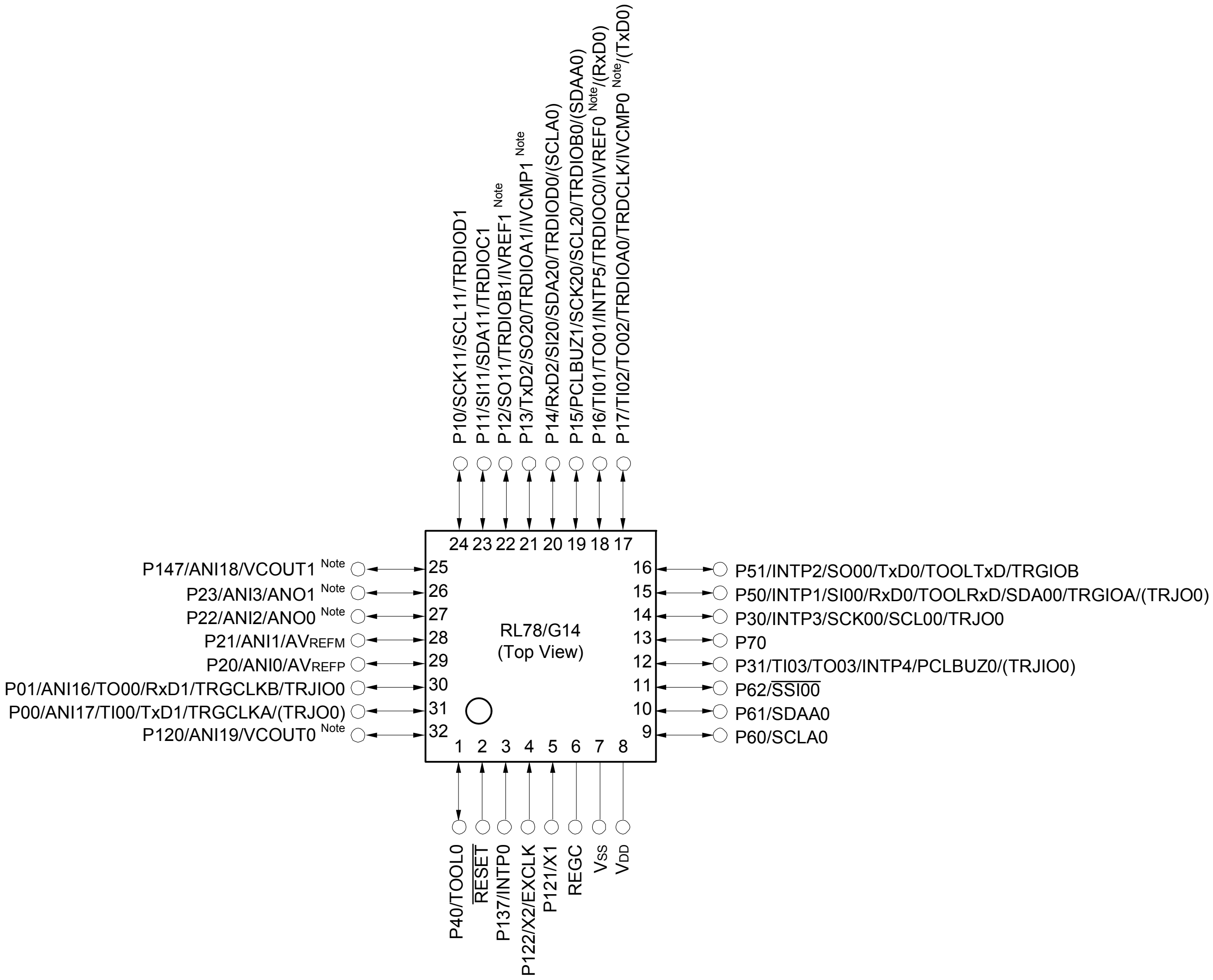
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



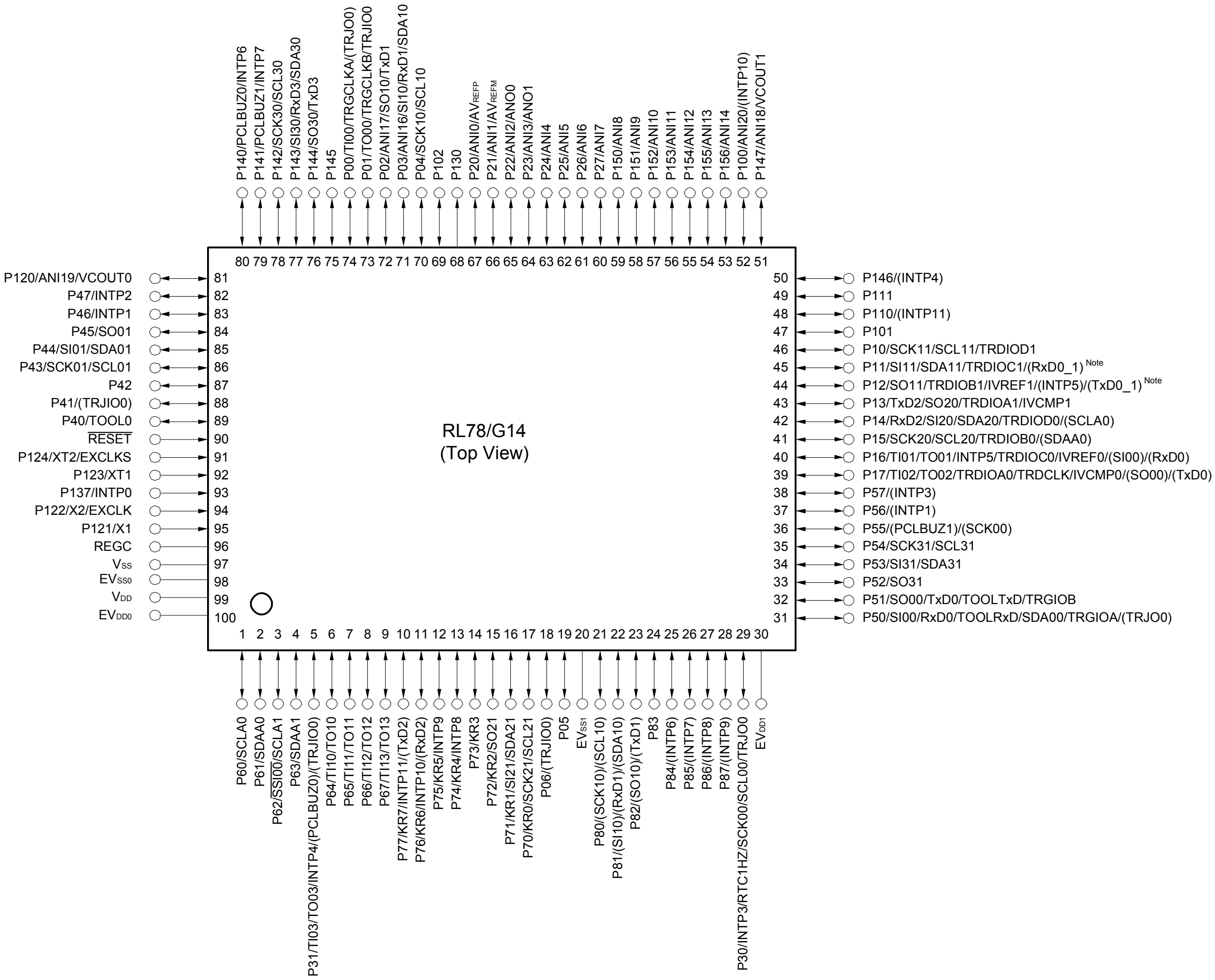
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins ($EV_{DD0} = EV_{DD1}$).

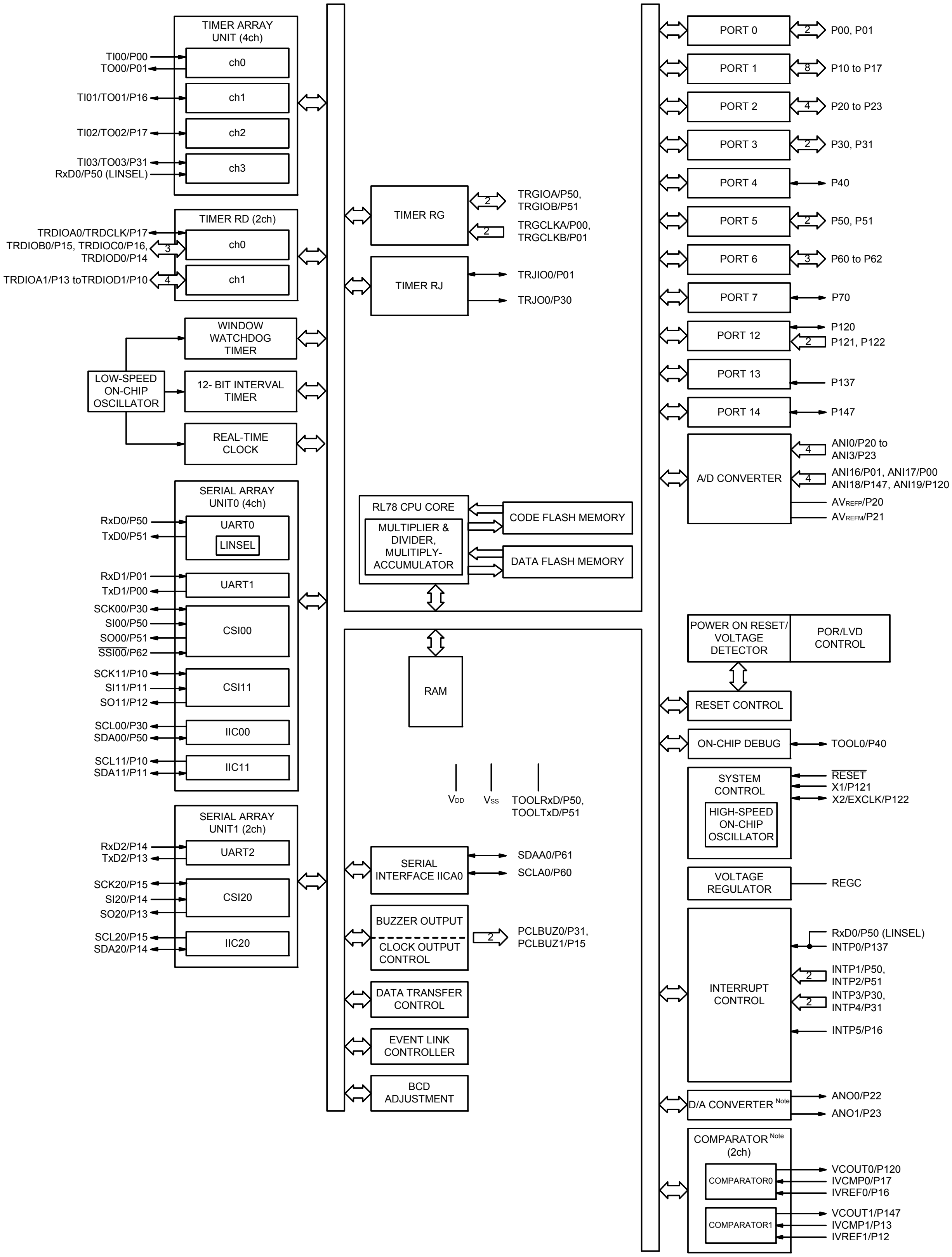
Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.

2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

This chapter describes the following electrical specifications.
Target products A: Consumer applications T_A = -40 to +85°C
R5F104xxAxx
D: Industrial applications T_A = -40 to +85°C
R5F104xxDxx
G: Industrial applications when T_A = -40 to +105°C products is used in the range of T_A = -40 to +85°C
R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual**.**

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.4		mA
						V_{DD} = 3.0 V		2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		
						V_{DD} = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		5.1	8.7	mA
						V_{DD} = 3.0 V		5.1	8.7	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	8.1	
						V_{DD} = 3.0 V		4.8	8.1	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.0	6.9	
						V_{DD} = 3.0 V		4.0	6.9	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.8	6.3	
						V_{DD} = 3.0 V		3.8	6.3	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.6	
						V_{DD} = 3.0 V		2.8	4.6	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.0	mA
						V_{DD} = 2.0 V		1.3	2.0	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA
						Resonator connection		3.4	5.5	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.3	
						Resonator connection		3.4	5.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.1	
						Resonator connection		2.1	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA
						Resonator connection		1.2	2.0	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.2	1.9	
						Resonator connection		1.2	2.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.7	6.1	μA
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.7	6.1	
						Resonator connection		4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.8	6.7	
						Resonator connection		4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.8	7.5	
						Resonator connection		4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.4	8.9	
						Resonator connection		5.4	8.9	

(**Notes** and **Remarks** are listed on the next page.)

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.80	3.09	mA
					V_{DD} = 3.0 V		0.80	3.09	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.49	2.40	
					V_{DD} = 3.0 V		0.49	2.40	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.62	2.40	
					V_{DD} = 3.0 V		0.62	2.40	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.4	1.83	
					V_{DD} = 3.0 V		0.4	1.83	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.37	1.38	
					V_{DD} = 3.0 V		0.37	1.38	
			LS (low-speed main) mode Note 7	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	710	μA
					V_{DD} = 2.0 V		260	710	
			LV (low-voltage main) mode Note 7	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		420	700	μA
					V_{DD} = 2.0 V		420	700	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.55	mA
					Resonator connection		0.40	1.74	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.55	
					Resonator connection		0.40	1.74	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.25	0.93	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.25	0.93	
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	550	μA
					Resonator connection		140	590	
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		95	550	
					Resonator connection		140	590	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = -40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.30	0.57	
					Resonator connection		0.49	0.76	
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.36	1.17	
					Resonator connection		0.59	1.36	
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.49	1.97	
					Resonator connection		0.72	2.16	
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		0.97	3.37	
					Resonator connection		1.16	3.56	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.18	0.51	μA
			T_A = +25°C				0.24	0.51	
			T_A = +50°C				0.29	1.10	
			T_A = +70°C				0.41	1.90	
			T_A = +85°C				0.90	3.30	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

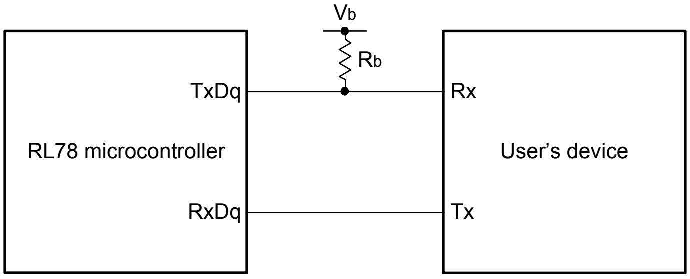
(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

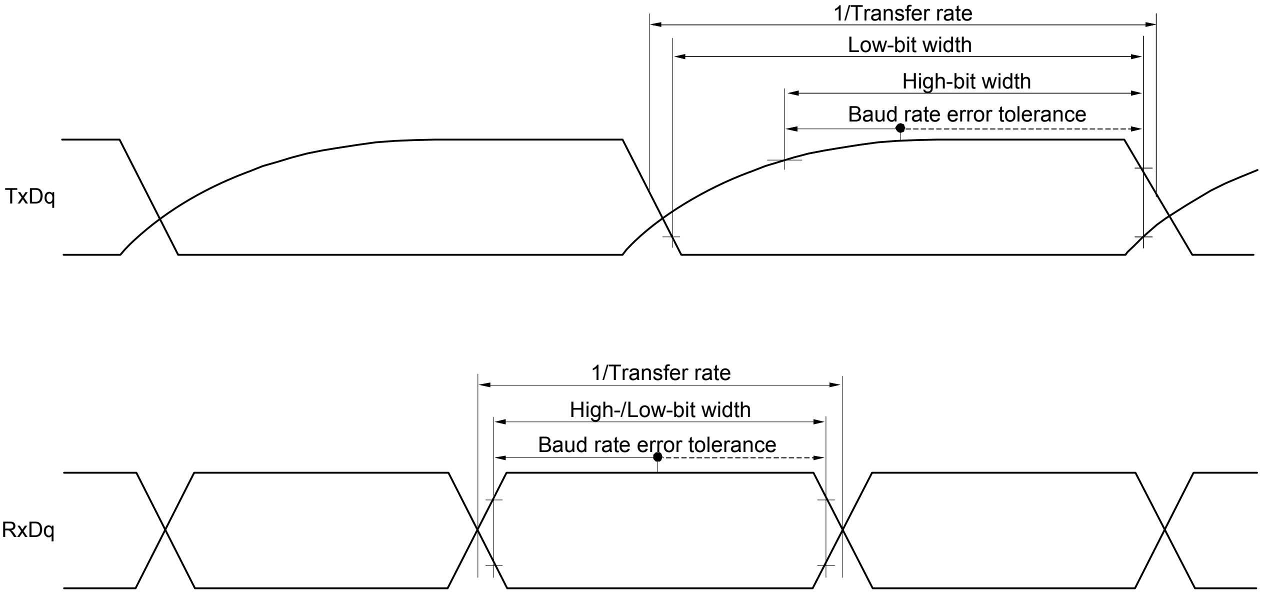
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.93	3.32	mA
					V_{DD} = 3.0 V		0.93	3.32	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.5	2.63	
					V_{DD} = 3.0 V		0.5	2.63	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.72	2.60	
					V_{DD} = 3.0 V		0.72	2.60	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	2.03	
					V_{DD} = 3.0 V		0.42	2.03	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.50	
					V_{DD} = 3.0 V		0.39	1.50	
			LS (low-speed main) mode Note 7	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		270	800	μA
					V_{DD} = 2.0 V		270	800	
			LV (low-voltage main) mode Note 7	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		450	755	μA
					V_{DD} = 2.0 V		450	755	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.31	1.69	mA
					Resonator connection		0.41	1.91	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.31	1.69	
					Resonator connection		0.41	1.91	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.21	0.94	
					Resonator connection		0.26	1.02	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.21	0.94	
					Resonator connection		0.26	1.02	
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		110	610	μA
					Resonator connection		150	660	
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		110	610	
					Resonator connection		150	660	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = -40°C	Square wave input		0.31		μA
					Resonator connection		0.50		
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.38	0.76	
					Resonator connection		0.57	0.95	
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.47	3.59	
					Resonator connection		0.70	3.78	
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.80	6.20	
					Resonator connection		1.00	6.39	
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		1.65	10.56	
					Resonator connection		1.84	10.75	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.19		μA
			T_A = +25°C				0.30	0.59	
			T_A = +50°C				0.41	3.42	
			T_A = +70°C				0.80	6.03	
			T_A = +85°C				1.53	10.39	

(**Notes** and **Remarks** are listed on the next page.)

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

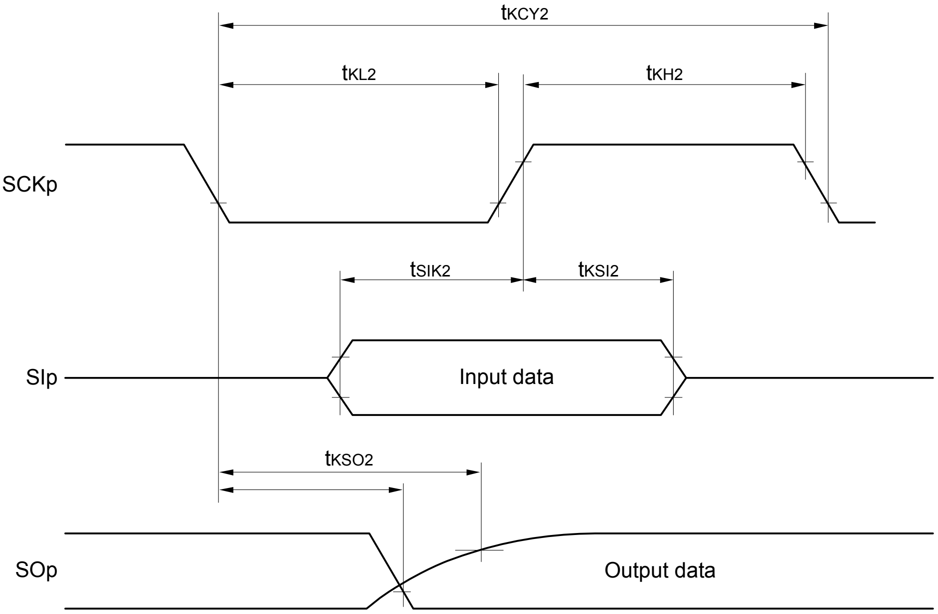
Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use it with EV_{DD0} ≥ V_b.

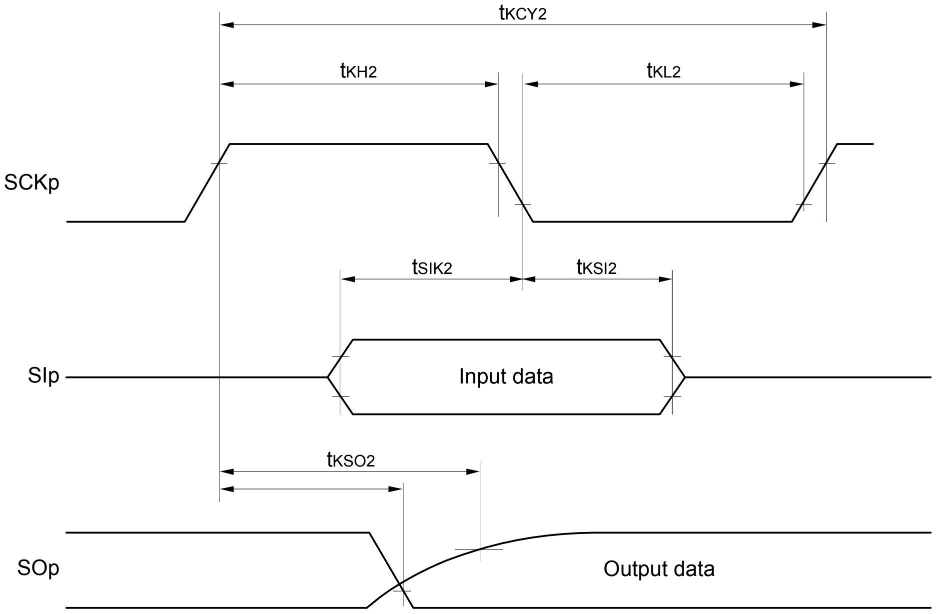
Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} = EV_{DD1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error:	Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.
Integral linearity error:	Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.
Differential linearity error:	Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = $\mathrm{AV_{REFP}}$ Reference voltage (-) = $\mathrm{AV_{REFM}}$	Reference voltage (+) = $\mathrm{V_{DD}}$ Reference voltage (-) = $\mathrm{V_{SS}}$	Reference voltage (+) = $\mathrm{V_{BGR}}$ Reference voltage (-)= $\mathrm{AV_{REFM}}$
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI20	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = $\mathrm{AV_{REFP}}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $\mathrm{AV_{REFM}}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($\mathrm{T_A}$ = -40 to +105°C, 2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V, $\mathrm{V_{SS}}$ = 0 V, Reference voltage (+) = $\mathrm{AV_{REFP}}$, Reference voltage (-) = $\mathrm{AV_{REFM}}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$ Note 3	2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	$\mathrm{t_{CONV}}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	$\mathrm{E_{ZS}}$	10-bit resolution $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$ Note 3	2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	$\mathrm{E_{FS}}$	10-bit resolution $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$ Note 3	2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$ Note 3	2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$ Note 3	2.4 V ≤ $\mathrm{AV_{REFP}}$ ≤ 5.5 V			±1.5	LSB
Analog input voltage	$\mathrm{V_{AIN}}$	ANI2 to ANI14		0		$\mathrm{AV_{REFP}}$	V
		Internal reference voltage output (2.4 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V, HS (high-speed main) mode)		$\mathrm{V_{BGR}}$ Note 4			V
		Temperature sensor output voltage (2.4 V ≤ $\mathrm{V_{DD}}$ ≤ 5.5 V, HS (high-speed main) mode)		$\mathrm{V_{TMPS25}}$ Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $\mathrm{AV_{REFP}}$ < $\mathrm{V_{DD}}$, the MAX. values are as follows.

Overall error:	Add ±1.0 LSB to the MAX. value when $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$.
Zero-scale error/Full-scale error:	Add ±0.05%FSR to the MAX. value when $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$.
Integral linearity error/ Differential linearity error:	Add ±0.5 LSB to the MAX. value when $\mathrm{AV_{REFP}}$ = $\mathrm{V_{DD}}$.

Note 4. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

3.6.4 Comparator

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref			0		EV_{DD0} - 1.4	V
	Ivcmp			-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V Input slew rate > 50 mV/µs	Comparator high-speed mode, standard mode			1.2	µs
			Comparator high-speed mode, window mode			2.0	µs
			Comparator low-speed mode, standard mode		3.0	5.0	µs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode			0.76 V_{DD}		V
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode			0.24 V_{DD}		V
Operation stabilization wait time	t_{CMP}			100			µs
Internal reference voltage Note	VBGR	2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.50	V

Note Not usable in sub-clock operation or STOP mode.

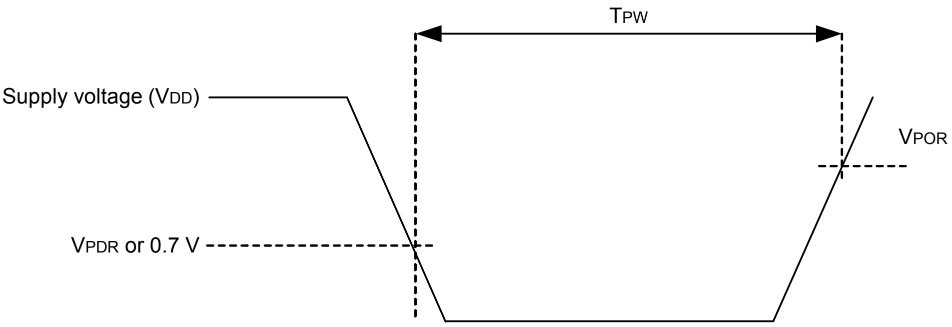
3.6.5 POR circuit characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on V_{DD} rising	1.45	1.51	1.57	V
	V_{PDR}	Voltage threshold on V_{DD} falling Note 1	1.44	1.50	1.56	V
Minimum pulse width Note 2	T_{PW}		300			µs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

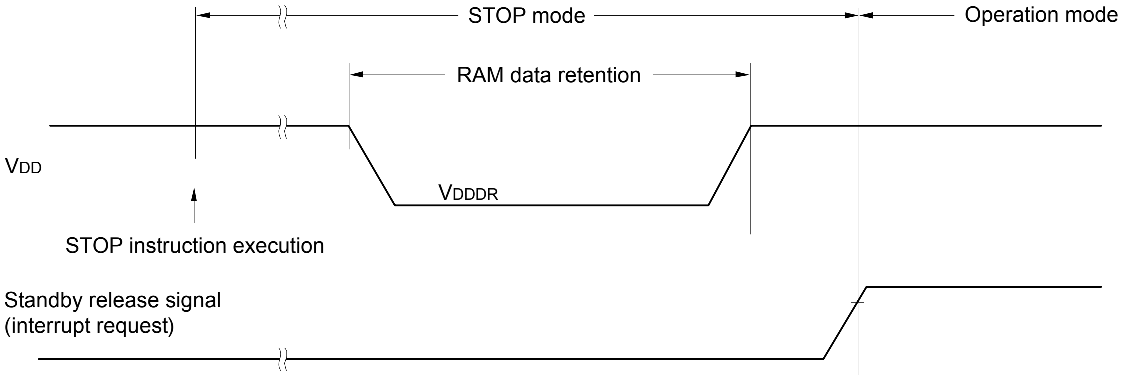


3.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

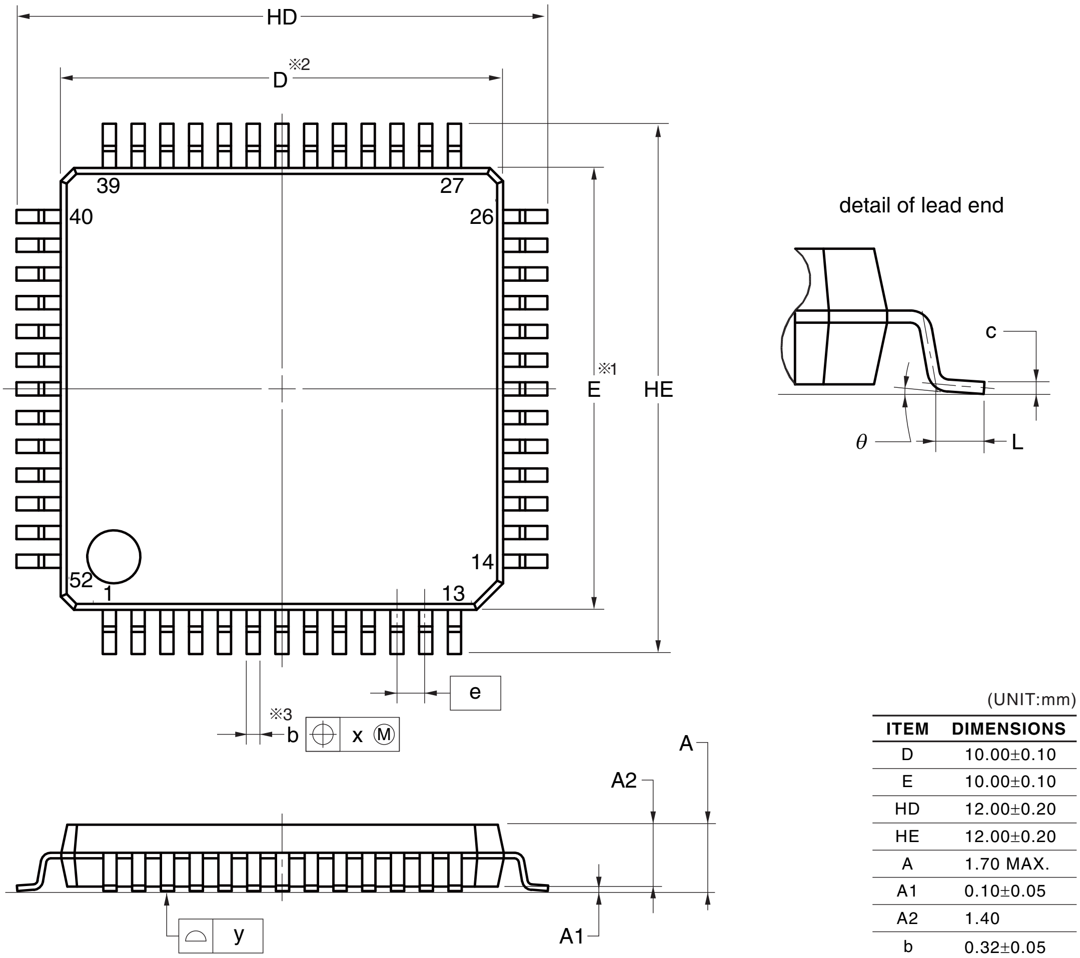
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

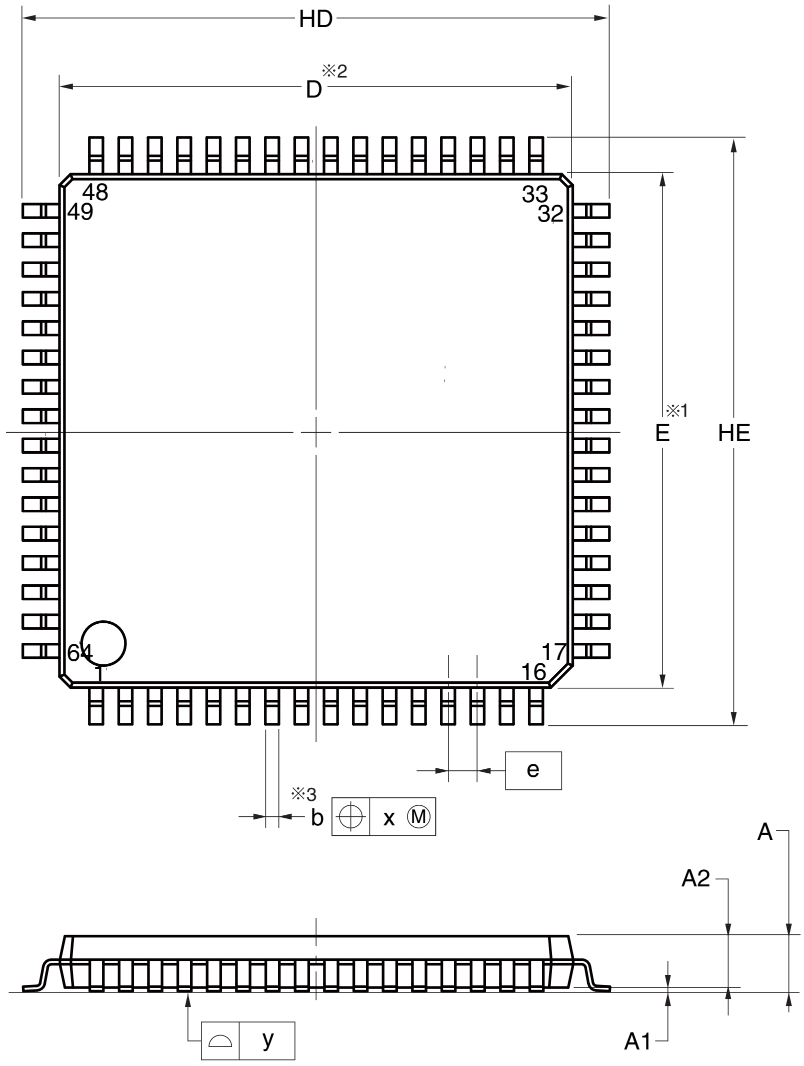
NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

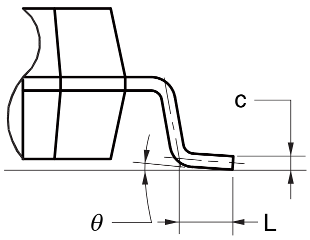
2.Dimension “※3” does not include trim offset.

R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LFDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.10
E	14.00±0.10
HD	16.00±0.20
HE	16.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	$0.37^{+0.08}_{-0.05}$
c	$0.125^{+0.05}_{-0.02}$
L	0.50±0.20
θ	0° to 8°
$\boxed{e}$	0.80
x	0.20
y	0.10

NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.