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What is "Embedded - Microcontrollers"?

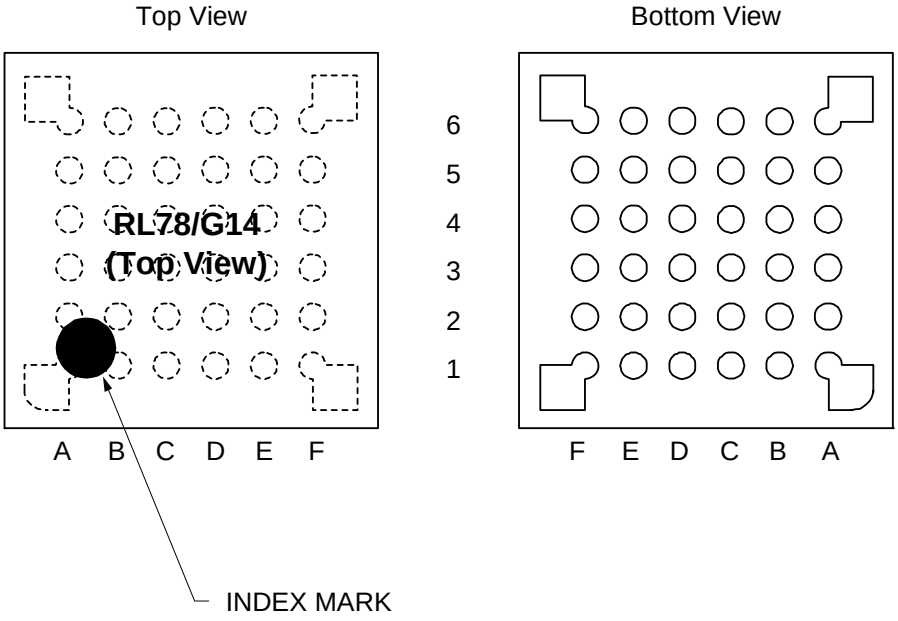
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104pgafa-v0

1.3.3 36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	P60/SCLA0	VDD	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62/$\overline{\text{SSI00}}$	P61/SDAA0	VSS	REGC	$\overline{\text{RESET}}$	P120/ANI19/ VCOUT0 Note	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0)	P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0)	P00/TI00/TxD1/ TRGCLKA/ (TRJO0)	P01/TO00/ RxD1/TRGCLKB/ TRJIO0	4
3	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0)	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0)	P22/ANI2/ ANO0 Note	P20/ANI0/ AVREFP	P21/ANI1/ AVREFM	3
2	P30/INTP3/ SCK00/SCL00/ TRJO0	P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0)	P12/SO11/ TRDIOB1/ IVREF1 Note	P11/SI11/ SDA11/ TRDIOC1	P24/ANI4	P23/ANI3/ ANO1 Note	2
1	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note/ (TXD0)	P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note	P10/SCK11/ SCL11/ TRDIOD1	P147/ANI18/ VCOUT1 Note	P25/ANI5	1
	A	B	C	D	E	F	

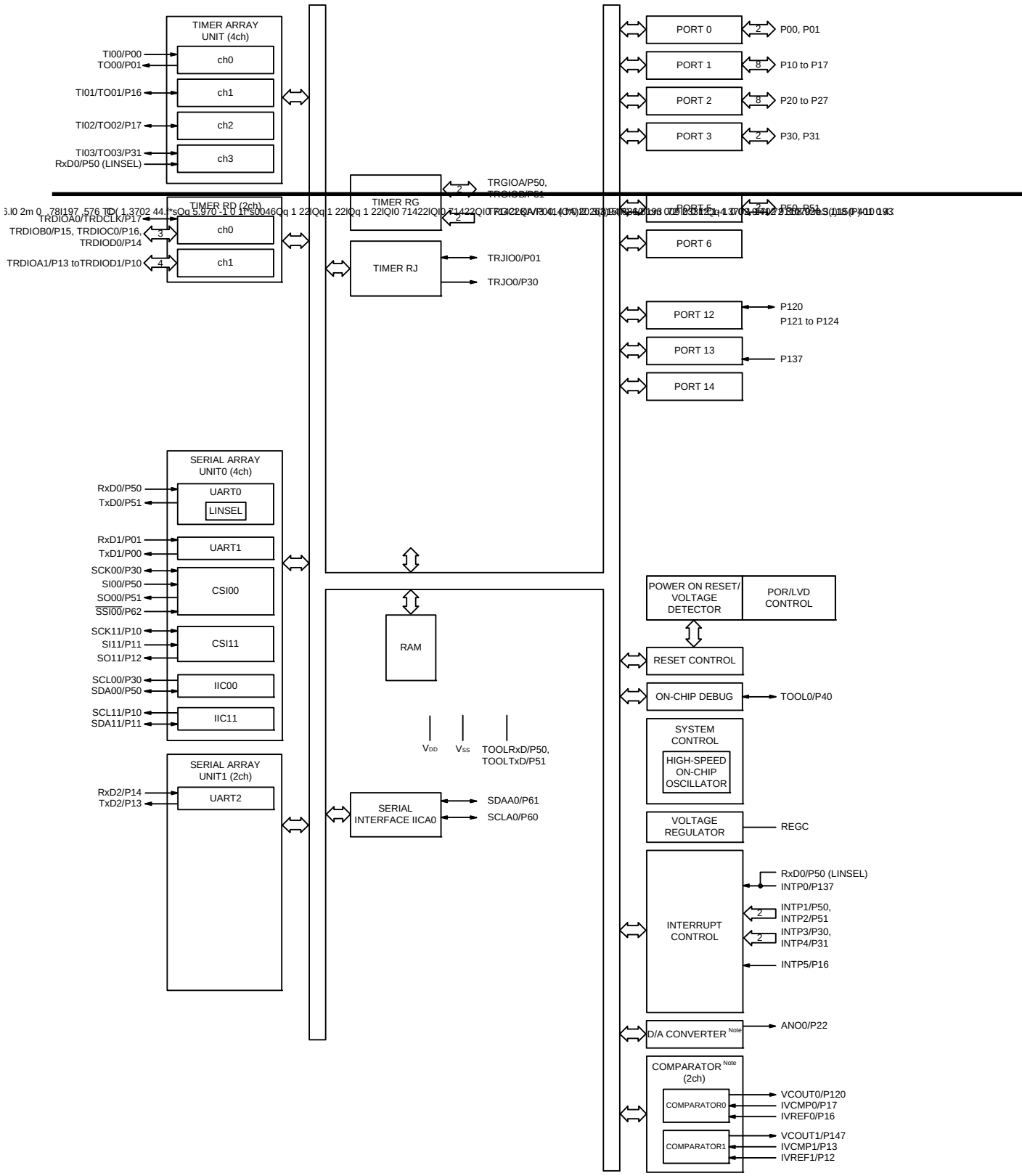
Note Mounted on the 96 KB or more code flash memory products.

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.5 44-pin products



Note Mounted on the 96 KB or more code flash memory products.TIMER RG

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

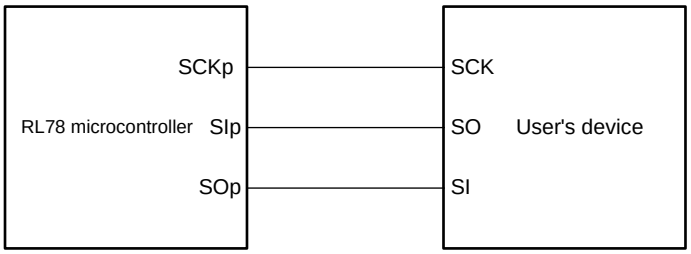
(T_A = -40 to +85°C, 1.6 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V EV_{DD0} 5.5 V	120		120		120		ns
			1.8 V EV_{DD0} 5.5 V	200		200		200		ns
			1.7 V EV_{DD0} 5.5 V	400		400		400		ns
			1.6 V EV_{DD0} 5.5 V	—		400		400		ns
		DAPmn = 1	2.7 V EV_{DD0} 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			1.8 V EV_{DD0} 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.7 V EV_{DD0} 5.5 V	1/f_{MCK} + 400		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
			1.6 V EV_{DD0} 5.5 V	—		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V EV_{DD0} 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			1.8 V EV_{DD0} 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.7 V EV_{DD0} 5.5 V	1/f_{MCK} + 400		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
			1.6 V EV_{DD0} 5.5 V	—		1/f_{MCK} + 400		1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V EV_{DD0} 5.5 V	120		120		120		ns
			1.8 V EV_{DD0} 5.5 V	200		200		200		ns
			1.7 V EV_{DD0} 5.5 V	400		400		400		ns
			1.6 V EV_{DD0} 5.5 V	—		400		400		ns

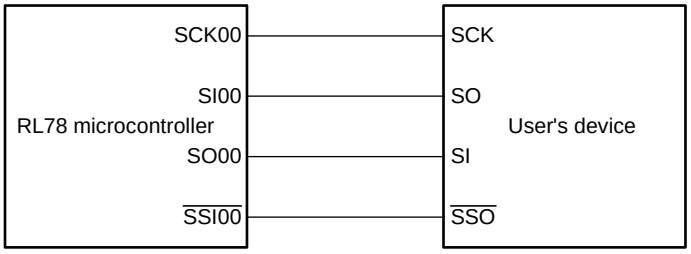
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} 4/f_{CLK}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k	300		1150		1150		ns
			2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k	500		1150		1150		ns
			1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note, C_b = 30 pF, R_b = 5.5 k	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note, C_b = 30 pF, R_b = 5.5 k		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note, C_b = 30 pF, R_b = 5.5 k		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns

Note Use it with EV_{DD0} V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k	44		110		110		ns
		2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k	44		110		110		ns
		1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 k	110		110		110		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k	19		19		19		ns
		2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k	19		19		19		ns
		1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 k	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	4.0 V EV_{DD0} 5.5 V, 2.7 V V_b 4.0 V, C_b = 30 pF, R_b = 1.4 k		25		25		25	ns
		2.7 V EV_{DD0} < 4.0 V, 2.3 V V_b 2.7 V, C_b = 30 pF, R_b = 2.7 k		25		25		25	ns
		1.8 V EV_{DD0} < 3.3 V, 1.6 V V_b 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 k		25		25		25	ns

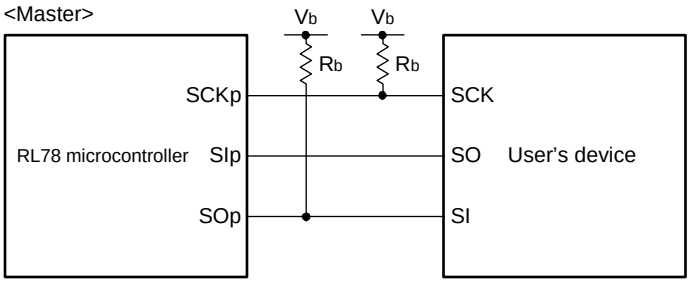
Note 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use it with EV_{DD0} V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential



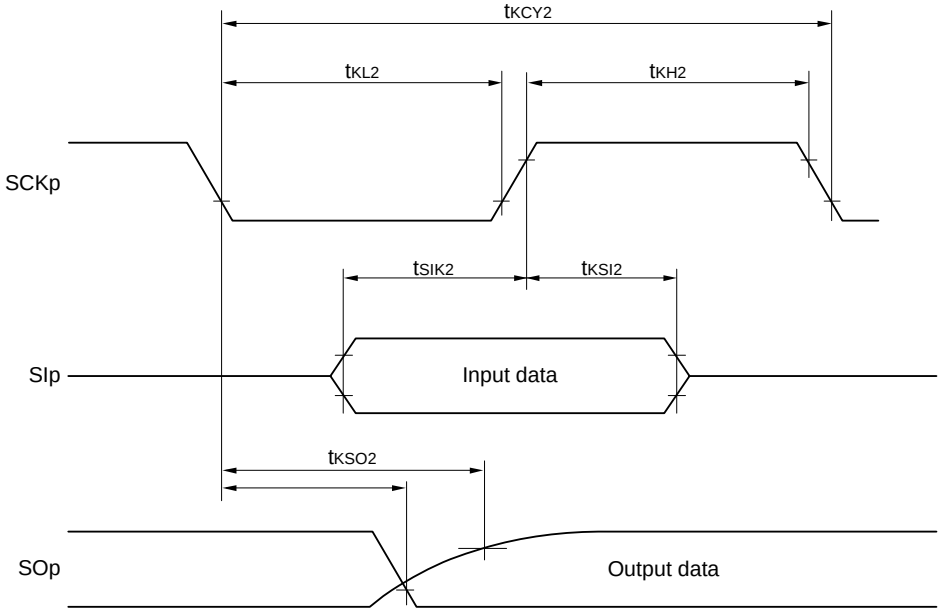
Remark 1. R_b[ ]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

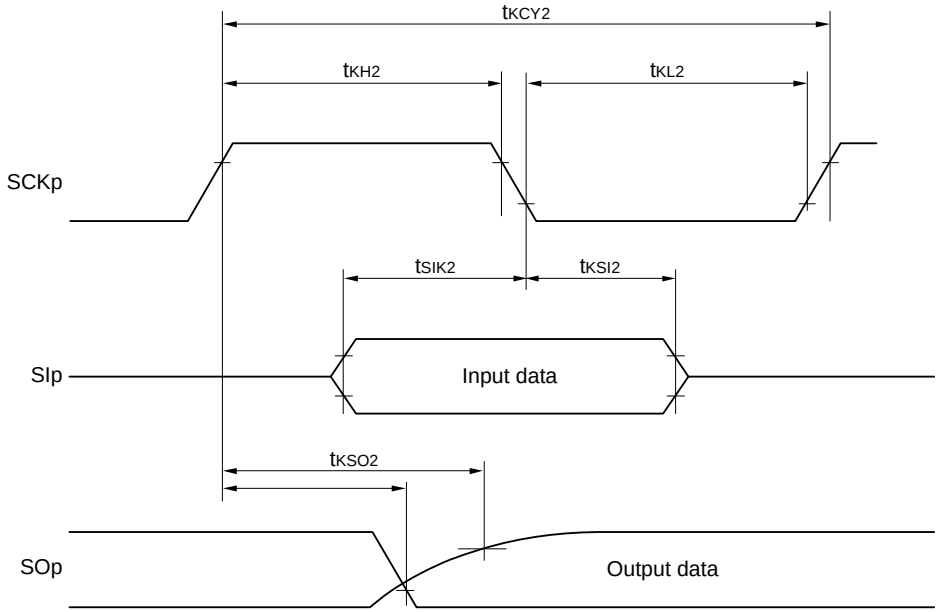
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(3) I²C fast mode plus

(T_A = -40 to +85°C, 1.6 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} 10 MHz	2.7 V EV_{DD0} 5.5 V	0	1000	—		—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V EV_{DD0} 5.5 V		0.26		—		—		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V EV_{DD0} 5.5 V		0.26		—		—		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V EV_{DD0} 5.5 V		0.5		—		—		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V EV_{DD0} 5.5 V		0.26		—		—		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V EV_{DD0} 5.5 V		50		—		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V EV_{DD0} 5.5 V		0	0.45	—		—		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V EV_{DD0} 5.5 V		0.26		—		—		μs
Bus-free time	t_{BUF}	2.7 V EV_{DD0} 5.5 V		0.5		—		—		μs

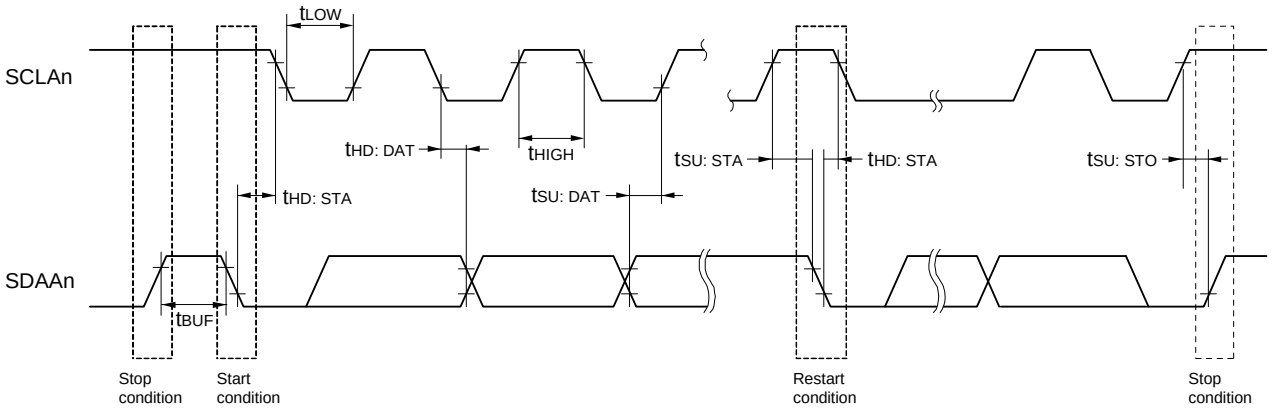
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Note 3. The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 k

IICA serial transfer timing



Remark n = 0, 1

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(T_A = -40 to +85°C, 2.4 V V_{DD} 5.5 V, 1.6 V EV_{DD} = EV_{DD1} V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V V_{DD} 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V V_{DD} 5.5 V			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V V_{DD} 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V V_{DD} 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Operation of products rated “G: Industrial applications (T_A = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

Remark The electrical characteristics of products rated “G: Industrial applications (T_A = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to **3.1** to

(T_A = -40 to +105°C, 2.4 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V_I = EV_{SS0}				-1	μA
	I_{LIL2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V_I = EV_{SS0}, In input port		10	20	100	k

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2.

<R>

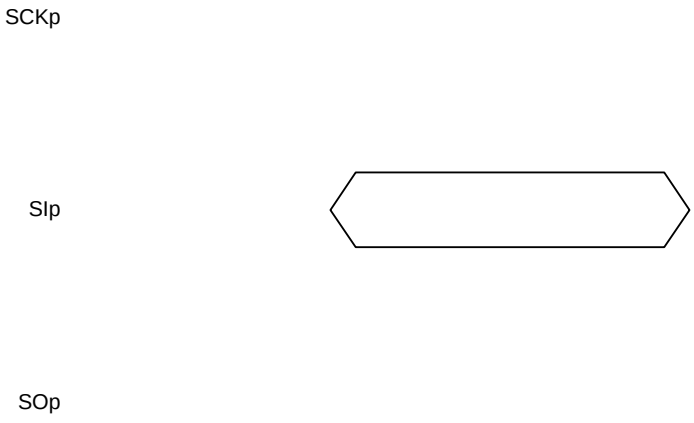
(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(T_A = -40 to +105°C, 2.4 V EV_{DD0} = EV_{DD1} V_{DD} 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.93	5.16	mA
					V_{DD} = 3.0 V		0.93	5.16	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.5	4.47	
					V_{DD} = 3.0 V		0.5	4.47	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.72	4.08	
					V_{DD} = 3.0 V		0.72	4.08	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	3.51	
					V_{DD} = 3.0 V		0.42	3.51	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	2.38	
					V_{DD} = 3.0 V		0.39	2.38	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.31	2.83	mA
					Resonator connection		0.41	2.92	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.31	2.83	
					Resonator connection		0.41	2.92	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.21	1.46	
					Resonator connection		0.26	1.57	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.21	1.46	
					Resonator connection		0.26	1.57	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = -40°C	Square wave input		0.31	0.76	μA
					Resonator connection		0.50	0.95	
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.38	0.76	
					Resonator connection		0.57	0.95	
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.47	3.59	
					Resonator connection		0.70	3.78	
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.80	6.20	
					Resonator connection		1.00	6.39	
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		1.65	10.56	
					Resonator connection		1.84	10.75	
				f_{SUB} = 32.768 kHz Note 5, T_A = +105°C	Square wave input		8.00	65.7	
					Resonator connection		8.00	65.7	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.19	0.63	μA
			T_A = +25°C				0.30	0.63	
			T_A = +50°C				0.41	3.47	
			T_A = +70°C				0.80	6.08	
			T_A = +85°C				1.53	10.44	
			T_A = +105°C				6.50	67.14	

(**Notes** and **Remarks** are listed on the next page.)

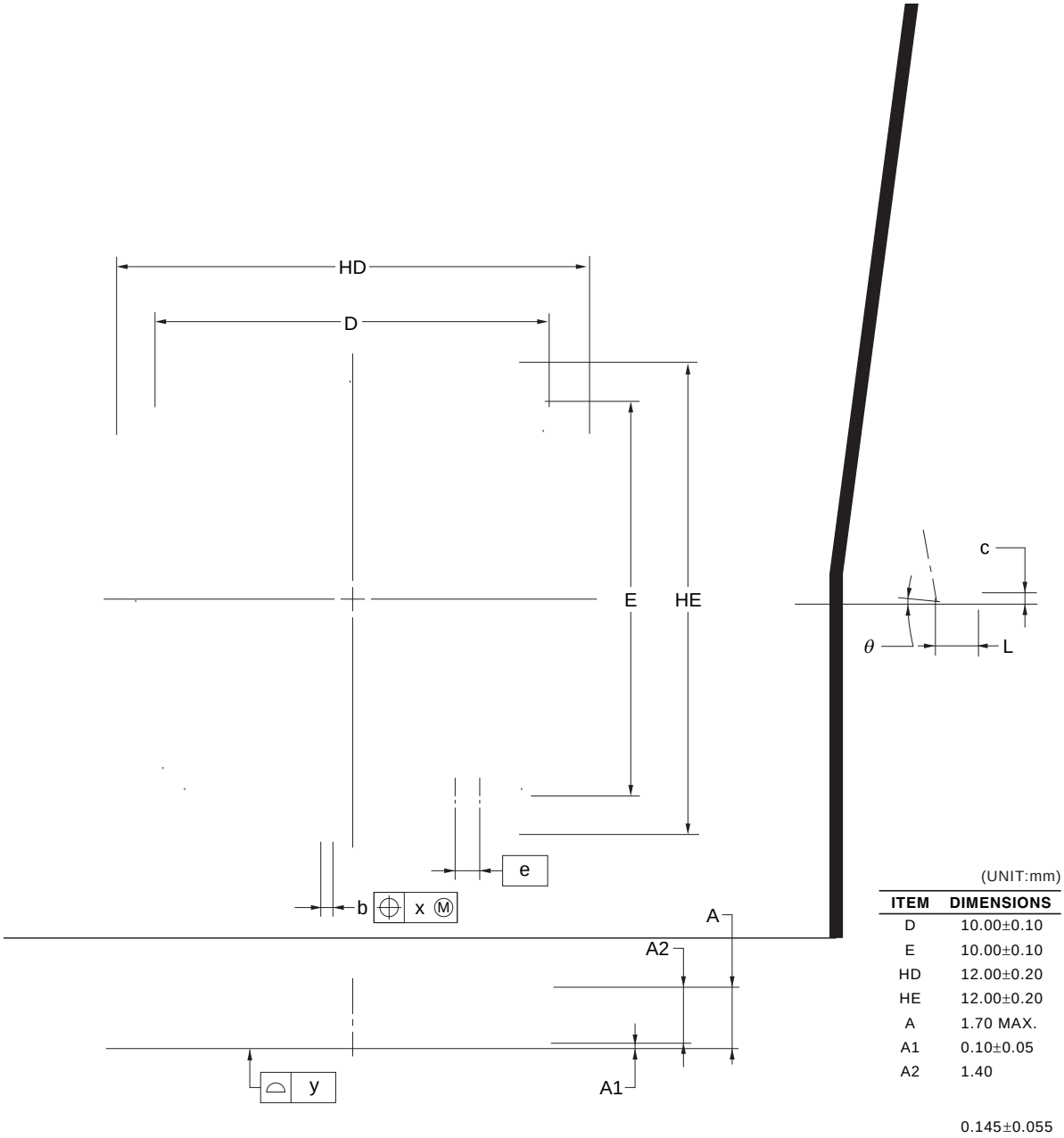
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA