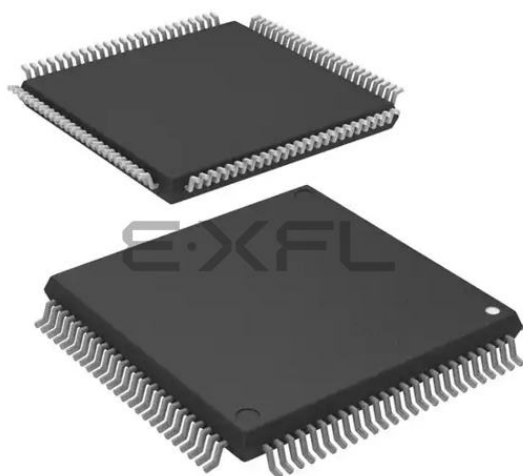




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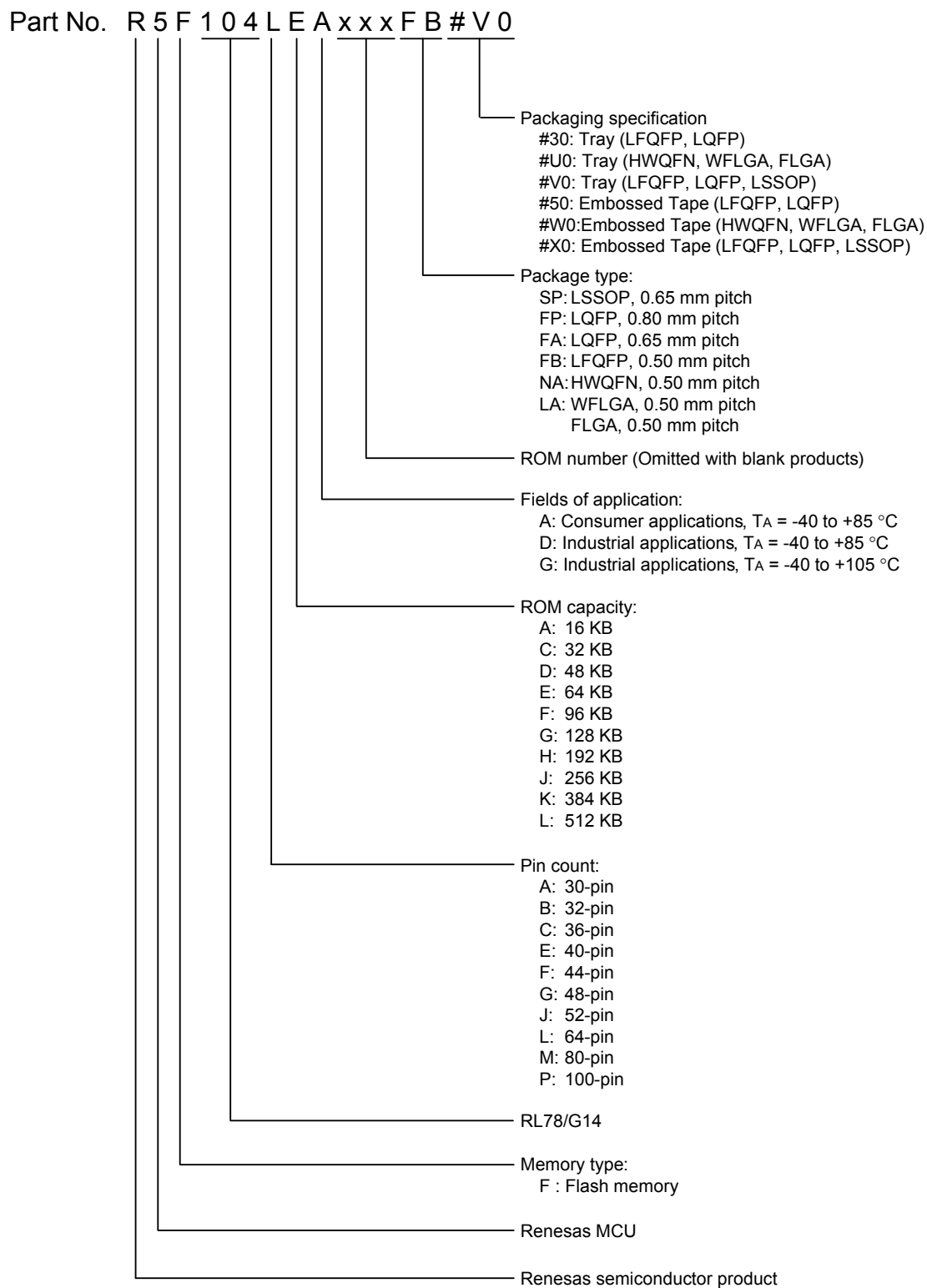
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104pga#30

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14



(3/5)

Pin count	Package	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0 R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 R5F104GKAFB#30, R5F104GLAFB#30 R5F104GKAFB#50, R5F104GLAFB#50
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0 R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0 R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0 R5F104GKGB#30, R5F104GLGB#30 R5F104GKGB#50, R5F104GLGB#50
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0 R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0 R5F104GKANA#U0, R5F104GLANA#U0 R5F104GKANA#W0, R5F104GLANA#W0
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0 R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0 R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0 R5F104GKGNA#U0, R5F104GLGNA#U0 R5F104GKGNA#W0, R5F104GLGNA#W0
	52 pins	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHFAFA#V0, R5F104JJFAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHFAFA#X0, R5F104JJFAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJFAFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJFAFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

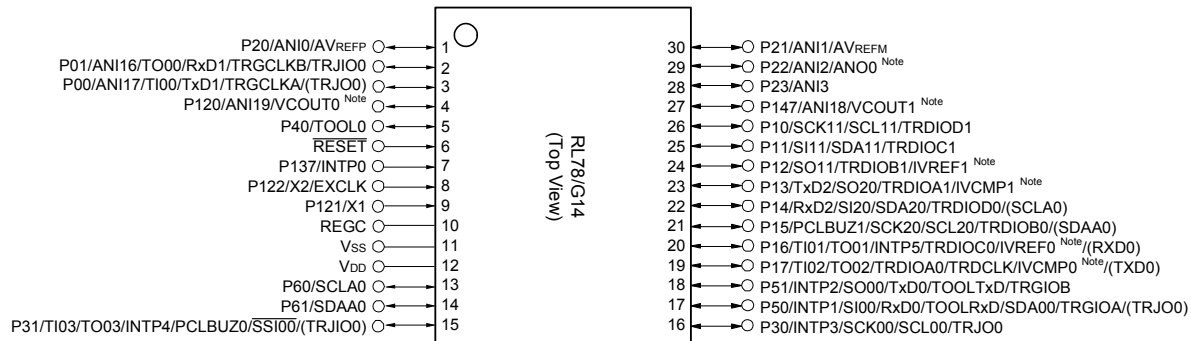
Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

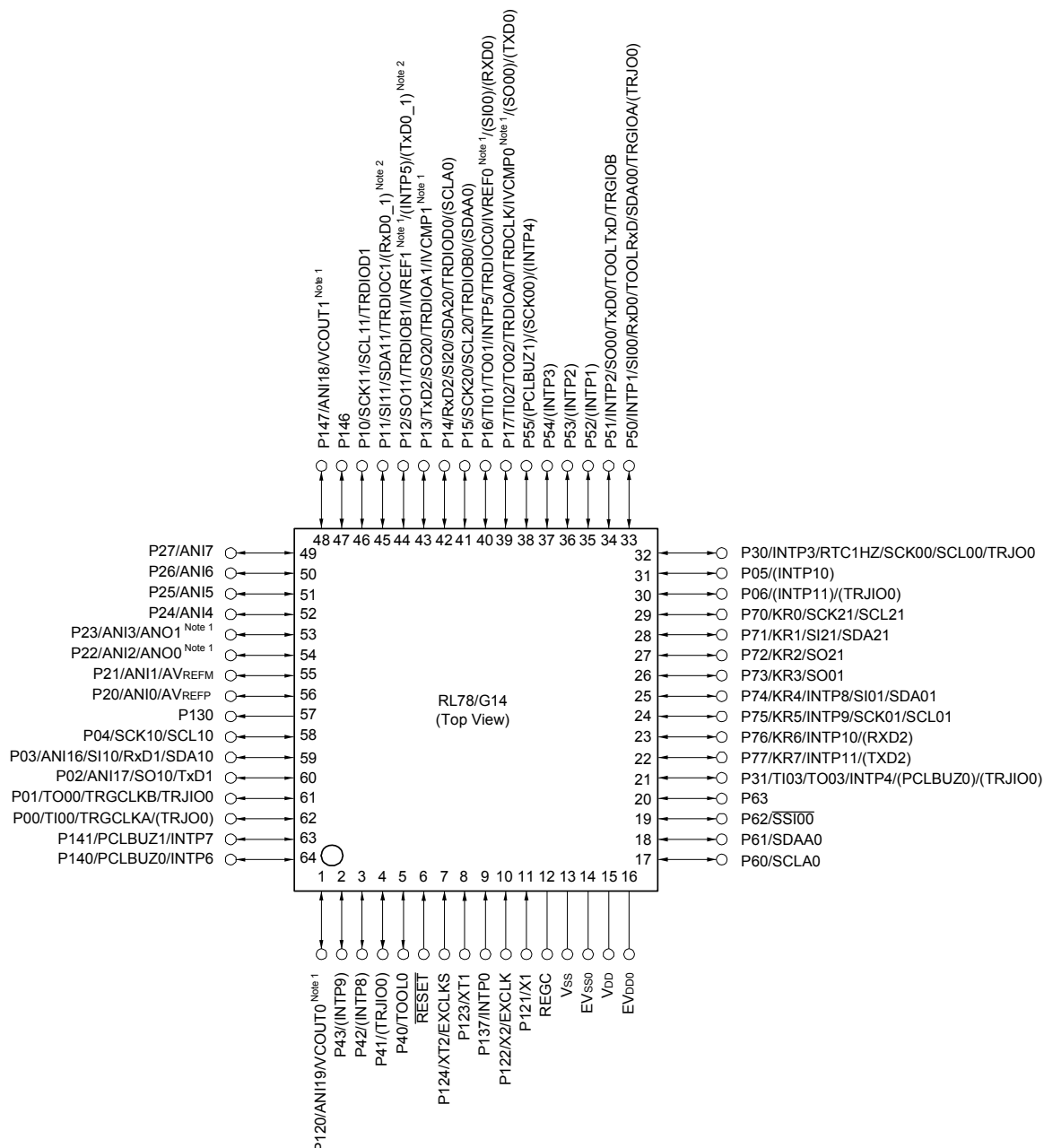
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

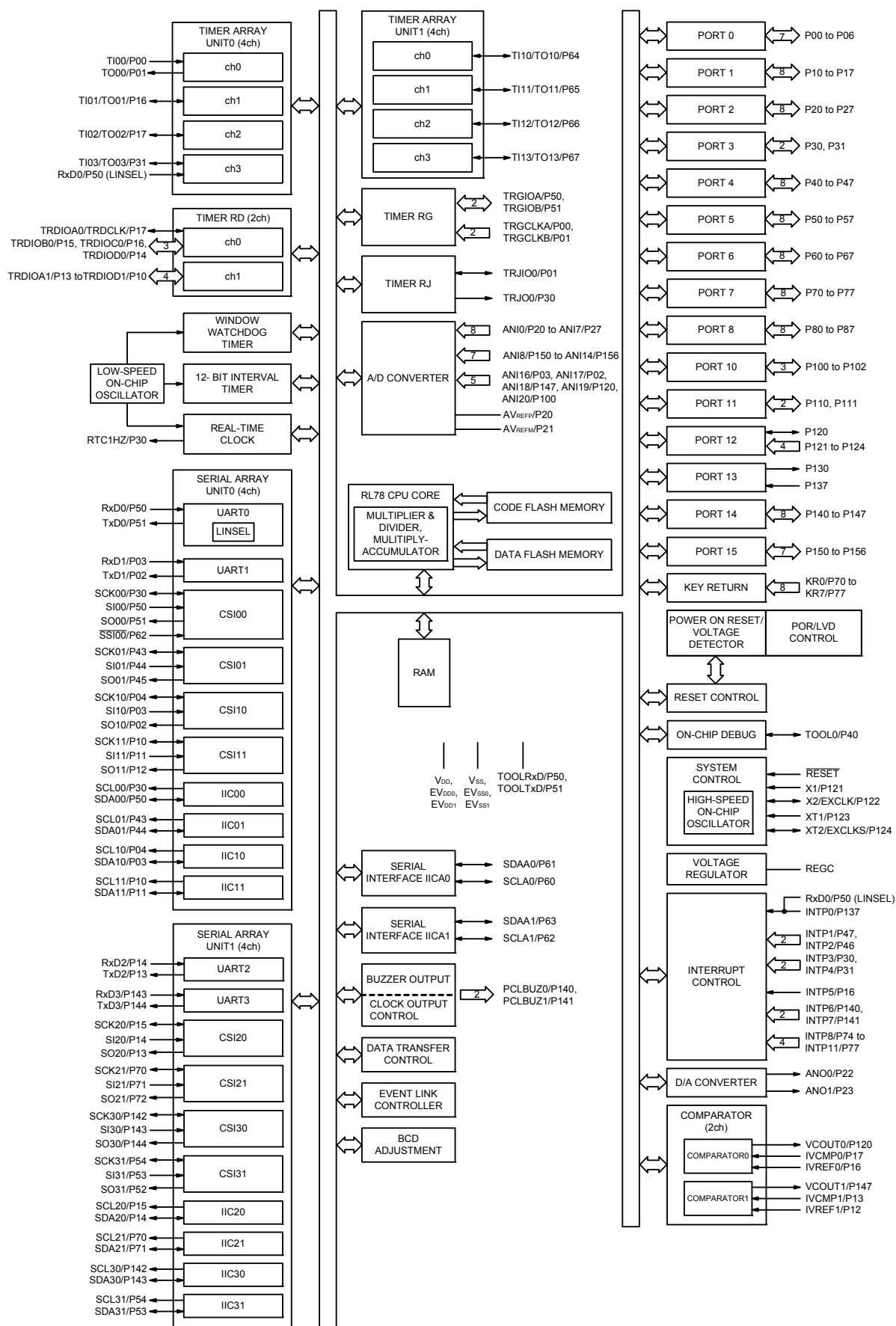
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVss0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.10 100-pin products



Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

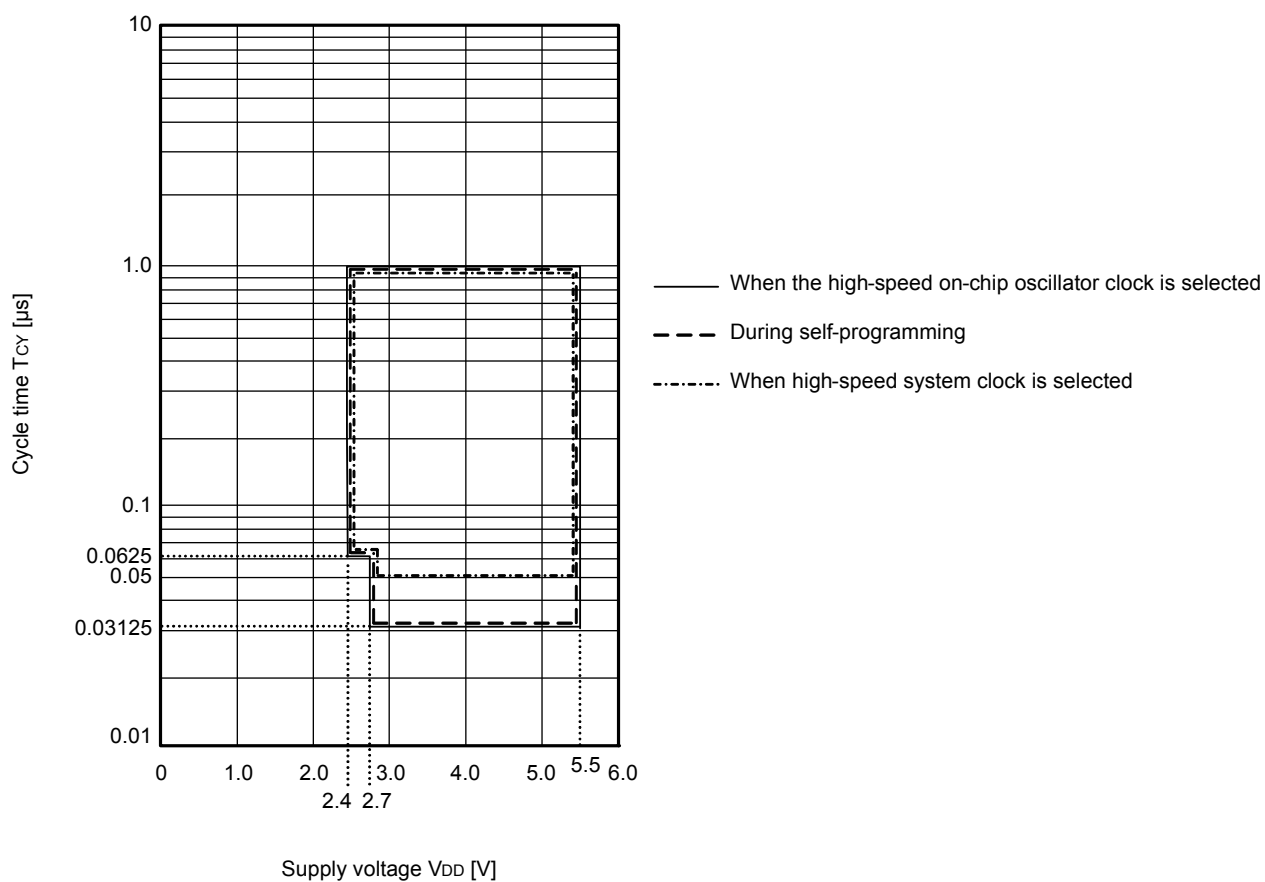
Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

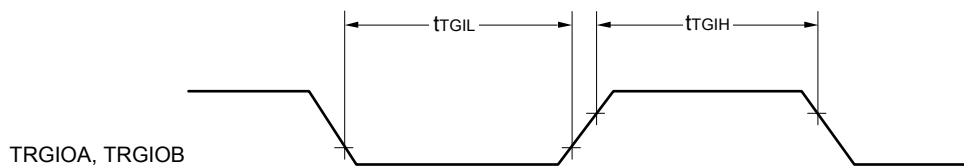
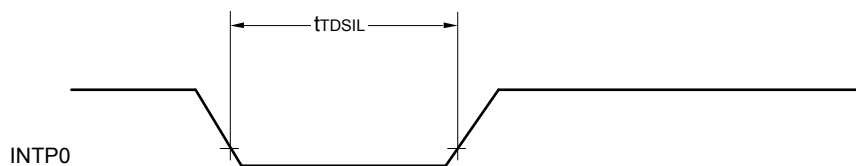
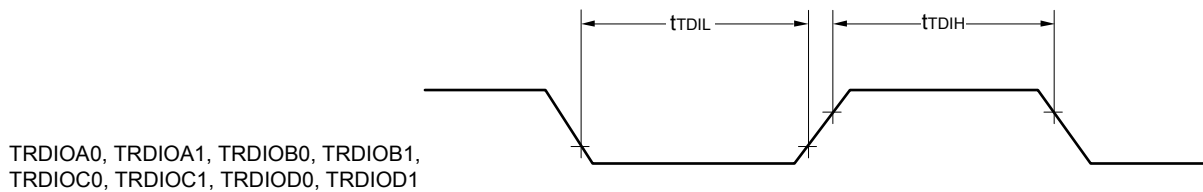
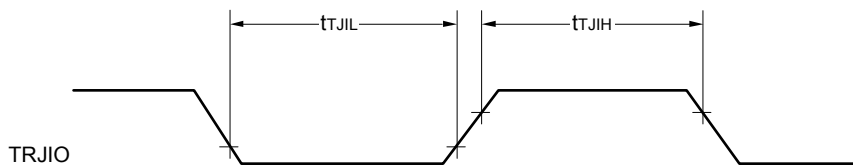
(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	3.32	mA			
					VDD = 3.0 V		0.93	3.32				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	2.63				
					VDD = 3.0 V		0.5	2.63				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	2.60				
					VDD = 3.0 V		0.72	2.60				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	2.03				
					VDD = 3.0 V		0.42	2.03				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	1.50				
					VDD = 3.0 V		0.39	1.50				
			LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		270	800	μA			
					VDD = 2.0 V		270	800				
			LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		450	755	μA			
					VDD = 2.0 V		450	755				
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	1.69	mA			
					Resonator connection		0.41	1.91				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31		1.69		
					Resonator connection		0.41	1.91				
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21		0.94		
					Resonator connection		0.26	1.02				
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	0.94				
					Resonator connection		0.26	1.02				
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA		
						Resonator connection		150	660			
			fMX = 8 MHz Note 3, VDD = 2.0 V		Square wave input		110	610				
					Resonator connection		150	660				
			Subsystem clock oper- ation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31		μA			
					Resonator connection		0.50					
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.38	0.76				
					Resonator connection		0.57	0.95				
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47	3.59				
					Resonator connection		0.70	3.78				
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80	6.20				
					Resonator connection		1.00	6.39				
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65	10.56				
					Resonator connection		1.84	10.75				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19		μA
					TA = +25°C					0.30	0.59	
					TA = +50°C					0.41	3.42	
					TA = +70°C					0.80	6.03	
					TA = +85°C					1.53	10.39	

(Notes and Remarks are listed on the next page.)

Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	t _{KSI1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

Note 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1.**Note 2.** Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(2) I²C fast mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	tSU: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	tHD: STA	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	tSU: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	tSU: STO	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Caution** The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} \leq EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

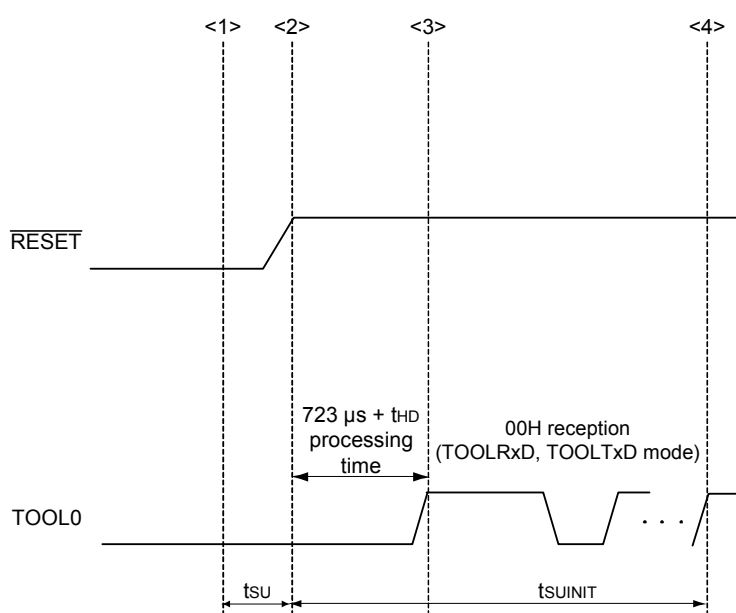
Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

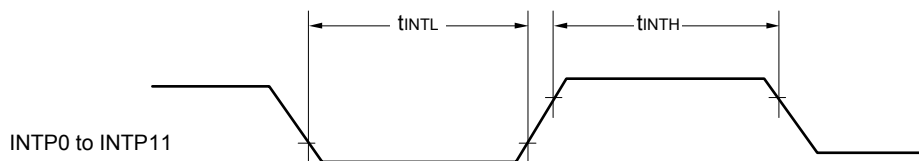
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

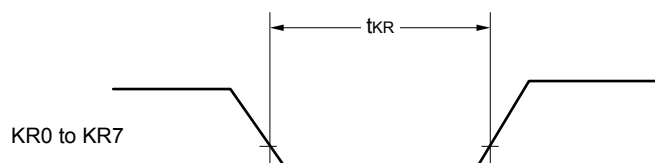
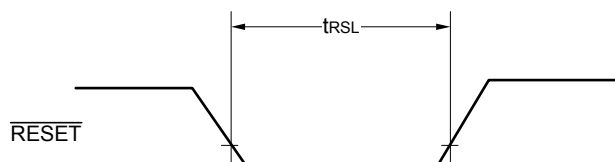
tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

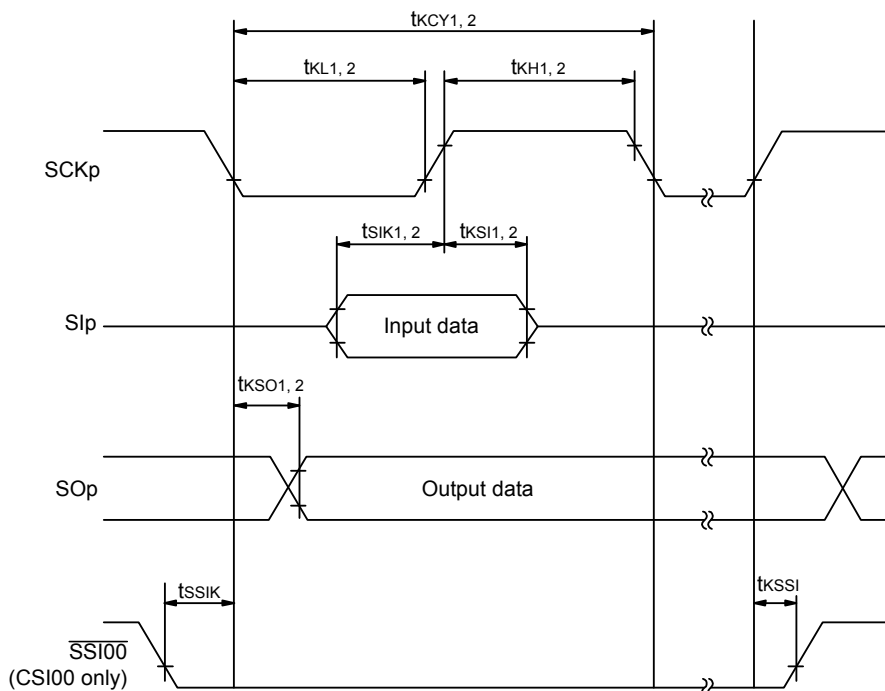
Interrupt Request Input Timing



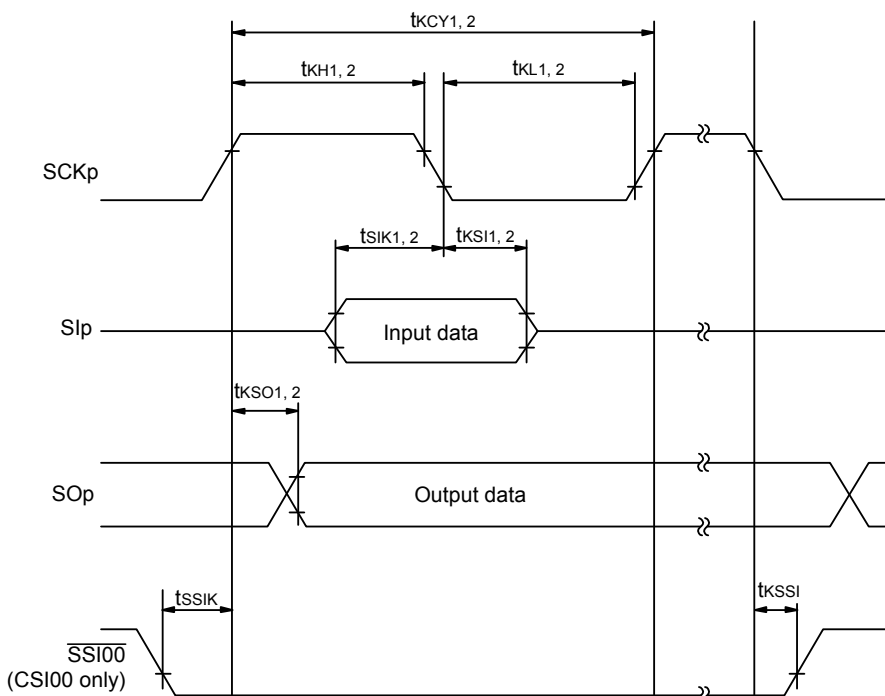
Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 Note 1	kHz
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU: DAT}}$	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ Note 2		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ Note 2		ns
Data hold time (transmission)	$t_{\text{HD: DAT}}$	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Note 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

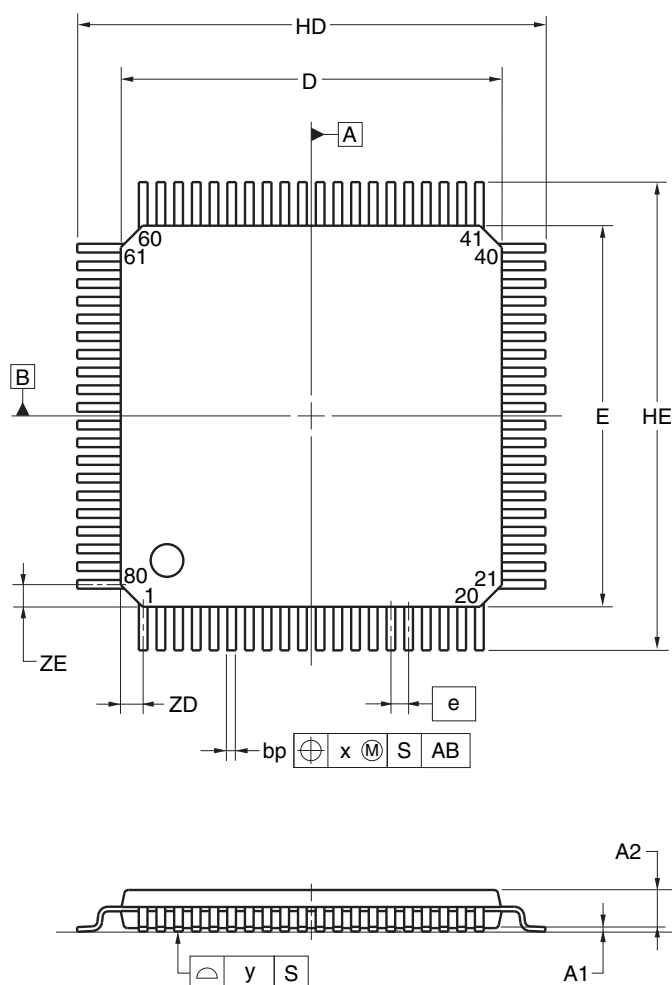
Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} $\geq 4/f_{\text{CLK}}$ 4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω		600		ns
			2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω	1000		ns
			2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω	2300		ns
SCKp high-level width	t _{KH1}	4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω		t _{KCY1} /2 - 150		ns
		2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω		t _{KCY1} /2 - 340		ns
		2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω		t _{KCY1} /2 - 916		ns
SCKp low-level width	t _{KL1}	4.0 V $\leq \text{EVDD0} \leq 5.5\text{ V}$, 2.7 V $\leq \text{Vb} \leq 4.0\text{ V}$, C _b = 30 pF, R _b = 1.4 k Ω		t _{KCY1} /2 - 24		ns
		2.7 V $\leq \text{EVDD0} < 4.0\text{ V}$, 2.3 V $\leq \text{Vb} \leq 2.7\text{ V}$, C _b = 30 pF, R _b = 2.7 k Ω		t _{KCY1} /2 - 36		ns
		2.4 V $\leq \text{EVDD0} < 3.3\text{ V}$, 1.6 V $\leq \text{Vb} \leq 2.0\text{ V}$, C _b = 30 pF, R _b = 5.5 k Ω		t _{KCY1} /2 - 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

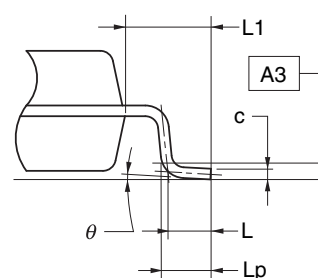
(Remarks are listed two pages after the next page.)

R5F104MFAFA, R5F104MGAFA, R5F104MHAFA, R5F104MJFAFA
 R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
 R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
 R5F104MKAFA, R5F104MLAFA
 R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



detail of lead end



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
θ	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—

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