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What is "[Embedded - Microcontrollers](#)"?

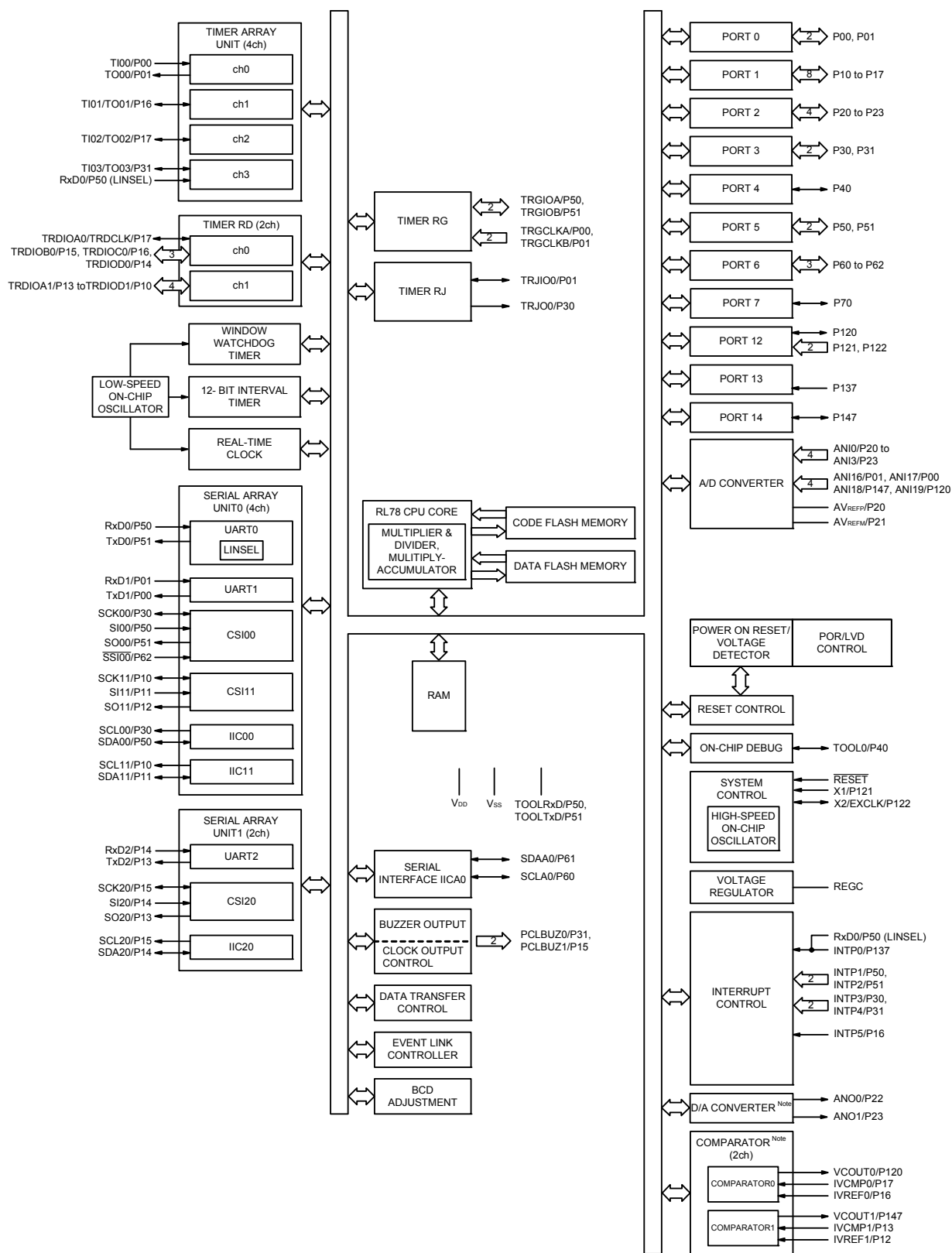
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104pjafa-v0

1.5.2 32-pin products



Note Mounted on the 96 KB or more code flash memory products.

(2/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Clock output/buzzer output		2	2	2	2
		[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels
Serial interface		[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		28 sources			29 sources
Event link controller (ELC)		Event input: 19 Event trigger output: 7			Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	24	24	24	24
	External	6	6	6	7
Key interrupt		—	—	—	4
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V ($T_A = -40$ to +85°C) 1.51 ±0.06 V ($T_A = -40$ to +105°C) • Power-down-reset: 1.50 ±0.04 V ($T_A = -40$ to +85°C) 1.50 ±0.06 V ($T_A = -40$ to +105°C)			
Voltage detector		1.63 V to 4.06 V (14 stages)			
On-chip debug function		Provided			
Power supply voltage		$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to +85°C) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to +105°C)			
Operating ambient temperature		$T_A = -40$ to +85°C (A: Consumer applications, D: Industrial applications), $T_A = -40$ to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = F to H, J)	R5F104Gx (x = F to H, J)	R5F104Jx (x = F to H, J)	R5F104Lx (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256	96 to 256	96 to 256
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 24 Note	12 to 24 Note	12 to 24 Note	12 to 24 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)			

(Note is listed on the next page.)

Absolute Maximum Ratings

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-10.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-55.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-10.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-5.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-80.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-19.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-10.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-5.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-135.0 ^{Note 4}	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
 <Example> Where n = 80% and I_{OH} = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Note 4. -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

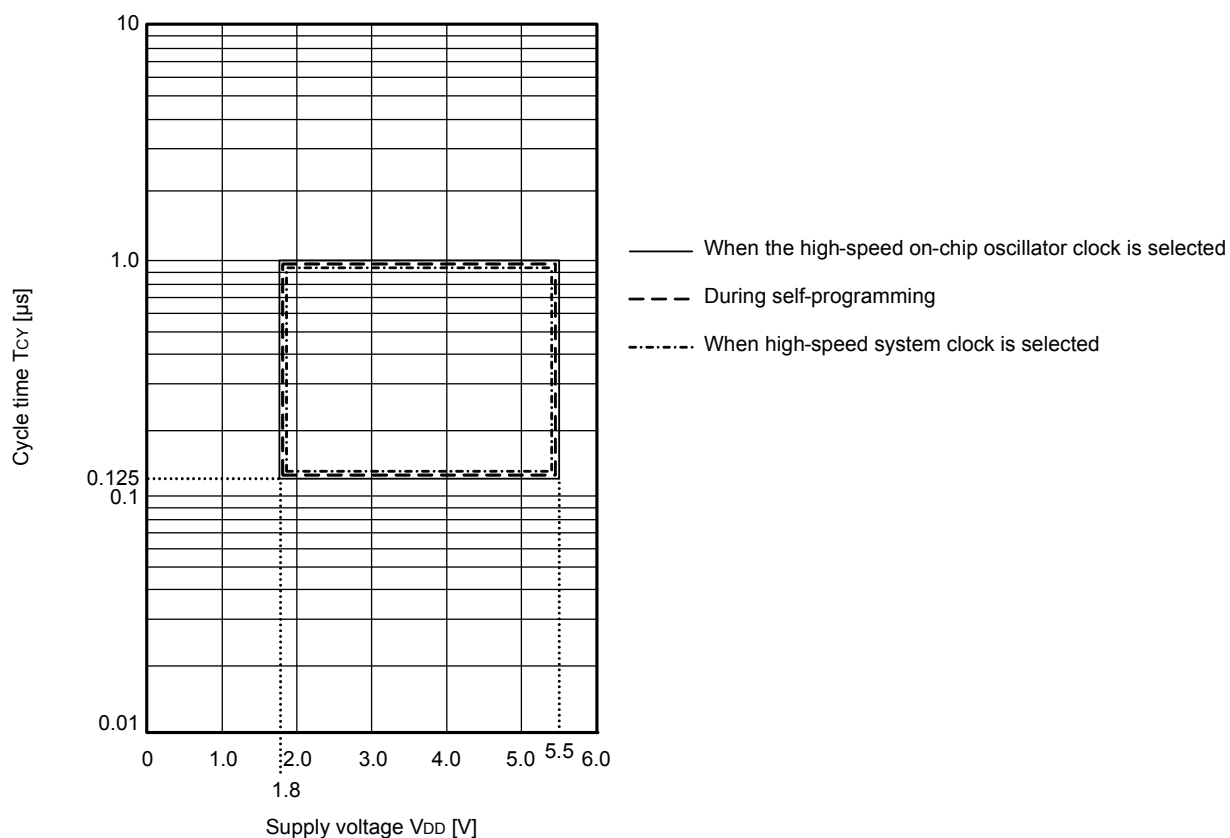
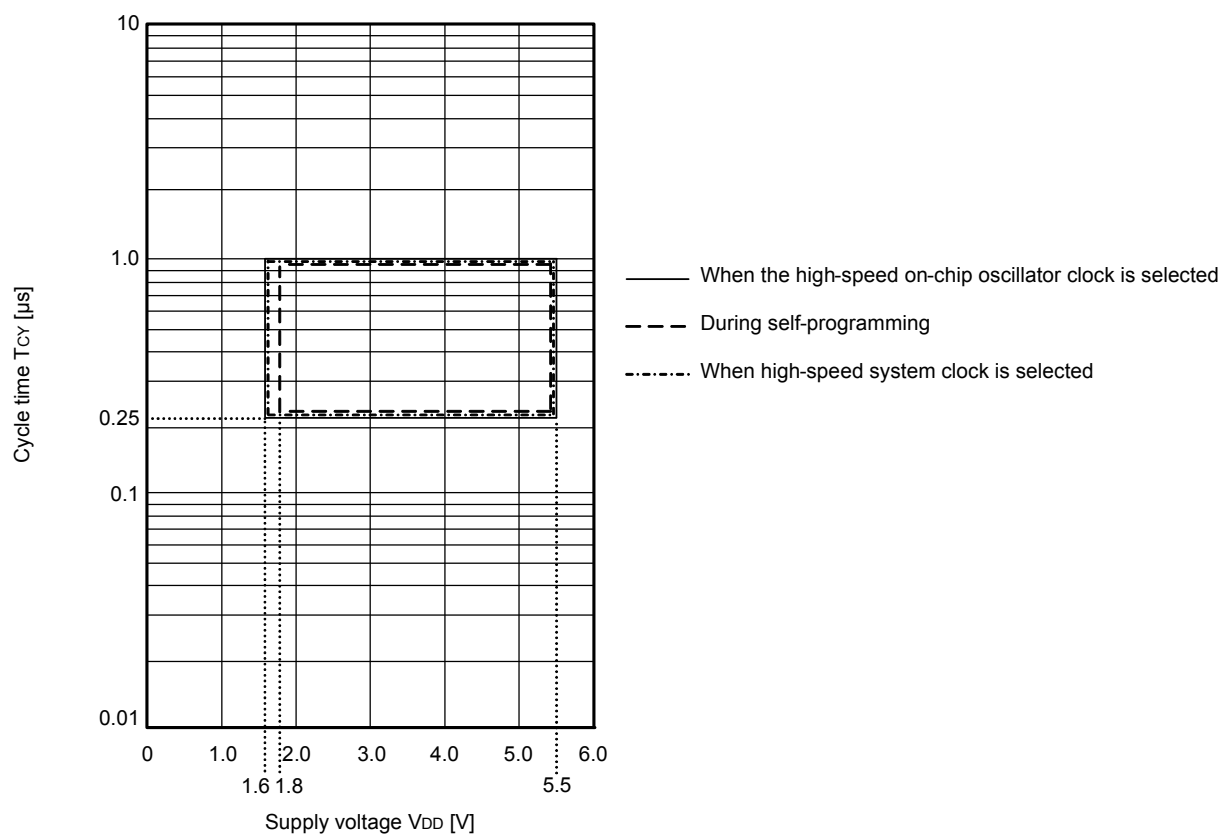
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Note 1.** Total current flowing into VDD, EVDD0, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0, and EVDD1, or VSS, EVSS0, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|-------------------------------------|
| HS (high-speed main) mode: | 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ VDD ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ VDD ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** fIH: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	3.32	mA			
					VDD = 3.0 V		0.93	3.32				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	2.63				
					VDD = 3.0 V		0.5	2.63				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	2.60				
					VDD = 3.0 V		0.72	2.60				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	2.03				
					VDD = 3.0 V		0.42	2.03				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	1.50				
					VDD = 3.0 V		0.39	1.50				
			LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		270	800	μA			
					VDD = 2.0 V		270	800				
			LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		450	755	μA			
					VDD = 2.0 V		450	755				
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	1.69	mA			
					Resonator connection		0.41	1.91				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31		1.69		
					Resonator connection		0.41	1.91				
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21		0.94		
					Resonator connection		0.26	1.02				
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	0.94				
					Resonator connection		0.26	1.02				
					LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA	
							Resonator connection		150	660		
			fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input			110	610				
				Resonator connection			150	660				
			Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31		μA			
					Resonator connection		0.50					
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.38	0.76				
					Resonator connection		0.57	0.95				
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47	3.59				
					Resonator connection		0.70	3.78				
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80	6.20				
					Resonator connection		1.00	6.39				
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65	10.56				
					Resonator connection		1.84	10.75				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19		μA
					TA = +25°C					0.30	0.59	
					TA = +50°C					0.41	3.42	
					TA = +70°C					0.80	6.03	
					TA = +85°C					1.53	10.39	

(Notes and Remarks are listed on the next page.)

T_{CY} vs V_{DD} (LS (low-speed main) mode)T_{CY} vs V_{DD} (LV (low-voltage main) mode)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ EVDD0 ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 12		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 18		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 38		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		t _{KCY1} /2 - 100		t _{KCY1} /2 - 100		t _{KCY1} /2 - 100		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		t _{KCY1} /2 - 100		t _{KCY1} /2 - 100		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EVDD0 ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) Note 2	t _{KSI1}	1.7 V ≤ EVDD0 ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t _{KSO1}	1.7 V ≤ EVDD0 ≤ 5.5 V C = 30 pF Note 4			25		25		25	ns
		1.6 V ≤ EVDD0 ≤ 5.5 V C = 30 pF Note 4			—		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
Data hold time (transmission)	thd: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		0	405	0	405	ns

Note 1. The value must also be equal to or less than fMCK/4.**Note 2.** Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
									Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
									Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	fMCK/6 Notes 1, 2, 3		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
									Mbps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 4	5.3		1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. Use it with EVDD0 ≥ Vb.**Note 3.** The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb [V]: Communication line voltage**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

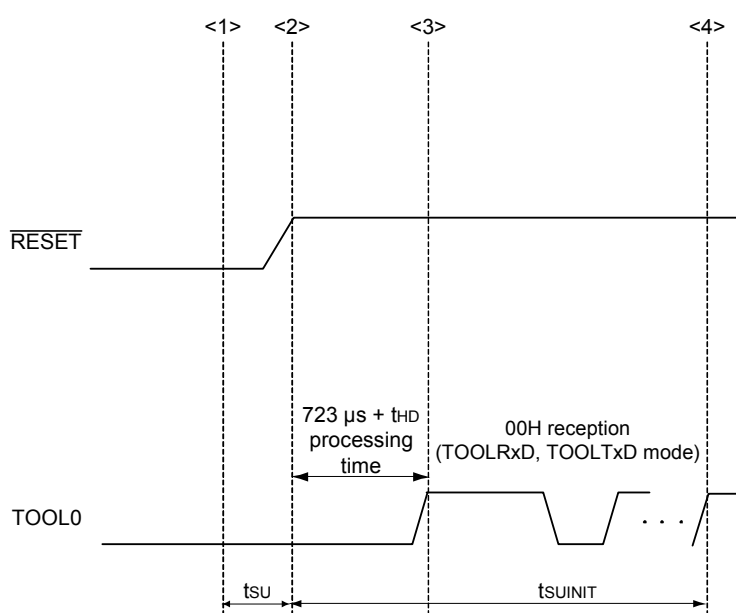
n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$		-10.0	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		-60.0	mA
	IOH2	Per pin for P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(\text{IOH} \times 0.7)/(n \times 0.01)$
 <Example> Where $n = 80\%$ and $\text{IOH} = -10.0\text{ mA}$
 Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			80.0	mA
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

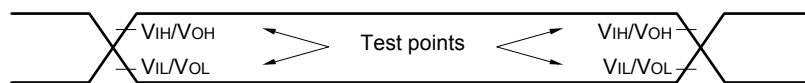
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(4) Peripheral Functions (Common to all products)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

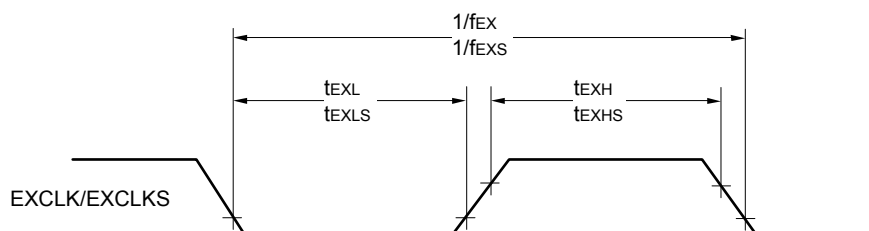
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fIL = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMP5 Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

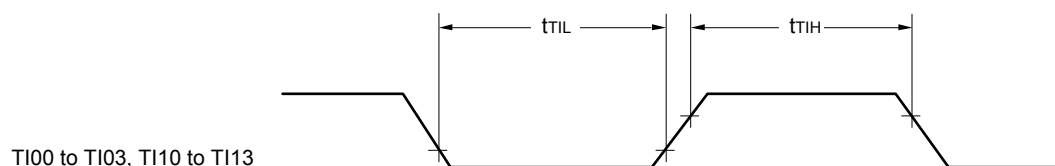
AC Timing Test Points



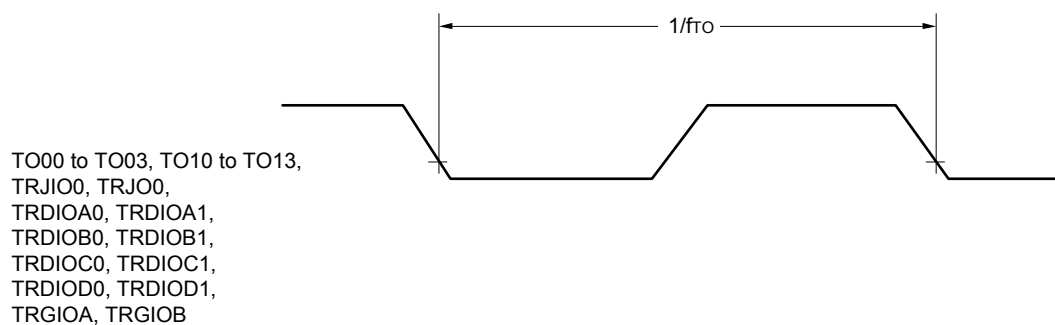
External System Clock Timing



TI/TO Timing



TI00 to TI03, TI10 to TI13



TO00 to TO03, TO10 to TO13,
TRJIO0, TRJO0,
TRDIOA0, TRDIOA1,
TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1,
TRDIOD0, TRDIOD1,
TRGIOA, TRGIOB

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V,

Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

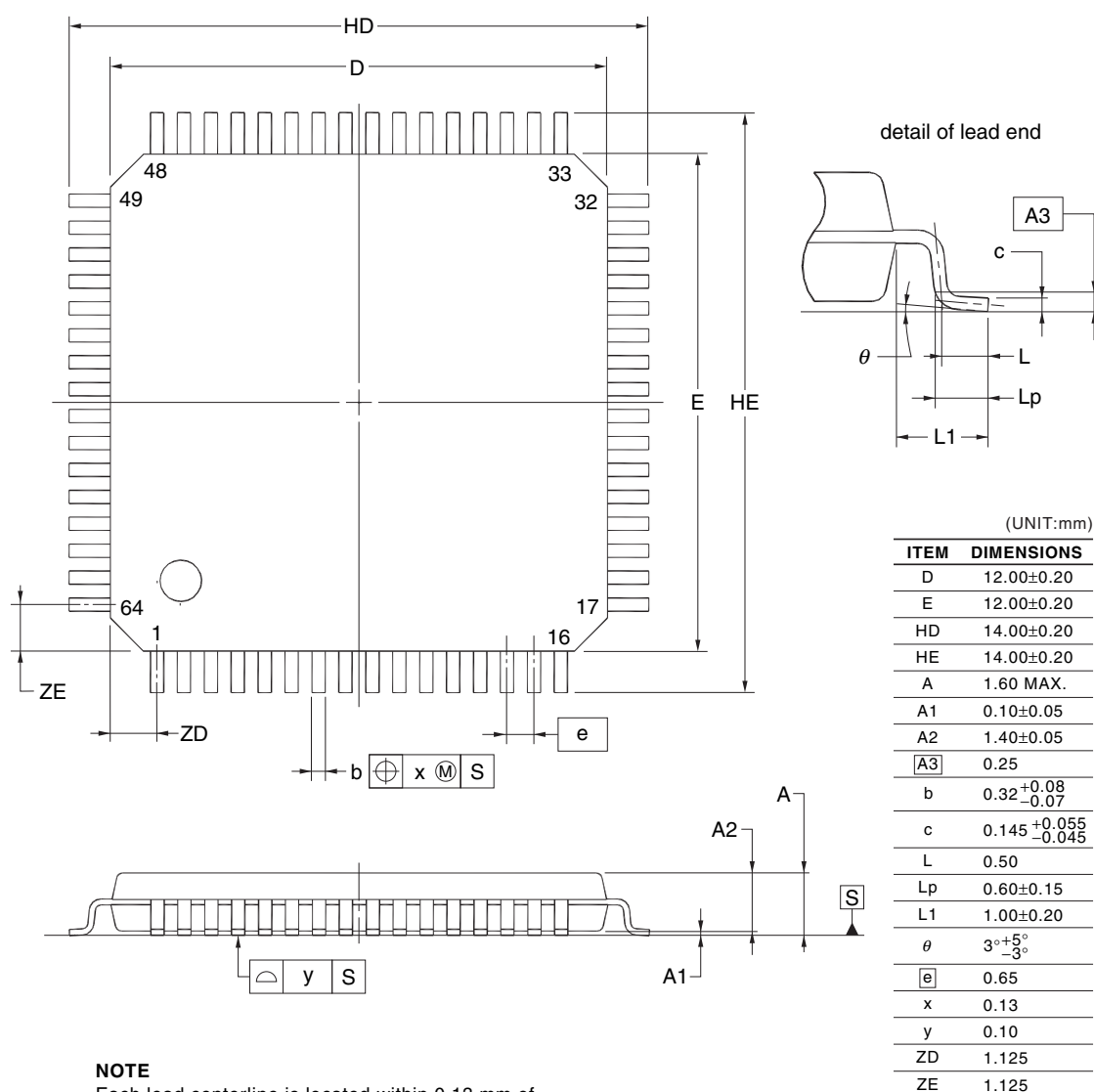
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

4.8 64-pin products

R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFa, R5F104LHAFA, R5F104LJAFA
 R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFa, R5F104LHDFA, R5F104LJDFA
 R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
 R5F104LKAFA, R5F104LLAFA
 R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB

